```
1
2   `timescale 1ns/100ps
3
4
5   module tb_CPU_6502 ;
6
7   parameter word_size=8,addr_size=16,Sel1_size=4,Sel2_size=3,state_size=5,cnt_size=4,
    ASize=3;
8
9     reg clk, rst;
10    reg [ASize-1:0] rptr;
11    wire [word_size-1:0] rdout;
12
13    wire [word_size-1:0]  instruction, DBus_1,DBus_2,DBus_3;
14    wire [addr_size-1:0]  ABus;
15    wire [addr_size-1:0]  address;
16    wire [word_size-1:0]          rom_word,ram_word;
17
18    wire Load_ACC,Inc_ACC,Dec_ACC;
19    wire Load_SP,Inc_SP,Dec_SP;
20    wire Load_X;
21    wire Load_Y;
22
23    wire Load_ALU,Load_FLAG;
24    wire Load_IR, Load_ALB;
25    wire Load_PC_H,Load_PC_L, Inc_PC, Dec_PC;
26    wire Load_DAR_H,Load_DAR_L;
27    wire Load_DR,Load_DB,Reset_Vector;
28
29    wire Sel1_ALU;
30    wire Sel1_PC1, Sel1_PC2, Sel1_DAR1, Sel1_DAR2;
31    wire Sel1_ACC, Sel1_IR;
32    wire Sel1_DR,Sel1_DB;
33    wire Sel1_SP1,Sel1_SP2,Sel1_X,Sel1_Y,Sel1_ALB,Sel1;
34
35    wire Sel2_ALU;
36    wire Sel2_PC1, Sel2_PC2, Sel2_DAR1, Sel2_DAR2;
37    wire Sel2_ACC, Sel2_IR;
38    wire Sel2_DR,Sel2_DB;
39    wire Sel2_SP1,Sel2_SP2,Sel2_X,Sel2_Y,Sel2_ALB,Sel2;
40
41    wire Sel3_ALU ,Sel3_ACC,Sel3_IR,Sel3_PC1,Sel3_DAR1,
42            Sel3_DR,Sel3_DB,Sel3_SP1,Sel3_X,Sel3_Y,Sel3_FLAG,Sel3 ;
43    wire Sel4_DAR2, Sel4_PC2, Sel4_SP2;
44
45    wire RWn;
46    wire zero;
47    wire [addr_size-1:0] Reg_PC;
48    wire [state_size-1:0] state;
49    wire [3:0] T;
50
51
52
53   CPU_6502 CPU
54          (
55                  clk, rst,
56
57       rptr,
58       rdout,
```

```
59
60                  instruction,
61                  DBus_1,DBus_2,DBus_3,
62      ABus,
63      address,
64
65                  rom_word,ram_word,
66
67                  Load_ACC,Inc_ACC,Dec_ACC,
68                  Load_SP,Inc_SP,Dec_SP,
69                  Load_X,
70                  Load_Y,
71
72          Load_ALU,Load_FLAG,
73                  Load_IR, Load_ALB,
74                  Load_PC_H,Load_PC_L, Inc_PC, Dec_PC,
75                  Load_DAR_H,Load_DAR_L,
76                  Load_DR,Load_DB,Reset_Vector,
77
78                  Sel1_ALU,
79                  Sel1_PC1, Sel1_PC2, Sel1_DAR1, Sel1_DAR2,
80                  Sel1_ACC, Sel1_IR,
81                  Sel1_DR,Sel1_DB,
82                  Sel1_SP1,Sel1_SP2,Sel1_X,Sel1_Y,Sel1_ALB,Sel1,
83
84                  Sel2_ALU,
85                  Sel2_PC1, Sel2_PC2, Sel2_DAR1, Sel2_DAR2,
86                  Sel2_ACC, Sel2_IR,
87                  Sel2_DR,Sel2_DB,
88                  Sel2_SP1,Sel2_SP2,Sel2_X,Sel2_Y,Sel2_ALB,Sel2,
89
90                  Sel3_ALU ,Sel3_ACC,Sel3_IR,Sel3_PC1,Sel3_DAR1,
91                  Sel3_DR,Sel3_DB,Sel3_SP1,Sel3_X,Sel3_Y,Sel3_FLAG,Sel3,
92
93                  Sel4_DAR2, Sel4_PC2, Sel4_SP2,
94
95                  RWn,
96                  zero,
97                  Reg_PC,
98                  state,
99                  T
100     );
101   defparam CPU.word_size =word_size,CPU.addr_size =addr_size,CPU.state_size=
    state_size, CPU.cnt_size =cnt_size;
102   defparam CPU.ASize=3;
103
104 always #10 clk=~clk;
105
106 initial
107   begin
108     #0  clk=1'b0; rst=1'b1;
109     #90  rst=1'b0;
110     #100 rst=1'b1;rptr=0;
111
112   end
113 endmodule
114
```