```
module Reg_file
  #(parameter DSize=8,ASize=5)
  (
    output reg [DSize-1:0] dout,
    input [DSize-1:0] din,
    input [ASize-1:0] addr,
    input Load_R,RW_n,
    input clk,rst
    );

 reg [DSize-1:0]R[2**ASize-1:0];

 assign dout = R[addr] ;

 always @(posedge clk or negedge rst)
  begin
   if(!rst)
     R[addr]=0;
   else if(Load_R & !RW_n)
    R[addr]= din;
  end
 endmodule
```