op1[3..0] INPUT VCC

op2[3..0] INPUT VCC

result[3..0] OUTPUT

cy_in INPUT VCC

op2[0] op1[0]

result[0]

op2[1] op1[1]

result[1]

op2[2] op1[2]

result[2]

op2[3] op1[3]

result[3]

alu_slice

cy_in   result
op1   cy_out
op2
S
V
R

alu_slice_bit_0

alu_slice

cy_in   result
op1   cy_out
op2
S
V
R

alu_slice_bit_1

alu_slice

cy_in   result
op1   cy_out
op2
S
V
R

alu_slice_bit_2

alu_slice

cy_in   result
op1   cy_out
op2
S
V
R

alu_slice_bit_3

OUTPUT cy_out

XOR
inst

OUTPUT vf_out

S INPUT VCC
V INPUT VCC
R INPUT VCC

PROJECT	**A-Z80**	MODULE **alu_core**
DESIGNER	Goran Devic	
DATE	May 18, 2014	REV 1.2

alu_core.bdf