RXAUI Interface and RXAUI Adapter Specifications

Doc. No. MV-S105386-00, Rev. A
June 3, 2008, Preliminary
CONFIDENTIAL
Document Classification: Proprietary Information

Document Conventions

	**Note:** Provides related information or information of special importance.
	**Caution:** Indicates potential damage to hardware or software, or loss of data.
	**Warning:** Indicates a risk of personal injury.

Document Status

Doc Status: Preliminary	Technical Publication: 0.xx

For more information, visit our website at: www.marvell.com

Table of Contents

List of Tables

List of Figures

1 Introduction

In recent years, the 10 Gigabit Ethernet market has expanded rapidly and it will continue to grow in the years to come. This rapid growth is the result of cost reduction, market demands, and a mature technology. In the coming years new products will be required to enable increased bandwidth, higher port density, and lower power and reduced cost.

A typical MAC/PHY interface uses the IEEE 802.3ae XGXS interface also known as XAUI, which runs four lanes of SERDES, running at 3.125 GHz in each direction, between the MAC and the PHY, using four 8/10 PCS lanes.

This document introduces a new interface called Reduced XAUI (RXAUI), which is based on 6.25 GHz SERDES. It requires two lanes, instead of the standard four 3.125 GHz XAUI SERDES, to achieve the same effective 10 Gbps rate.

RXAUI enables doubling the number of 10 GbE ports supported by a given number of SERDES, leading to a significant reduction in power, as well as silicon and system cost.

6.25 GHz SERDES has been chosen because it provides the optimal mW/Gbps and mm^2/Gbps for 90/65/45 nm technologies, based on a survey of the market.

Additionally, this document specifies the Marvell XAUI to RXAUI Adapter, which is provided as Verilog RTL code. It can be used by system vendors implementing an ASIC or FPGA, to interface with the Marvell advanced multi-10-GbE port devices that incorporate an RXAUI interface.

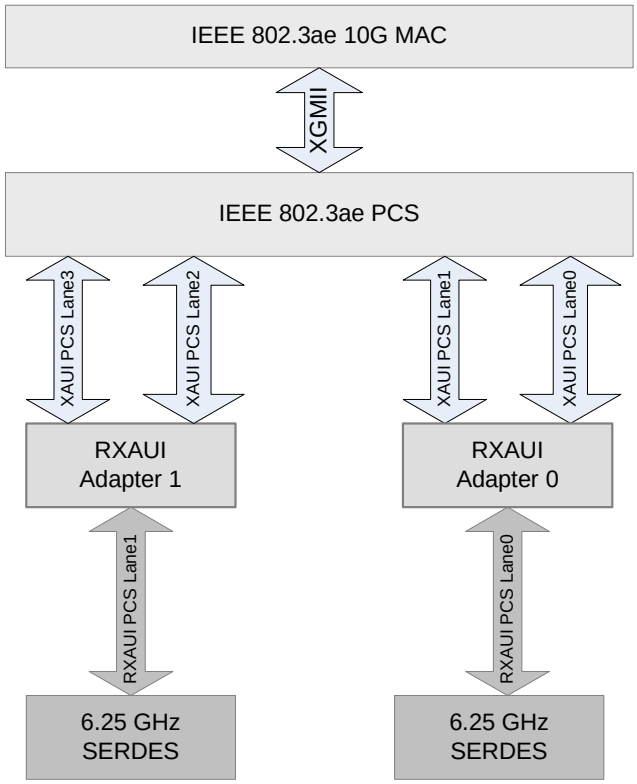
2 RXAUI Interface Functional Specifications

2.1 Overview

RXAUI is implemented as an Adapter layer (or Mux/Demux layer) between the two 6.25 GHz SERDES lanes (PMA) and the standard IEEE 802.3ae clause 48 XAUI PCS sub-layer. It is introduced as an in-line Mux/Demux layer, which does not require changes in the standard 10 GbE MAC and PCS or any of the inter-layer interfaces defined by IEEE. The Mux/Demux layer does not alter 10-bit symbols. This preserves existing designs created for ASICs, NPUs, and FPGAs.

Figure 1 illustrates the location of the RXAUI Adapter block. Note that two identical blocks are used.

Figure 1: RXAUI Adapter Block Location



On the transmit path each of the two RXAUI Adapters folds two XAUI PCS lanes from the PCS sub-layer onto a single RXAUI PCS lane running at double frequency.

On the receive path each of the two RXAUI Adapters de-muxes the recovered data and splits it back into two XAUI PCS lanes.

Note

As the folding of the two lanes into a single lane takes place after the PCS layer, the folded data stream does not obey the disparity rules required for the 6.25 GHz SERDES. However it is built from two lanes, each obeying the disparity rules. This introduces a minimal effect on Inter Symbol Interference (ISI) that has no practical influence on on-board terminations. To validate line quality, it is recommended to use the standard PRBS15 instead of the standard PRBS7.

2.2 RXAUI Adapter

2.2.1 Transmit Path

The RXAUI Adapter Transmit block receives two XAUI PCS lanes and interleaves them into a single lane.

The IEEE standard defines the XAUI PCS as four 10-bit lanes running at 312.5 MHz. Figure 2 illustrates how two of these lanes are folded into a single 10-bit RXAUI running at 625 MHz.

However in most of the currently deployed 10 GbE solutions, the four XAUI PCS lanes use 20-bit lanes running at 156.25 MHz.

Figure 2: Two 10-bit XAUI Lanes to a Single 10-bit RXAUI Lane

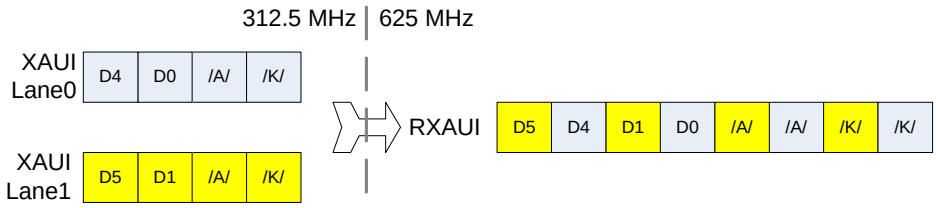


Figure 3: Two 20-bit XAUI Lanes to a Single 20-bit RXAUI Lane

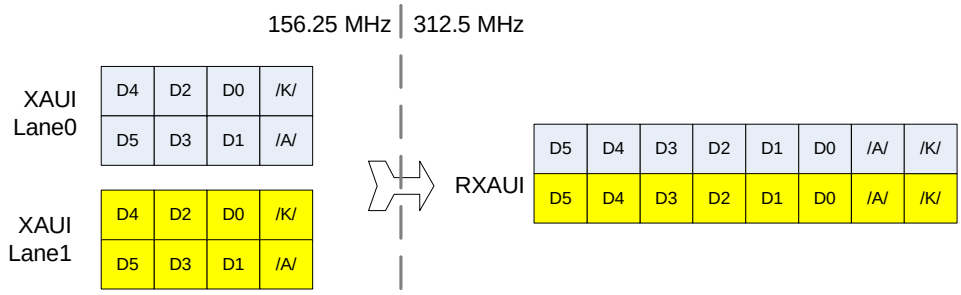


Figure 3 illustrates how two 20-bit XAUI PCS lanes running at 156.25 MHz are folded into a single 20-bit RXAUI running at 312.5 MHz.

Interleaving the two lanes onto a single lane implies a clock domain crossing. It is assumed that both clock domains—XAUI and RXAUI (fast)—are driven by a single PLL. Therefore there is no frequency PPM difference and the phase difference between the two clocks is constant.

On every two RXAUI clock cycles, both lanes are fetched and data is forwarded towards the 6.25 GHz SERDES. In 20-bit mode, on the first cycle, the two LSB symbols from each lane are sent. The two MSB symbols are sent on the second clock cycle. Lane0 data is sent on the LSB symbol of the transmitted word.

Note The /A/ symbol appears in pairs on the RXAUI lane. This is because the XAUI PCS transmits an ||A|| column (word-set) on all four slow-lanes concurrently. This property is used by the Receive Demux block to split the lanes.

2.2.2 Receive Path

The RXAUI Adapter Receive block receives a single RXAUI PCS lane and distributes it onto two XAUI PCS lanes.

The IEEE standard defines the XAUI PCS as four 10-bit lanes running at 312.5 MHz. Figure 4 illustrates how a single 10-bit RXAUI lane running at 625 MHz is distributed onto two 10-bit XAUI PCS lanes running at 312.5 MHz.

However in most of the currently deployed 10 GbE solutions, the four XAUI PCS lanes use 20-bit lanes running at 156.25 MHz. Figure 5 illustrates how a single 20-bit RXAUI running at 312.5 MHz is distributed onto two 20-bit XAUI PCS lanes running at 156.25 MHz.

Figure 4: Single 10-bit RXAUI Lane to Two 10-bit XAUI Lanes

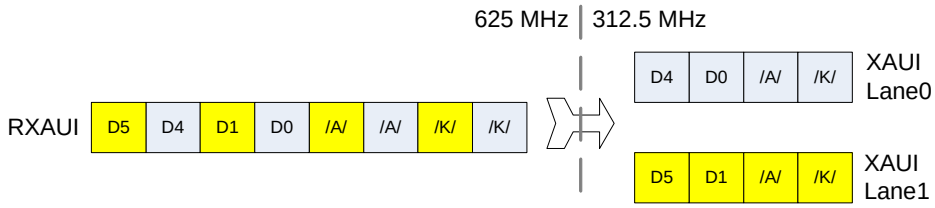
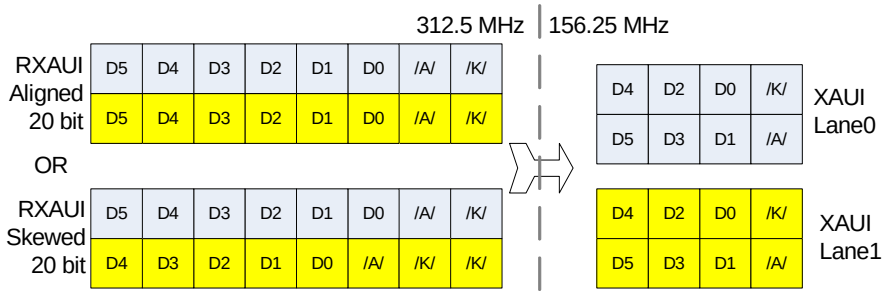


Figure 5: Single 20-bit RXAUI lane to Two 10-bit XAUI Lanes

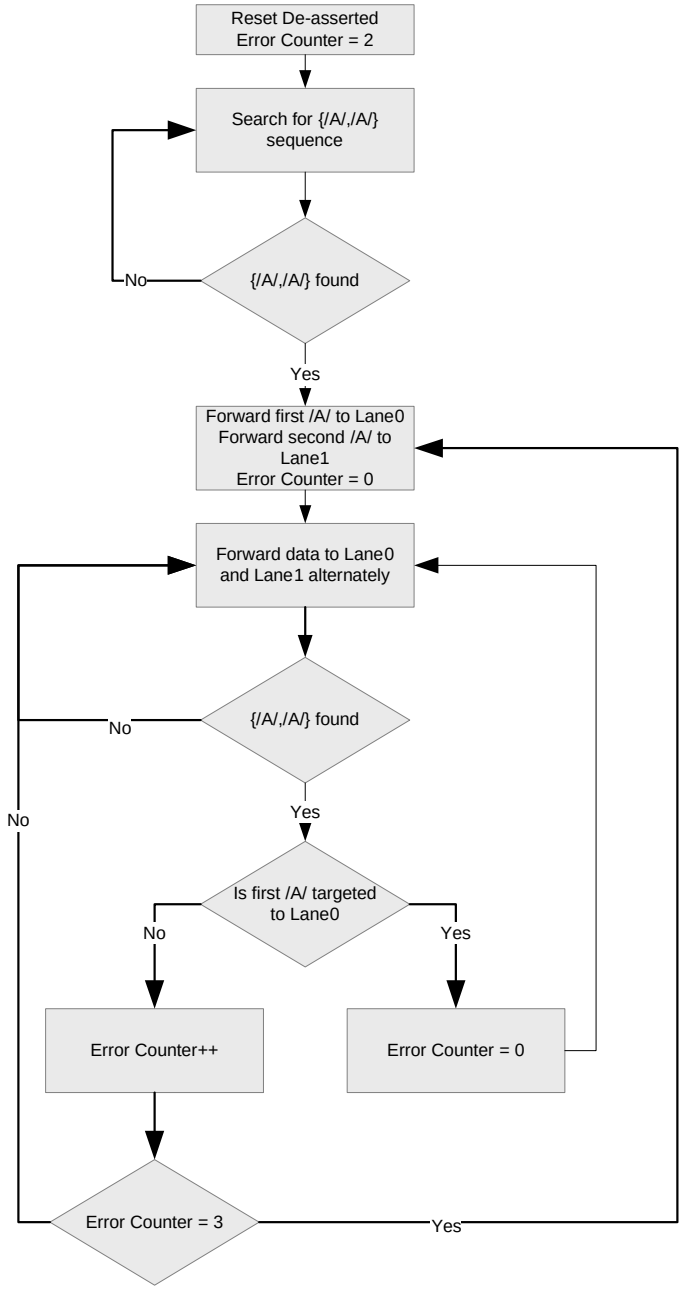


On the receive side, one lane data is divided between two lanes running at half clock frequency. The receiver always waits for the first /A/ symbol to align the stream. The first /A/ symbol is identified by the sequence {/A/,/A/}. After identifying this sequence, the first /A/ symbol is sent to Lane0, and from this point data is distributed to the lanes alternately. The receiver keeps searching for the sequence {/A/,/A/} for dynamic lane alignment, thus improving noise immunity. When this sequence is

identified, the distribution order is checked for correctness, i.e., the first /A/ is indeed targeted to Lane0. The receiver enforces the first /A/ to be forwarded to Lane0 only after three consecutive errors in forwarding correctness. After reset and before matching the first /A/, the receiver passes the data alternately without any guarantee for data correctness.

Figure 6 illustrates the receive flow.

Figure 6: Receive Flow



Note

SERDES output towards the MAC is not aligned, i.e., the 20 bits received from the SERDES are not aligned to 10-bit words. Before the identification of any symbol the words must be aligned using a preceding Comma Detect block. The Comma Detect block is enabled immediately after reset and is disabled when both lanes' Sync_OK indications from the PCS layer are asserted.

3 Marvell RXAUI Adapter

3.1 Introduction

The Marvell RXAUI Adapter is designed to enable the connection of four lanes of 8/10 PCS to two 6.2 GHz SERDES lanes. It is provided as verilog RTL code and can be used by system vendors implementing ASIC or FPGA to interface with the Marvell advanced multi-10-GbE ports devices that incorporate RXAUI interface.

The RXAUI Adapter implements all the RXAUI interface functions as specified in Section 2,RXAUI Interface Functional Specifications.

The RXAUI Adapter is connected to two PCS lanes at one end and to a single RXAUI SERDES at the other end.

To implement a 10 GbE RXAUI interface, two instances of the RXAUI Adapter are needed, as illustrated in Figure 1, “RXAUI Adapter Block Location.

The RXAUI Adapter is implemented using 20 bits per lane on both the PCS and SERDES sides.

The RXAUI Adapter provides both Rx and Tx clock to the 10 GbE PCS.

Additionally, on the receive path it also provides comma detection functionality.

3.2 External Interfaces

Table 1 specifies the Marvell RXAUI Adapter’s external interfaces.

Table 1: RXAUI Adapter External Interfaces

Signal Name	I/O	Description
6.25 GHz SERDES INTERFACE		
Clocks		
s_tx_clk	I	312.5 MHz Tx clock from the 6.25 GHz RXAUI SERDES
s_rx_clk	I	312.5 MHz Rx clock from the 6.25 GHz RXAUI SERDES
Data and Control		
rxaui_tx_data[19:0]	O	Tx data to the 6.25 GHz RXAUI SERDES Synchronized to s_tx_clk
rxaui_rx_data[19:0]	I	Rx data from the 6.25 GHz RXAUI SERDES Synchronized to s_rx_clk

Table 1: RXAUI Adapter External Interfaces (Continued)

Signal Name	I/O	Description
XAUI PCS INTERFACE		
Clocks		
txclk_out	O	156.25 MHz Tx clock to both lanes of PCS Generated by dividing s_tx_clk by two. **NOTE:** As this clock is generated from the SERDES s_tx_clk it can be used as the source 156.25 MHz clock of the PCS and MAC. When connecting two blocks of RXAUI Adapter to four lanes of PCS, only one of the txclk_out outputs is used; the other can be left NC.
rx_clk0	O	156.25 MHz Rx clock to PCS Lane0 Generated by dividing s_rx_clk by two.
rx_clk1	O	156.25 MHz Rx clock to PCS Lane1 Generated by dividing s_rx_clk by two.
txclk_in0	I	Lane0 Tx clock This clock is txclk_out after the PCS and MAC block clock tree. Used for providing source synchronous interface for txdata_serdes0[19:0].
txclk_in1	I	Lane1 Tx clock This clock is txclk_out after the PCS and MAC block clock tree. it is used for providing source synchronous interface for txdata_serdes1[19:0].
Data and Control		
txdata_serdes0[19:0]	I	Tx data from XAUI PCS Lane0 Synchronized to txclk_in0.
txdata_serdes1[19:0]	I	Tx data from XAUI PCS Lane1 Synchronized to txclk_in1.
rxdata_serdes0[19:0]	O	Rx data to XAUI PCS Lane0 Synchronized to rx_clk0.
rxdata_serdes1[19:0]	O	Rx data to XAUI PCS Lane1 Synchronized to rx_clk1.
sync_ok_lane0	I	XAUI PCS Lane0 is synchronized Used by the Comma Detect machine to start/stop comma detection process.
sync_ok_lane1	I	XAUI PCS Lane1 is synchronized Used by the Comma Detect machine to start/stop comma detection process.
lock	O	Comma Detect is locked. Status output

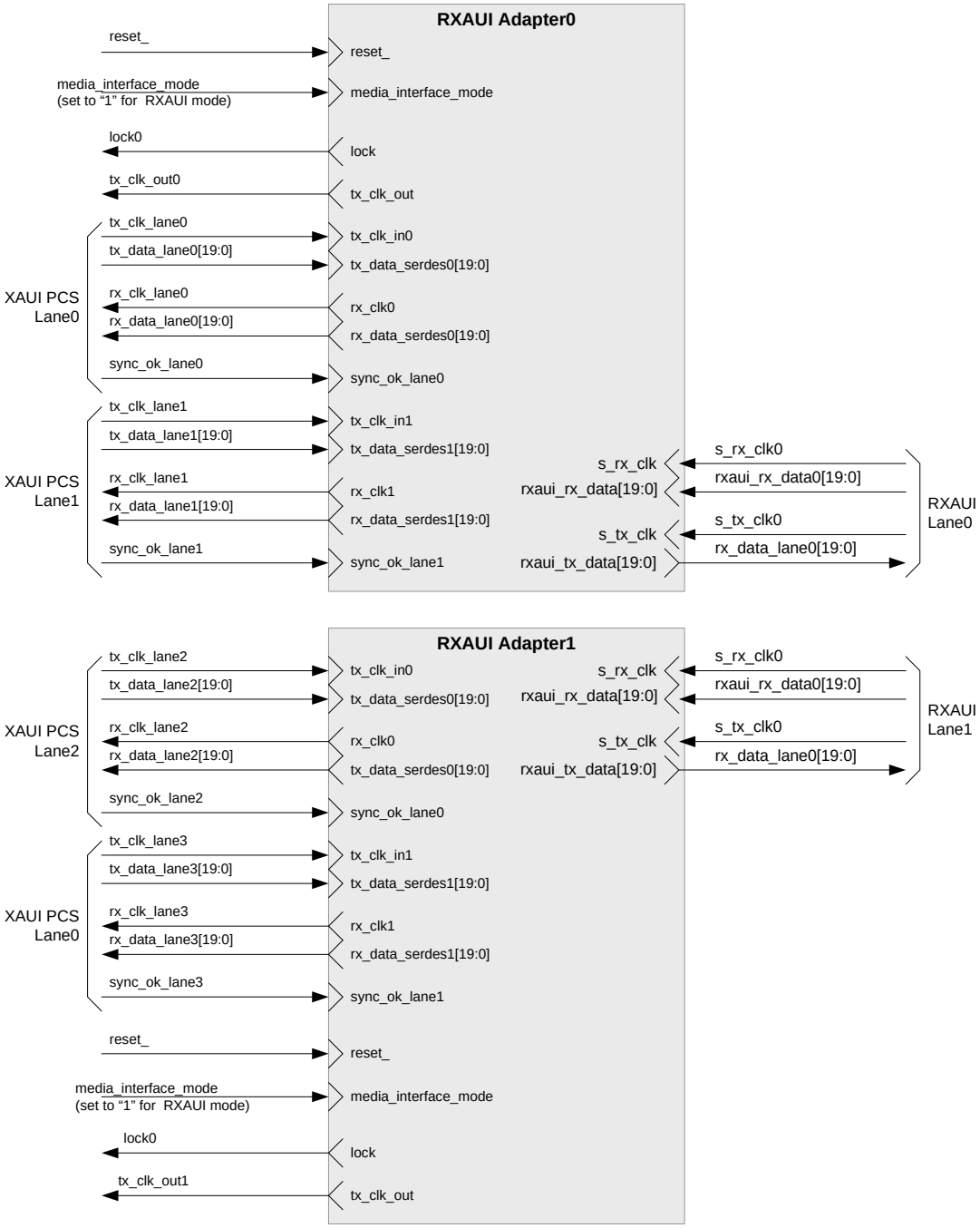
Table 1: RXAUI Adapter External Interfaces (Continued)

Signal Name	I/O	Description
GENERAL INTERFACE		
Reset		
reset_in_	I	Asynchronous reset. RXAUI Adapter synchronizes this reset per each of its clock domains.
CONFIGURATION INTERFACE		
media_interface_ mode	I	Working in XAUI or RXAUI 0 = XAUI Mode: In this mode XAUI PCS Lane0 is connected via the phase FIFO to the SERDES interface. Lane1 is not used 1 = RXAUI Mode

3.3 Connecting the Marvell RXAUI Adapter to XAUI PCS

Figure 7 illustrates how to connect the Marvell RXAUI Adapter to a XAUI PCS to implement a 10 Gbps RXAUI interface.

Figure 7: RXAUI Adapter Connection to XAUI PCS



Two blocks of RXAUI Adapter are used:

- XAUI PCS Lane0 and Lane1 are connected to RXAUI Adapter0 and then to RXAUI Lane0.
- XAUI PCS Lane2 and Lane3 are connected to RXAUI Adapter1 and then to RXAUI Lane1.

On the XAUI PCS side, each lane is a 20-bit source synchronous interface:

On Rx The RXAUI Adapter provides an rxclk0/1 per interface and provides the 20-bit rx_data_serdes0/1[19:0] synchronized to this clock.
Additionally the PCS Rx issues sync_ok_lane0/1, to indicate it has detected a comma.

On Tx The RXAUI Adapter expects a tx_clk_in0/1 per interface and 20-bit tx_data_serdes0/1[19:0] synchronized to this clock.

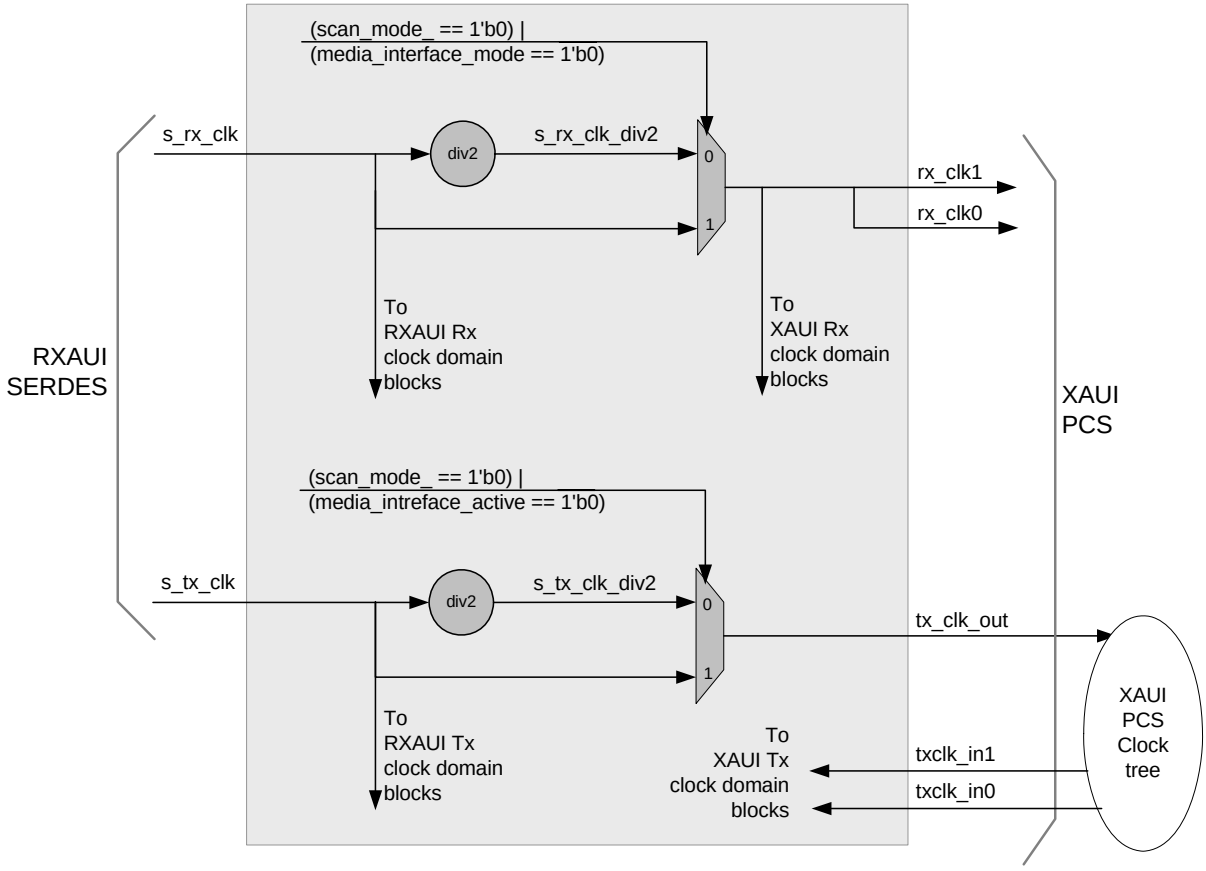
The tx_clk_out from one of the blocks is used as a reference 156.25 MHz clock to the PCS and MAC.

For RXAUI media_interface_mode must be set HIGH.

3.4 RXAUI Adapter: Clocks

Figure 8 illustrates the RXAUI Adapter clock scheme.

Figure 8: RXAUI Adapter Clock Scheme



On the Receive path:

- s_rx_clk is a 312.5 MHz clock provided by the 6.25 GHz SERDES.
- rxaui_rx_data[19:0] is synchronized to s_rx_clk.
- s_rx_clk is used in the RXAUI Adapter for the RXAUI Rx clock domain blocks (see Section 3.6).
- When media mode is RXAUI, s_rx_clk is divided by two to generate a 156.25 MHz clock.
- The divided clock is used in the RXAUI Adapter for the XAUI Rx clock domain blocks (see Section 3.6).
- The divided clock is also issued to the XAUI PCS block for both lanes of XAUI PCS —rx_clk0 and rx_clk1.
- The 20-bit data issued to XAUI PCS Lane0 rxdata_serdes0[19:0] is synchronized to rx_clk0.
- The 20-bit data issued to XAUI PCS Lane0 rxdata_serdes1[19:0] is synchronized to rx_clk1.

On the Transmit path:

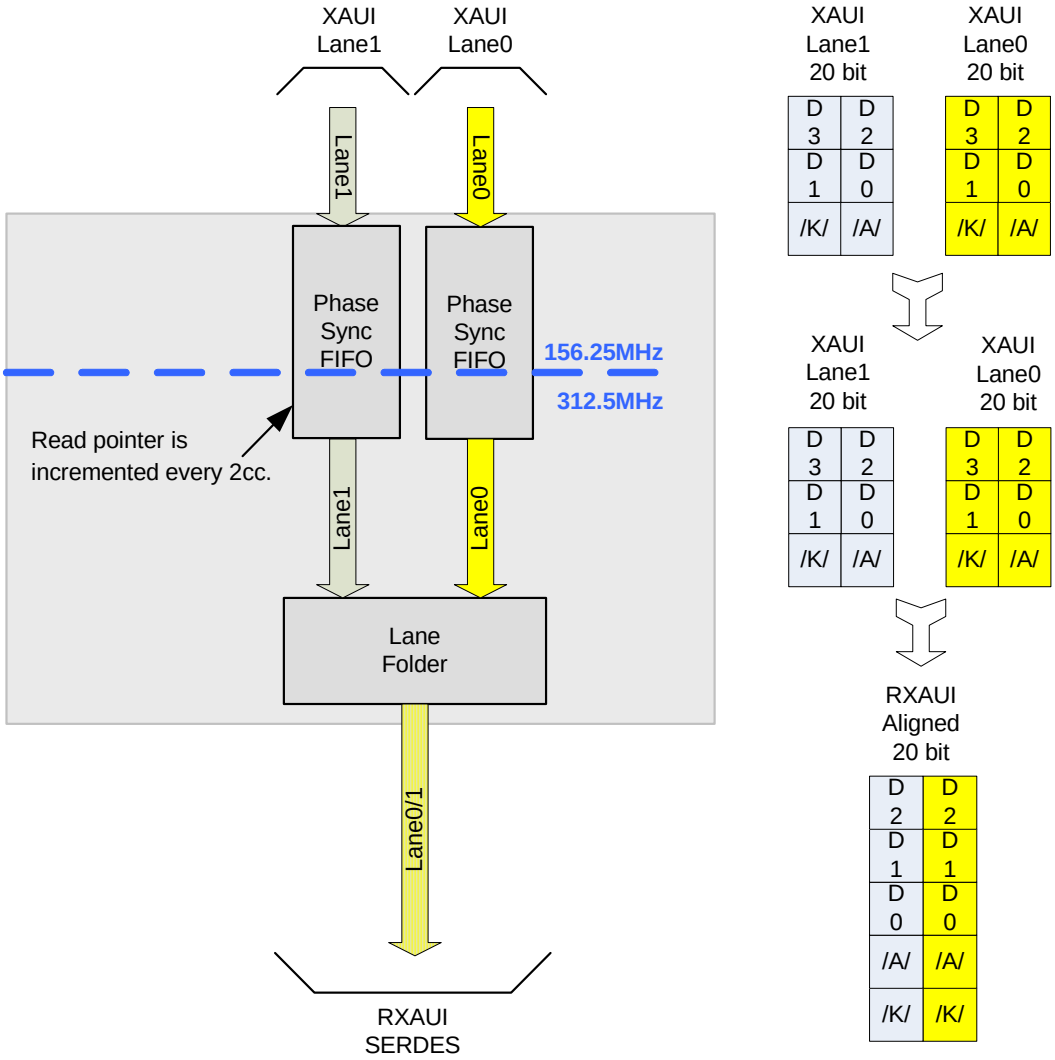
- s_tx_clk is a 312.5 MHz clock provided by the 6.25 GHz SERDES.
- rxaui_tx_data[19:0] is synchronized to s_tx_clk.
- s_tx_clk is used in the RXAUI Adapter for the RXAUI Tx clock domain blocks (see Section 3.5).
- When media mode is RXAUI, s_tx_clk is divided by two to generate a 156.25 MHz clock.
- The divided clock is issued to the XAUI PCS via txclk_out.
- txclk_out is the source 156.25 clock for the XAUI PCS block.
- txclk_in0 and txclk_in1 are derived from txclk_out after the clock tree of the XAUI PCS block.
- The 20-bit data issued to XAUI PCS Lane0 txdata_serdes0[19:0] is synchronized to txclk_in0.
- The 20-bit data issued to XAUI PCS Lane0 txdata_serdes1[19:0] is synchronized to txclk_in1.
- txclk_in0 and txclk_in1 are used in the RXAUI Adapter for the XAUI Tx clock domain blocks (see Section 3.5).

Note For interface timing and synthesis constraints, contact your Marvell representative.

3.5 RXAUI Adapter: Transmit Path

Figure 9 is a block diagram of the RXAUI Adapter transmit path.

Figure 9: RXAUI Adapter: Transmit Path Block Diagram



This diagram incorporates two phase synchronization FIFOs and a lane folder.

The phase synchronization FIFOs synchronize between the XAUI clock domain of 156.25 MHz and the RXAUI clock domain of 312.5 MHz.

txclk_in0 is the 156.25 MHz clock used for writing the 20-bit XAUI data of Lane0 into the Lane0 Phase Sync FIFO.

txclk_in1 is the 156.25 MHz clock used for writing the 20-bit XAUI data of Lane1 into the Lane1 Phase Sync FIFO.

s_tx_clk is the 312.5 MHz clock used for reading the data from the phase sync FIFOs.

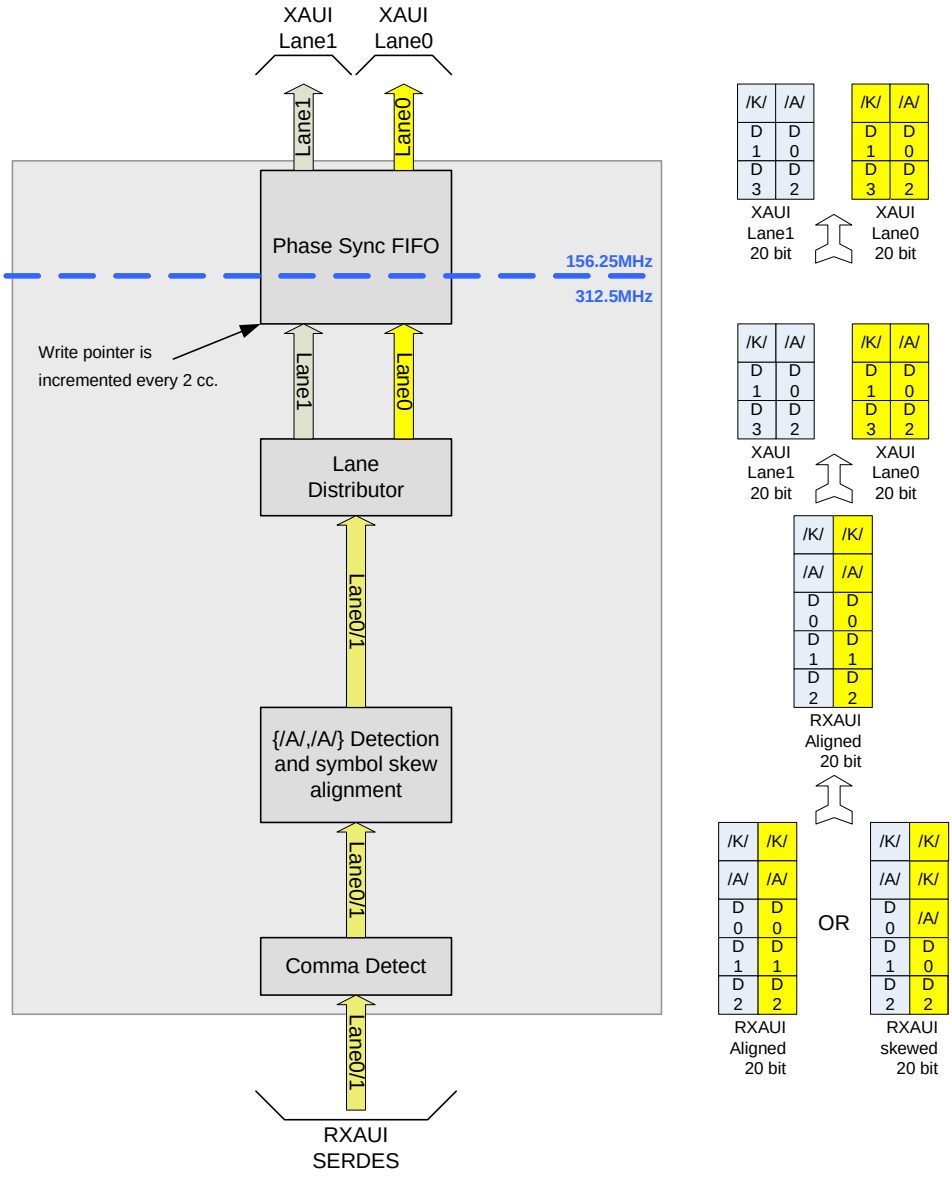
As described in Section 3.4, txclk_in0 and txclk_in1 are derived from s_tx_clk, thus s_tx_clk = 2*txclk_in0 and only phase synchronization is required.

The Lane folder folds the two XAUI lanes in to a single RXAUI lane, as described above.

3.6 RXAUI Adapter: Receive Path

Figure 10 is a block diagram of the RXAUI Adapter Receive path.

Figure 10: RXAUI Adapter: Receive Path Block Diagram



It incorporates a Comma Detect block, an {/A/,/A/} Detection and Symbol Skew Alignment block, a Lane Distribution block and a Phase synchronization FIFO.

3.6.1 Comma Detect

This block searches for a comma in the data received from the SERDES. After detecting a comma, the offset is locked and correct data is forwarded to the next block.

When it has found a comma, this block issues a lock status indication.

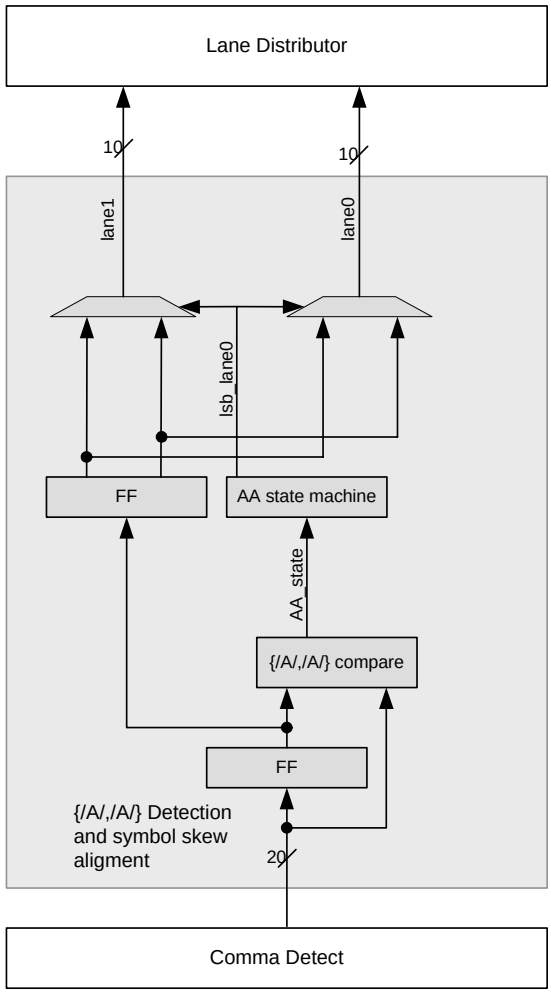
While sync_ok_lane0 or sync_ok_lane1 is LOW, this block continues to look for a comma symbol.

3.6.2 {/A/,/A/} Detection and Symbol Skew Alignment

This block searches for two consecutive {/A/,/A/}s, to distribute a data stream for Lane0 and Lane1.

Figure 11 illustrates this {/A/,/A/} detection and symbol skew alignment.

Figure 11: {/A/,/A/} Detection and Symbol Skew Alignment Block Diagram



This block receives a stream of 20-bit aligned RXAUI data at 312.5 MHz and issues a stream of 20-bit RXAUI data at 312.5 MHz. In the 20 bit output stream, the 10 LSBs are of XAUI Lane0 and the 20 MSBs are of XAUI Lane1.

The AA state machine follows the algorithm specified in Figure 6, Receive Flow, on page 9.

3.6.3 Lane Distributor

The Lane Distributor receives 20-bit RXAUI data at 312.5 MHz. In the 20 bit stream the 10 LSBs are of XAUI Lane0 and the 20 MSBs are of XAUI Lane1.

Every other 312.5 MHz clock cycle issues 40 bits of data—20 bits for XAUI Lane0 and 20 bits for XAUI Lane1. These 40 bits of data are written into the Phase Sync FIFO.

3.6.4 Phase Sync FIFO

s_rx_clk is the 312.5 MHz clock used for writing XAUI Lane0 20 bits and XAUI Lane1 20 bits into the phase sync FIFOs.

s_rx_clk_div2 is the 156.25 MHz clock used for reading the 20-bit XAUI data of Lane0 and the 20-bit XAUI data of Lane1 from the Phase Sync FIFO.

As described in Section 3.4,RXAUI Adapter: Clocks, s_rx_clk_div2, rx_clk0 and rx_clk1 are derived from, s_rx_clk. Thus Fs_rx_clk = 2*s_rx_clk_dive and only phase synchronization is required.

4 Revision History

Table 2:

Revision	Date	Comments
A	June 3, 2008	Initial Release

Marvell Semiconductor, Inc.
5488 Marvell Lane
Santa Clara, CA 95054, USA

Tel: 1.408.222.2500
Fax: 1.408.752.9028

www.marvell.com

Marvell. Moving Forward Faster