Revision History

Revision	Date	Author	Description
0.1	2008-06-22	Thomas Thanner	Initial Version

1 Introduction

This core is intended to be used as an interface between an external mixrocontroller and an FPGA. Within that FPGA several functions are embedded that are controlled by the external microcontroller.
Typically the microcontroller does not have a regular memory or I/O bus to interface to external functions. Therefore a simple solution using a parallel port is used here.

The WISBONE specification and additional information about WISHBONE SoC can be found at:

http://www.opencores.org/wishbone/

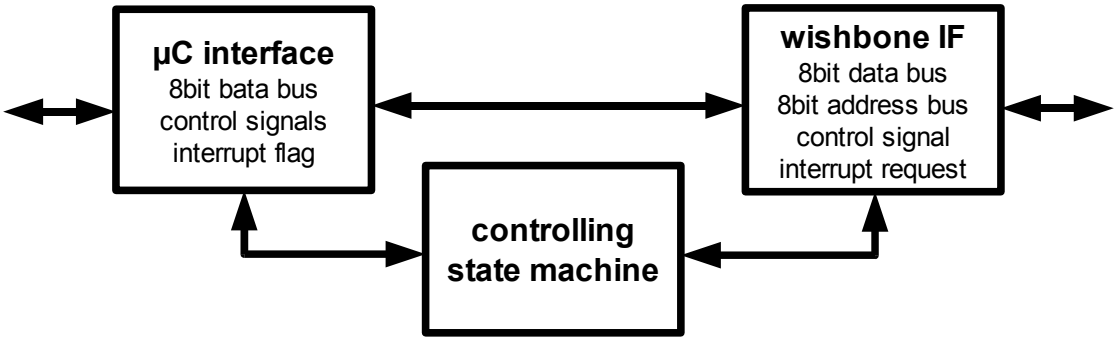
This interface is build according to wishbone specification B.3 (Sep. 7 2002)

The Main features of the Interface are:

- 8 bit bidirectional data bus
- two cycle bus transfer
- 8 bit internal register address transferred in first cycle
- 8 bit data transferred in second cycle
- asyncronous interface to microcontroller
- interrupt request line

2 Architecture

Below picture illustrates the overall architecture of the core:



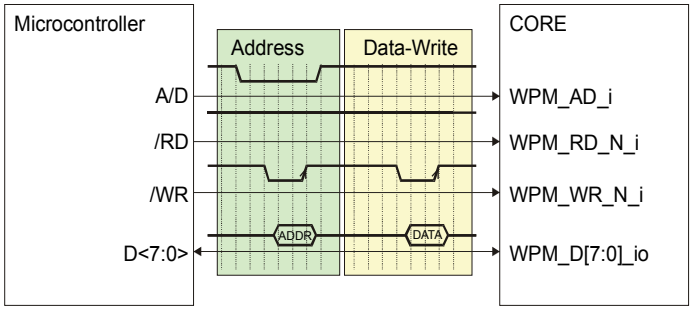
Two cycles on the microcontroller interface generate one cycle on the wishbone bus. First cycle transfers address, second cycle executes actual data transfer.

2.1 Microcontroller Interface

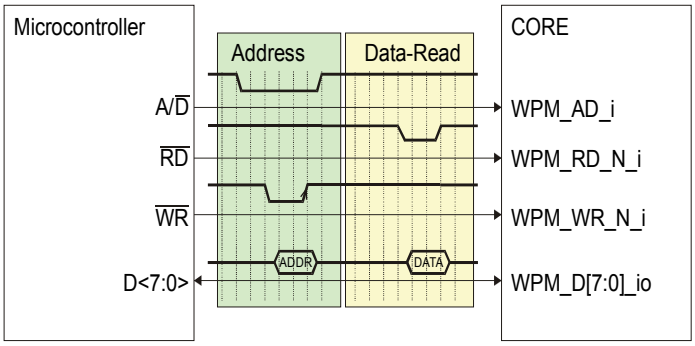
Communication between microcontroller and FPGA uses a simple parallel port. Microcontroller is bus master.

2.1.1 Standard Bus cycles

Write Cycle:



Read Cycle



Microcontroller puts /WR signal ("not write) low wile A/D is low as well and starts bus access. One access is completed after two cycles on the parallel bus. First bus cycle is always a write cycle and sets the 8bit address. Second cycle can be either read or write, depending on state of /WR and /RD lines.

2.1.2 Interrupt Request

The interrupt request output of the core is a simple copy of all internal interrupt request flags from other cores on the wishbone bus. It take off some load from the microcontroller. Using that signal no permanent check of all internal registers is required.

2.2 Wishbone Interface

Required documentation of the wishbone interface:

Revision Level of WISHBONE specification:
B.3, September 7, 2002

Type of interface:
Master

Port size:
8-bit

Port granularity:
8-bit

Maximum operand size:
8-bit

Transfer ordering:
BIG/LITTLE ENDIAN

Sequence of data transfer:
UNDEFINED

CLK_i costraints:
not defined yet

3 Core IOs

External microcontroller interface is a proprietary interface with the following signals:

Name	Width	Direction	Description
WPM_AD_pad_i	1	in	Address (Low) / Data (High) select
WPM_RD_n_pad_i	1	in	Low active read cycle marker
WPM_WR_n_pad_i	1	in	Low active write cycle marker
WPM_D_pad_i	8	in	Data input (during write cycles)
WPM_D_pad_o	8	out	Data output (during read cycles)
WPM_D_padoe_o	1	out	Output buffer enable (active high, during read cycles)
WPM_INT_o	1	out	High active Interrupt request output to microcontroller

Internal core interface is wishbone compatible master interface

Name	Width	Direction	Description
CLK_i	1	in	System clock
RST_i	1	in	Asynchronous system reset
DAT_i()	8	in	Data input, placed on microcontroller interface during read cycles
DAT_o()	8	out	Data output, sourced by microcontroller interface during write cycles
ACK_i	1	in	Acknowledge, terminates regular bus cycle
ADDR_o	8	out	Address output
CYC_o	1	out	Cycle output, indicates valid bus cycle in progress
STB_o	1	out	Strobe output, to validate data transfer cycle