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10GE MAC Core Specification

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Revision History

Rev.	Date	Author	Description
0.1	5/30/2008	A.Tanguay	Draft
0.2	6/6/2008	A.Tanguay	Added block diagram. Added mod[2:0] signals.

Contents

INTRODUCTION.....	1
ARCHITECTURE.....	2
OPERATION.....	4
REGISTERS.....	5
REGISTER LIST.....	5
CONFIGURATION REGISTER 0 – 0x00.....	5
INTERRUPT PENDING REGISTER – 0x08.....	6
INTERRUPT STATUS REGISTER – 0x0C.....	6
INTERRUPT MASK REGISTER – 0x10.....	7
CLOCKS.....	8
RESETS.....	9
IO PORTS.....	10
WISHBONE INTERFACE.....	10
PACKET RECEIVE INTERFACE.....	10
PACKET TRANSMIT INTERFACE.....	11
XGMII RECEIVE INTERFACE.....	12
XGMII TRANSMIT INTERFACE.....	13
WAVEFORMS.....	14
WISHBONE INTERFACE.....	14
PACKET RECEIVE INTERFACE.....	14
PACKET TRANSMIT INTERFACE.....	15
XGMII RECEIVE INTERFACE.....	15
XGMII TRANSMIT INTERFACE.....	15
TABLE 1: CONFIGURATION REGISTER 0.....	4
TABLE 2: LIST OF CLOCKS.....	6
TABLE 3: LIST OF CLOCKS.....	7
TABLE 4: LIST OF IO PORTS.....	8
TABLE 5: LIST OF IO PORTS.....	9
TABLE 6: LIST OF IO PORTS.....	9
TABLE 7: LIST OF IO PORTS.....	9

TABLE 8: LIST OF IO PORTS.....9

1.

Introduction

The 10GE MAC core is designed for easy integration with proprietary custom logic. It features a POS-L3 like interface for the datapath and a Wishbone compliant interface for management. The core was intentionally designed with a limited feature set for a small gate footprint.



2.

Architecture

A block diagram of the core is presented in the figure below.

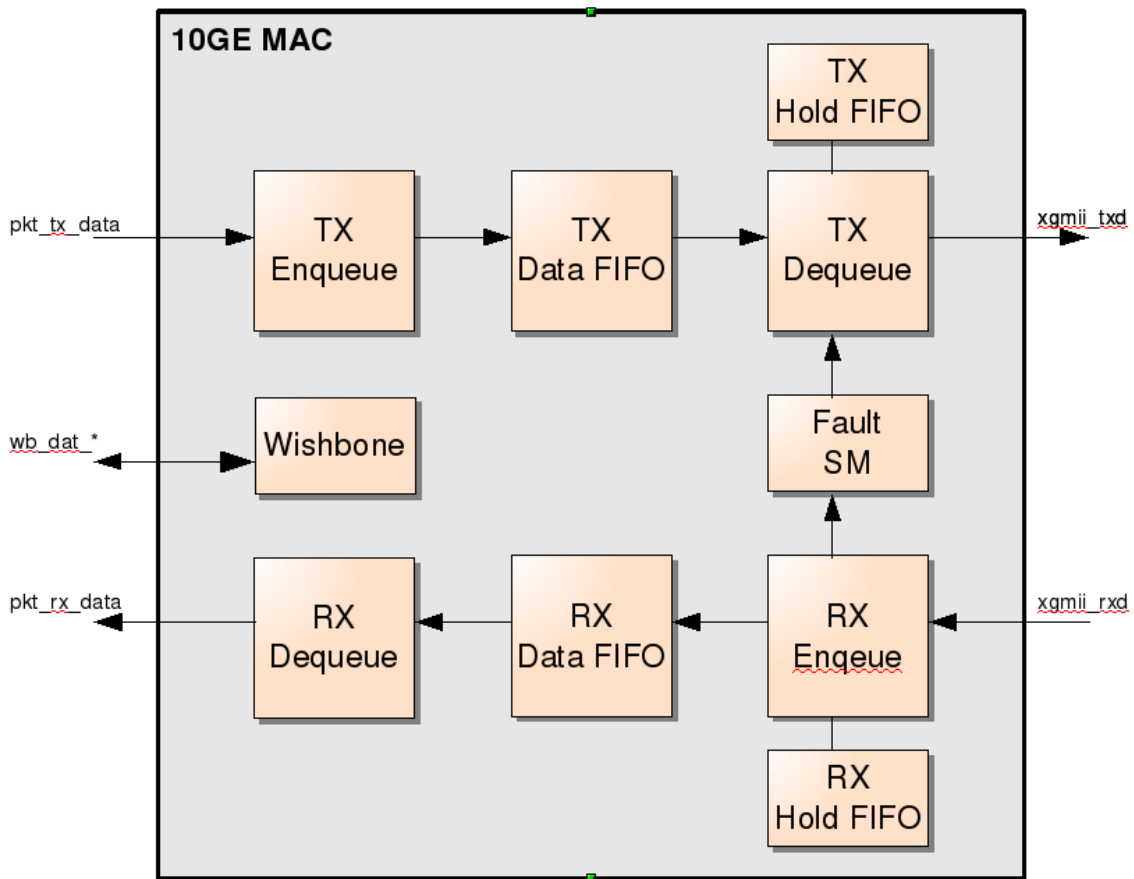


Figure 1: Block Diagram

3.

Operation

Operation. TBD.

4.

Registers

Register List

Name	Address	Width	Access	Description
Configuration Register 0	0x00	32	R/W	
Interrupt Pending Register	0x08	32	COR	
Interrupt Status Register	0x0c	32	RO	
Interrupt Mask Register	0x10	32	R/W	

Configuration Register 0 – 0x00

The registers of the WISHBONE slave unit start at offset 0x180.

RESET VALUE: 0x00000001

Bit #	Name	Description
31 - 1	Reserved	Reserved field. Reading returns zeros.
0	TX Enable	When set, transmission of frames is enabled. This bit is set by default.

Table 1: Configuration Register 0

Interrupt Pending Register – 0x08

This register is clear-on-read and provides an indication of pending interrupts.

RESET VALUE: 0x00000000

Bit #	Name	Description
31 - 9	Reserved	Reserved field. Reading returns zeros.
8	RX Fragment Error	When set, indicates that a fragment was received. A fragment is a frame that has a start of frame delimiter but no end of frame. Typically it is immediately followed by a new start of frame.
7	RX CRC Error	When set, indicates that a frame was received with invalid CRC.
6	RX Pause Frame	When set, indicates that a pause frame was received. Pause frames are discarded.
5	Remote Fault	When set, indicates that the fault state-machine has transitioned in or out of remote fault condition.
4	Local Fault	When set, indicates that the fault state-machine has transitioned in or out of local fault condition.
3	RX Data Fifo Underflow	When set, indicates that the receive data FIFO has experienced underflow. This may occur if “pkt_rx_ren” is asserted when no data is available in the receive FIFO.
2	RX Data Fifo Overflow	When set, indicates that the receive data FIFO has experienced overflow. This may occur if “pkt_rx_ren” remains de-asserted for a too long period while data is present in the receive FIFO.
1	TX Data Fifo Underflow	When set, indicates that the transmit data FIFO has experienced underflow. This situation should never occur.
0	TX Data Fifo Overflow	When set, indicates that the transmit data FIFO has experienced overflow. This may occur if “pkt_tx_val” is asserted and no room is left in the transmit FIFO.

Table 2: Interrupt Pending Register

Interrupt Status Register – 0x0C

This register is read-only and provides a direct status of interrupt lines used to set bits in the Interrupt Pending Register.

RESET VALUE: 0x00000000

Bit #	Name	Description
31 - 0	Interrupt Status	Each bit corresponds to an interrupt in the Interrupt

Bit #	Name	Description
		Pending Register.

Table 3: Interrupt Status Register

Interrupt Mask Register – 0x10

This register is read/write and can be used to enable individual interrupts. By default all interrupts are disabled.

RESET VALUE: 0x00000000

Bit #	Name	Description
31 - 0	Interrupt Mask	Each bit corresponds to an interrupt in the Interrupt Pending Register. Setting a bit enables the interrupt.

Table 4: Interrupt Mask Register

5.

Clocks

This section describes the various clocks required by the 10GE MAC core.

Name	Frequency	Description
wb_clk_i	30 - 156Mhz	Wishbone interface clock.
clk_156m25	156.25Mhz	Clock for transmit and receive packet interfaces towards user's core logic. "pkt_tx_*" and "pkt_rx_*" signal are timed to this clock.
clk_xgmii_rx	156.25Mhz	Clock for XGMII receive interface between 10GE MAC core and XAUI/PCS macro.
clk_xgmii_tx	156.25Mhz	Clock for XGMII transmit interface between 10GE MAC core and XAUI/PCS macro.

Table 5: 10GE MAC Clocks

6.

Resets

This section describes the various resets required by the 10GE MAC core. The user must ensure that each reset is synchronously de-asserted with it's corresponding clock. To ensure that transmit and receive FIFO's are initialized correctly, “reset_156m25_n”, “reset_xgmii_rx_n” and “reset_xgmii_tx_n” must be de-asserted within 2-cycles of each other.

Name	Description
wb_rst_i	Wishbone interface reset. Active high. Must be de-asserted synchronous to wb_clk_i.
reset_156m25_n	Core packet interfaces clock domain reset. Active low. Must be de-asserted synchronous to clk_156m25.
reset_xgmii_rx_n	XGMII receive clock domain reset. Active low. Must be de-asserted synchronous to clk_xgmii_rx.
reset_xgmii_tx_n	XGMII transmit clock domain reset. Active low. Must be de-asserted synchronous to clk_xgmii_tx.

Table 6: 10GE MAC Resets

7.

IO Ports

This section specifies the 10GE MAC core IO ports.

Wishbone Interface

Refer to Wishbone interface specification for more details on these signals.

Port	Direction	Description
wb_adr_i [7:0]	Input	Address input. All accesses to core must be 32-bit. Bits 0 and 1 are not used.
wb_cyc_i	Input	Wishbone cycle.
wb_dat_i [31:0]	Input	Wishbone data input.
wb_stb_i	Input	Wishbone strobe.
wb_we_i	Input	Wishbone write enable.
wb_ack_o	Output	Wishbone acknowledge.
wb_dat_o [31:0]	Output	Wishbone data output.
wb_int_o	Output	Wishbone interrupt signal. Active high.

Table 7: List of IO ports

Packet Receive Interface

This interface is used to transfer received packets to the FPGA/ASIC core logic.

Port	Direction	Description
pkt_rx_ren	Input	Receive Read Enable: This signal should only be asserted when a packet is available in the receive FIFO. When asserted, the 10GE MAC core will begin

Port	Direction	Description
		packet transfer on next cycle. Signal should remain asserted until EOP becomes valid.
pkt_rx_avail	Output	Receive Available: Indicates that a packet is available for reading in receive FIFO.
pkt_rx_data [63:0]	Output	Receive Data: Little-endian format. First byte of packet will appear on pkt_rx_data[7:0].
pkt_rx_eop	Output	Receive End of Packet: Asserted when the last word of a packet is read from receive FIFO.
pkt_rx_val	Output	Receive Valid: Indicates that valid data is present on the bus. This signal is typically asserted one cycle after pkt_rx_ren was asserted unless FIFO underflow occurs.
pkt_rx_sop	Output	Receive Start of Packet: Indicates that the first word of a frame is present on the bus.
pkt_rx_mod [2:0]	Output	Receive Packet Length Modulus: Valid during EOP. Indicates valid bytes during last word: 0: pkt_rx_data[63:0] is valid 1: pkt_rx_data[7:0] is valid 2: pkt_rx_data[15:0] is valid 3: pkt_rx_data[23:0] is valid 4: pkt_rx_data[31:0] is valid 5: pkt_rx_data[39:0] is valid 6: pkt_rx_data[47:0] is valid 7: pkt_rx_data[55:0] is valid
pkt_rx_err	Output	Receive Error: When asserted during a transfer, indicates that current packet is bad and should be discarded by user's logic. This signal is most likely asserted as the result of a CRC error.

Table 8: List of IO ports

Packet Transmit Interface

This interface accepts packets from the FPGA/ASIC core logic.

Port	Direction	Description
pkt_tx_data [63:0]	Input	Transmit Data: Little-endian format. First byte of packet must appear on pkt_rx_data[7:0].
pkt_tx_val	Input	Transmit Valid: This signal must be asserted for each valid data transfer to the 10GE MAC.
pkt_tx_sop	Input	Transmit Start of Packer: This signal must be asserted during the first word of a packet.
pkt_tx_eop	Input	Transmit End of Packet: This line must be asserted during the last word of a packet.
pkt_tx_mod [2:0]	Input	Transmit Packet Length Modulus: Valid during EOP. Indicates valid bytes during last word: 0: pkt_tx_data[63:0] is valid 1: pkt_tx_data[7:0] is valid 2: pkt_tx_data[15:0] is valid 3: pkt_tx_data[23:0] is valid 4: pkt_tx_data[31:0] is valid 5: pkt_tx_data[39:0] is valid 6: pkt_tx_data[47:0] is valid 7: pkt_tx_data[55:0] is valid
pkt_tx_full	Output	Transmit Full: This signal indicates that transmit FIFO is nearing full and transfers should be suspended at the end of the current packet. Transfer of next packet can begin as soon as this signal is de-asserted.

Table 9: List of IO ports

XGMII Receive Interface

This interface accepts data or control character from XAUI/PCS macro. A normal XGMII interface is made of a 32-bit data bus clocked on rising and falling edges of the clock. For simplicity the 10GE MAC uses a 64-bit interface clocked on the rising edge only.

Port	Direction	Description
xgmii_rxc [7:0]	Input	XGMII Receive Control: Each bit corresponds to a byte on the 64-bit interface. When high, indicates that the byte is a control character. When low, indicates that the byte carries data.

Port	Direction	Description
xgmii_rxd [63:0]	Input	XGMII Receive Data: When interfacing with 32-bit devices, xgmii_rxd[31:0] should be mapped to the rising edge of the clock and xgmii_rxd[63:32] should be mapped to the falling edge.

Table 10: List of IO ports

XGMII Transmit Interface

This interface transmits data and control character towards the XAUI/PCS macro. A normal XGMII interface is made of a 32-bit data bus clocked on rising and falling edges of the clock. For simplicity the 10GE MAC uses a 64-bit interface clocked on the rising edge only.

Port	Direction	Description
xgmii_txc [7:0]	Output	XGMII Transmit Control: Each bit corresponds to a byte on the 64-bit interface. When high, indicates that the byte is a control character. When low, indicates that the byte carries data.
xgmii_txd [63:0]	Output	XGMII Transmit Data: When interfacing with 32-bit devices, xgmii_txd[31:0] should be mapped to the rising edge of the clock and xgmii_txd[63:32] should be mapped to the falling edge.

Table 11: List of IO ports

8.

Waveforms

Wishbone Interface

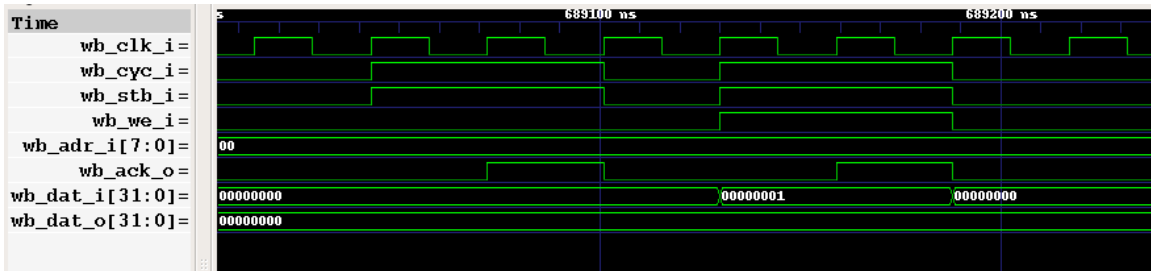


Figure 2: Wishbone Waveforms

Packet Receive Interface

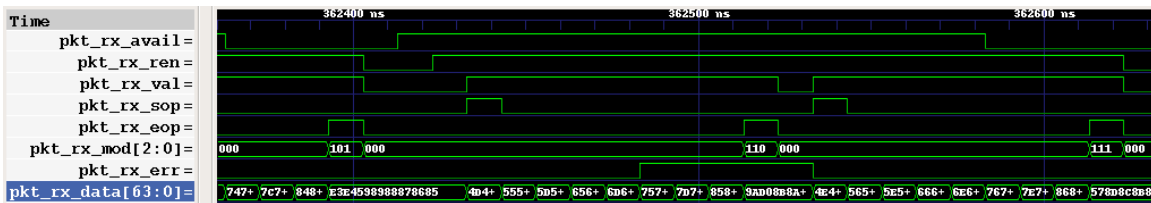


Figure 3: Packet Receive Interface Waveforms

Packet Transmit Interface

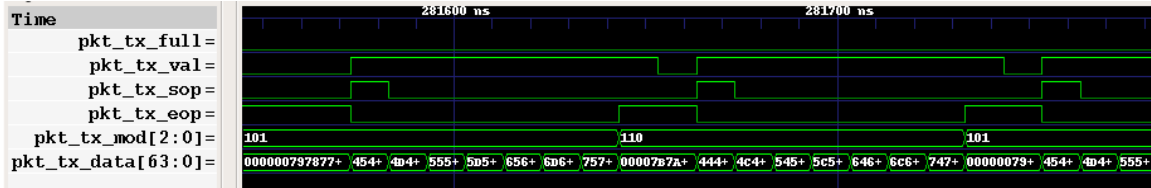


Figure 4: Packet Transmit Interface Waveforms

XGMII Receive Interface

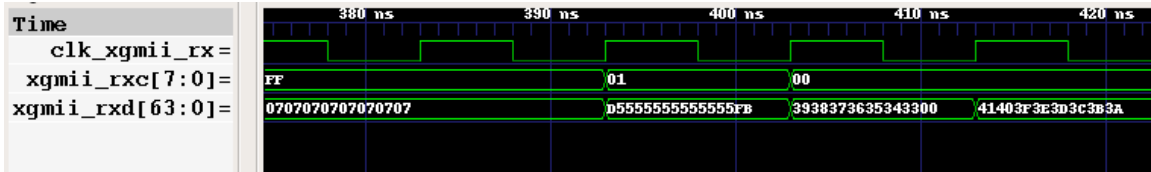


Figure 5: XGMII Receive Interface Waveforms

XGMII Transmit Interface

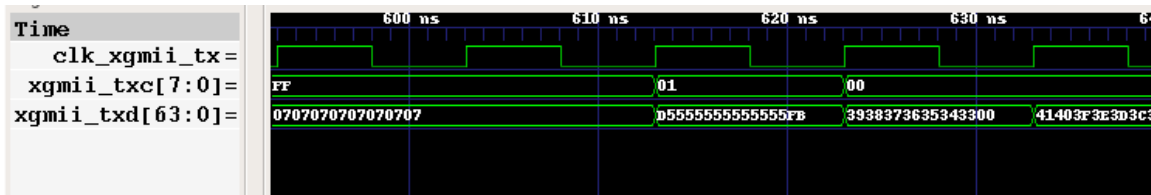


Figure 6: XGMII Transmit Interface Waveforms