Reed-Solomon Decoder IP Core

Unicore Systems Ltd
60-A Saksaganskogo St
Office 1
Kiev 01033
Ukraine
Phone: +38-044-289-87-44
Fax: : +38-044-289-87-44
E-mail: o.uzenkov@unicore.co.ua
URL: www.unicore.co.ua

Applications

- Storage Systems
- Modems
- Set-Top Boxes
- etc

Overview

Reed-Solomon (RS) is an error correcting code that works by oversampling the Galouee's field polynomial constructed from the data to be coded. It is widely used in data storages, communication systems to recover data from possible errors that occur during disc reading or data transmission respectively.

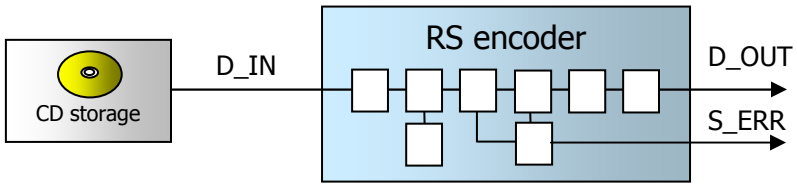

Figure 1: Typical RS decoder utilisation

Key Features

This core implements Reed-Solomon decoder for the 8-bit wide symbols. The core is designed to occupy fewer amounts of logic blocks, be fast and parametrizable.

The main features are:

- 8-bit input and output data busses
- Fully synchronous and pipelined design using a single clock
- Symbol width of 8 bits
- Corrected byte number signaling
- Detects condition when the number of errors is too high to be corrected
- can correct 2 symbols.

Functional Description

Reed-Solomon code is a block code that can be specified as RS(n,k). The parameter n is the size of the whole codeword, k is the number of coded data symbols. n is equal to the sum of k and 2t, where t is the number of symbols which can be corrected. The relationship between the symbol size and the size of the codeword is $n < 2^s$. In the Reed-Solomon decoder IP core the size of the symbol is selected as s = 8 bit, which satisfy the most of data transfer and store standards.

E.g.: RS(255,251) has the codeword size n of 255 symbols; the number of data symbols k of 251 symbols, the maximum of symbol errors that this decoder can correct is equal to t = 2 symbols. The size of each symbol (s) is 8 bits. In this IP core the parameter n is parametrizable one, the symbol error number t is given as 2.

In the Reed-Solomon decoder IP core the Berlekamp's and Chien's algorithms are utilized. The whole algorithm is illustrated by the Fig.2.

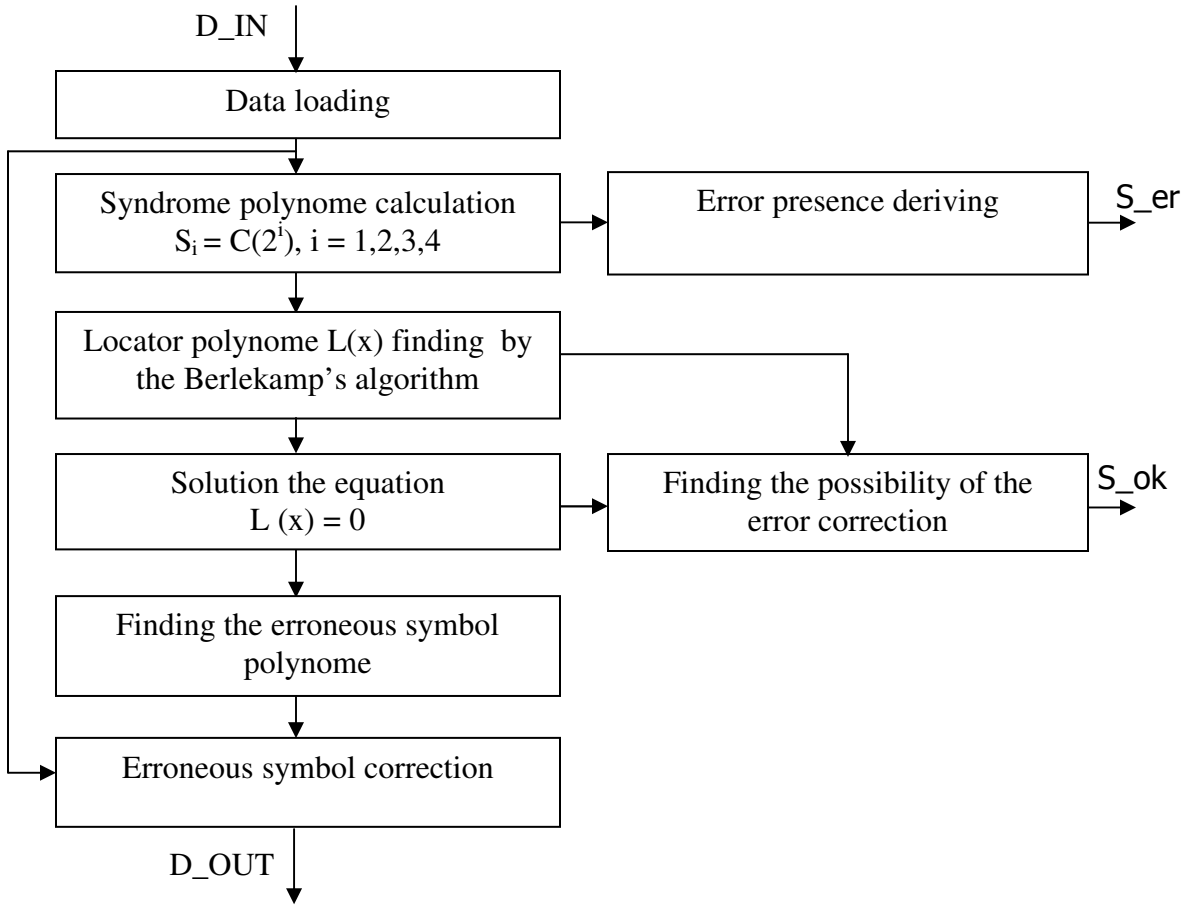

Figure 2: Reed-Solomon decoder algorithm

The Reed-Solomon decoder structure is shown in the Fig.3.

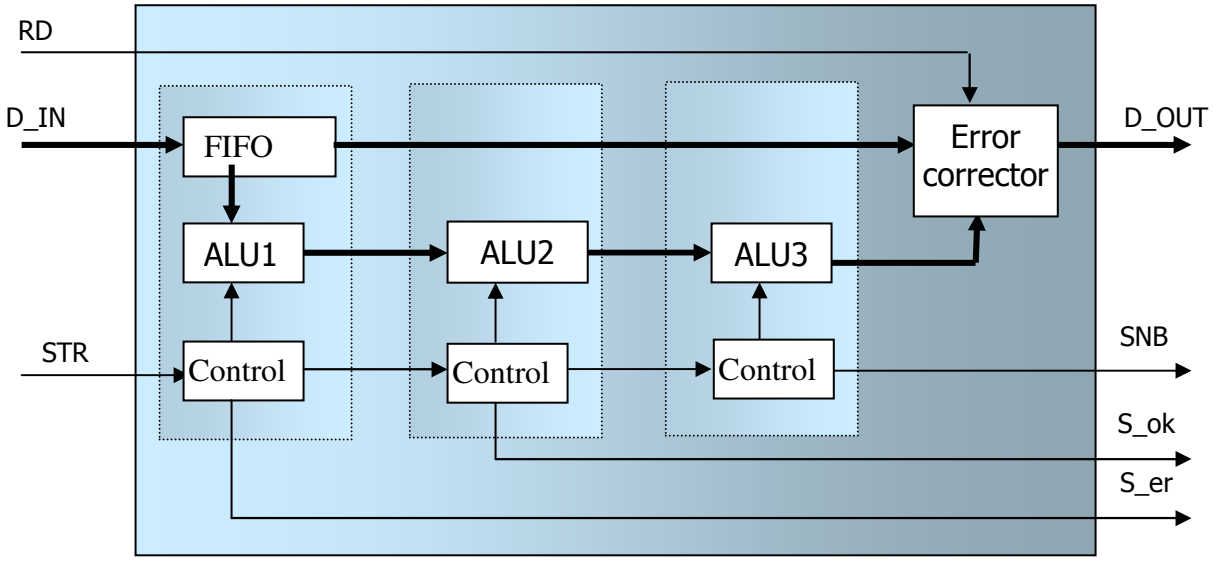

Figure 3: Block Diagram of Reed-Solomon decoder

Here ALU1, ALU2, and ALU3 perform syndrome polynome calculation, locator polynome L(x) finding, and erroneous symbol polynome finding, respectively. Input buffer FIFO loads the input data sequence of the length n and delays it till the period of the error correction.

The decoding process for 255 symbol words lasts 1605 clock cycles, beginning at the data loading, and finishing by the decoded data stream output start. The data loading process can be held in parallel with the decoded data reading.

Core I/O signals

Signal	Signal direction	Description
CLK	in	Clock signal
RST	in	General reset signal
STR	in	Input data start signal
D_IN[7:0]	in	Input data run at each clock impulse
RD	in	Output data read strobe
D_OUT[7:0]	out	Output data go in each clock impulse when RD=1
S_er	out	Is 1 when errors are found
S_ok	out	Is 1 when errors are corrected
SNB	out	Impulse when the decoding is finished

Verification description

The Reed-Solomon decoder has been tested in a testbench suite.

Design Features

- Technology independent
- Corrects up to two 8 bit wide symbols, this number can be increased
- The size of the codeword is selected up to 255, this number can be exchanged dynamically
- Fully Synchronous Design with no Latches
- Highly Modular Design with clearly defined interfaces
- Scan friendly RTL
- Consistent coding procedures

Implementation details

Target device	XC3S400-5	XC3SD1800A-4	XC4VLX15-12	XC5VLX30-3…..
Area, Slices	1527 (42%),	1681(10%)	1521 (24%),	533 (11%),
Area, BRAMs	5 (31%)	5(6%)	5 (10%)	5(16%)
Maximum system clock	80 MHz	80 MHz	165 MHz	210 MHz