OpenRISC development board

Datasheet

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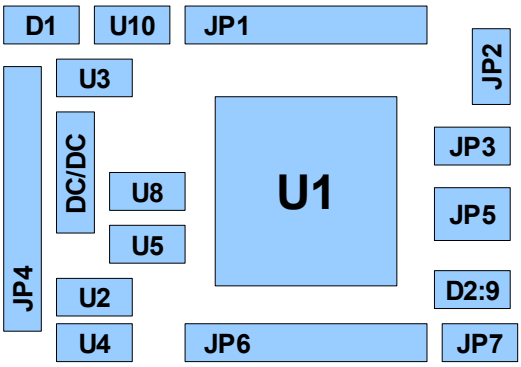
Chapter 1 Development board description

Functional description

The development board has the following functions



U1 - FPGA

The board contains an ACTEL ProASIC3 FPGA in a PQ208 package. The board can optionally be used with other ACTEL FPGA devices from ACTEL A3P or A3PE families.

The following variants are available:

FPGA	System gates	Versa Tiles DFF	RAM kbits	4608 bit blocks	FLASH ROM bits	PLLs	Global nets	I/O banks	IO SE / Diff
A3P1000	1M	24576	144	32	1024	1	18	4	154/35
A3PE1500	1.5M	38400	270	60	1024	6	18	8	147/65
A3PE3000	3M	75264	504	112	1024	6	18	8	147/65

For configuration of the FPGA use JTAG connector JP2.
For configuration use ACTEL FLASH Pro 3 JTAG download cable.

U5, U8, JP5 - Memory

The board has 32 Mbyte of SDRAM and a 1 Mbit SPI FLASH device.
There is also a SD connector, JP5, for high density FLASH cards.

The SDRAM is a Micron SDR SDRAM memory, MC48LC16M16-7E.

The memory has the following address table:

	Configuration	Refresh count	Row addressing	Bank addressing	Column addressing
16 Meg x 16	4 Meg x 16 x 4 banks	8K	8K (A0-A12)	4 (BA0, BA1)	512 (A0-A8)

The board has a M25P10 serial FLASH memory. The memory is organized as 4 sectors, each containing 128 pages. Each page is 256 bytes wide. Thus, the whole memory can be viewed as consisting of 512 pages, or 131,072 bytes.

The whole memory can be erased using the Bulk Erase instruction, or a sector at a time, using the Sector Erase instruction.

The FLASH PROM uses SPI communication. Input data is latched in on the rising edge of Serial Clock (C), and output data is available from the falling edge of Serial Clock (C).

In addition there is also a SD FLASH card connector on the bottom side of the board. This connector can be used for high capacity FLASH cards for mass storage.

JP1, JP6, JP7 - IO

There are two 2x20 pin 2 mm pitch headers for external connections. Each connector can be configured for any IO supply voltage.

A 10 pin 0.1" pitch header can be used for low density IO over a 10 pin flat cable.

JP3 - SoC debug

The OpenRISC processor has hardware support for JTAG debugging. On this board there is also a LVTTL serial port used as console. Both are connected to the debug connector. A JTAG debug cable with two independent channels can be used for both JTAG debug and a console.

This JTAG debug cable is available from ORSoC.

On board is also 8 LEDs that can be used for debugging purposes.

U2, U3, U4 - Oscillators

The board has three separate oscillators;

1. SDRAM and SoC , 25 MHz
2. Ethernet SMII channels @ 125 MHz.
   The SMII clock has a clock driver supporting up to 4 SMII channels
3. audio or general purpose

Only the first oscillator is mounted. Depending on needs the other two can optionally be mounted.

The first oscillator is connected to both the SDRAM CLK pin and a clock input on the FPGA. The SDRAM will run at the oscillator clock speed. The internal SoC could be running on any multiple of this clock through the PLL.

Second clock is intended for multiple Ethernet SMII channels. The board support up to four channels. This oscillator connects through a zero delay buffer to both the FPGA and to JP1. On A3PE equipped board this clock can use the PLL inside the FPGA.

Third clock could be used for VGA, audio or USB.

DC/DC converter

The board requires a single 3.3 volt supply if a local 1.5V DC/DC converter is mounted as a module. A linear converter sources the PLLs in the FPGA. All supply is available in JP4.

If a local 1.5V converter is not present this supply must be connected to JP4.

Chapter 2 Connectors

JP4 - Supply

When used as a daughter board supply should be applied to JP4. JP4 is a 2 mm pitch 10 pin header.

JP4		
1, 2, 3, 4	GND	
5, 6	3.3V	Supply
7, 8	1.5V ACTEL core	Supply
9, 10	1.5V ACTEL PLL supply	Sourced from local linear regulator

JP2 – JTAG configuration

Connect to ACTEL FLASH Pro3 for FPGA configuration.

JP2			FPGA
1	TCK		
3	TDO		108
4	NC		
5	TMS		103
6	3.3V	Supply	
7	Vpump	If R2 is mounted connected to 3.3V	106
8	TRST		109
9	TDI		102
2, 10	GND	Supply	

JP3 – JTAG debug

Connect to ORSoC USB JTAG debug cable.

JP2			FPGA
1	TCK		98
3	TDO	Output on FPGA	94
4	NC		
5	TMS		93
6	3.3V	Supply	
7	RX		92
8	TX		91
9	TDI		95
2, 10	GND		

JP1 – GPIO

JP1			FPGA
1	CLK2	Sourced from U10	
2	CLK1	Sourced from U10	
3	CLK3	Sourced from U10	
4	CLK4	Sourced from U10	
5	IO4		149
6	IO5		148
7	IO6		147
8	IO7		146
9	IO8		145
10	IO9		144
11	IO10		143
12	IO11		139
14	IO13		138
16	IO15		137
17	IO16		136
18	IO17		134
19	IO18		132
20	IO19		129
22	IO21		128
24	IO23		125
25	IO26		120
26	IO25		121
27	IO28		118
28	IO27		119
29	IO30		116
30	IO29		117
31	IO32		114
32	IO31		115
33	IO34		112
34	IO33		113
13, 23, 35, 37, 38	GND		
15, 21, 36, 39, 40	VIOB		111, 123, 140, 154

JP6 – GPIO

JP6			FPGA
1	IO0		205
2	IO1		204
3	IO2		4
4	IO3		5
5	IO4		6
6	IO5		7
7	IO6		8
8	IO7		9
9	IO8		10
10	IO9		11
11	IO10		12
12	IO11		13
13	IO12		14
14	IO13		15
17	IO16		21
18	IO17		22
19	IO18		23
20	IO19		24
21	IO20		26
22	IO21		28
24	IO23		31
25	IO24		32
26	IO25		33
27	IO26		34
28	IO27		35
29	IO28		37
30	IO29		38
31	IO30		39
32	IO31		42
33	IO32		43
34	IO33		44
35	IO34		45
36	IO35		46
15, 23, 37, 38	GND		
16, 39, 40	VIOB		3, 18, 40, 50

JP7 – GPIO

Intended use as serial IO, for example two SPI channels. Use pin 4 & 8 as clocks.

JP7			FPGA
1	IOB0		55
2	IOB1		63
3	IOB2		64
4	IOB3	Serial resistor 27R	66
5	IOB4		67
6	IOB5		68
7	IOB6		69
8	IOB7	Serial resistor 27R	70
9	IOB8		73
2, 10	GND		

JP5 – SD FLASH Card connector

Use this connector for SD FLASH Card, MMC or SDIO.

JP7			FPGA
1	CS		60
2	DI		59
3	GND		
4	3.3V		
5	SCLK		57
6	GND		
7	DO		58

Chapter 3 On board connections

LED

There are 8 LED indicators primarily for debug purposes. LEDs anode connected to 3.3V. Turn FPGA output low to turn on the light.

LED1	LED2	LED3	LED4	LED5	LED6	LED7	LED8
74	75	76	77	78	79	80	82

SPI FLASH memory

On board 1 Mbit 25MP10 SPI FLASH memory, U5.

D	C	Q	S	W	HOLD
87	90	85	84	83	86

SDRAM

On board 32 Mbyte SDR SDRAM memory, U8.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
159	161	164	166	168	172	174	176	175	173	169	167	165	163	160	152
			A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
			185	189	192	191	193	196	198	201	203	202	199	197	194
					DQMH	DQML		RAS		CAS		WE		CKE	
					180	177		182		181		179		183	

System signals

On the board there are three clock sources and one reset signal.

The reset signal is generated at startup from reset generator and can be asserted manually by pressing reset switch on the board

Source	Comment	Target
U4.CLK	Serie resistor 27R Connected to PLL	FPGA - U1.30 SDRAM - U8.28
U3.CLK 125MHz	Distrubuted to JP1 and FPGA with zero buffer delay	FPGA – U1.151
U2.CLK		FPGA – U1.206
RESET	U9 or SW1	FPGA – U1.49

Recommended Resources

ORSoC – http://www.orsoc.se

ORSoC is a fabless ASIC design & manufacturing services company, providing RTL to ASIC design services and silicon fabrication service. **ORSoC** are specialists building complex system based on the OpenRISC processor platform.

Open Source IP – http://www.opencores.org

Your number one source for open source IP and other FPGA/ASIC related information.