OpenRISC Ethernet development board

A board to be used in comapanion with an OpenRISC development board to get Ethernet, audio and other functions.

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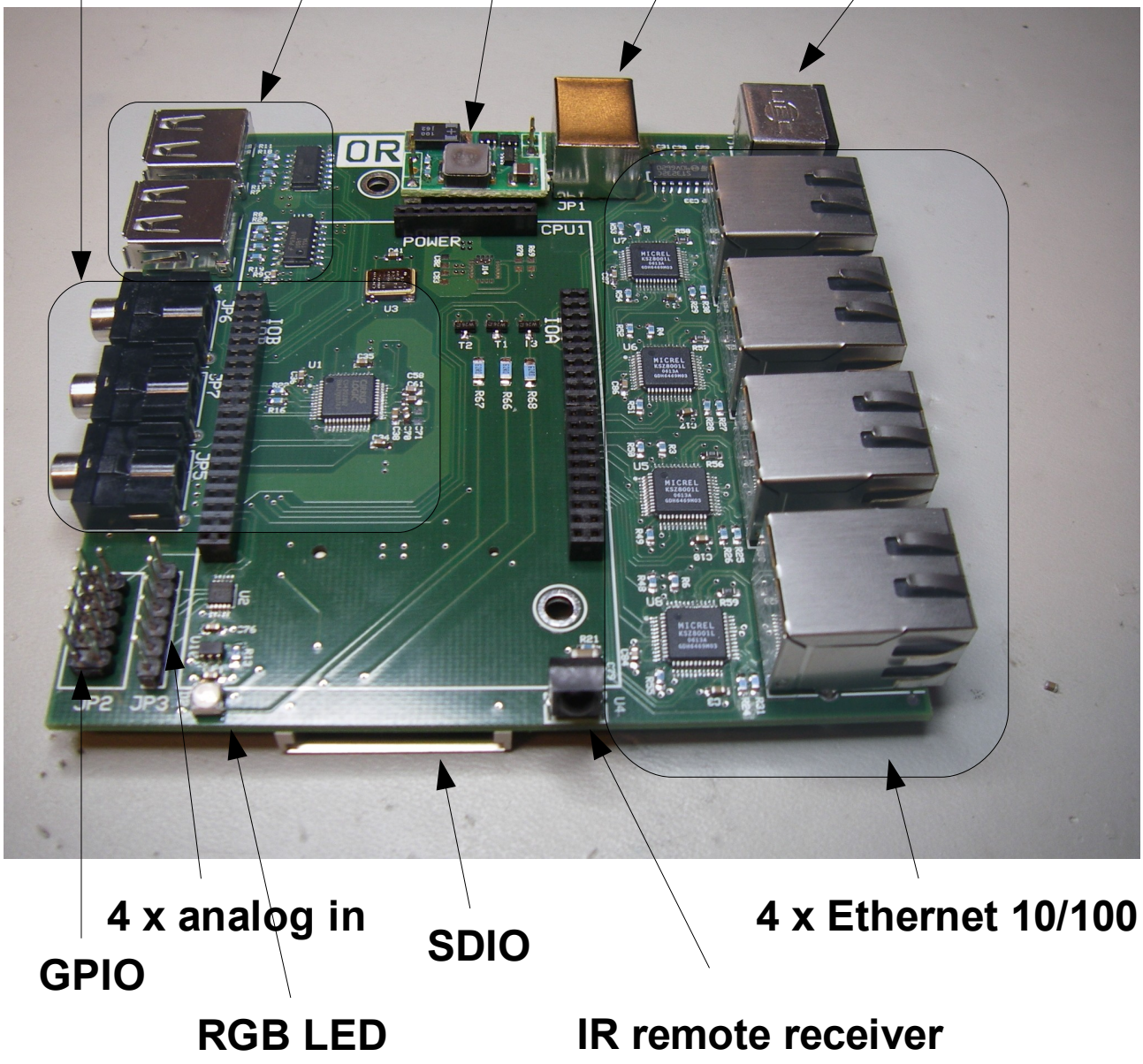
Table of Contents

Chapter 1 Ethernet development board description



On board functions:

1. four Fast Ethernet ports
2. GPS connector
3. two USB 1.1 host connectors
4. AC´97 with mic in, line in and line out
5. 4 analog inputs, 8 digital IO and SD FLASH / SDIO connector
6. RC5 compatible IR receiver
7. RGB LED

Chapter 2 Detailed function description

Fast Ethernet

The board has four independent fast Ethernet channels. Each channel is based on a Ethernet PHY from Micrel, KS8001L. The devices is configured for SMII towards FPGA board.

Each channel has RJ45 connectors with integrated magnetics and LED indicators

GPS connector

A connector for an external GPS receiver adds a convenient way to attach a high accuracy time reference.

Possible usage with GlobalSat MR-350.

USB 1.1 host

The board has two independent USB 1.1 compatible host channels. Each channels uses a USB1T11 transceiver from Fairchild.

AC'97 audio

The board has an audio solution based on a AC'97 compatible codec from Cirrus Logic, CS4202.

The following functions are available on connectors

1. mic in, 3.5 mm jack
2. line in, 3.5 mm jack
3. line out, 3.5 mm jack
4. External Amplifier Power Down, header

RC5 compatible IR receiver

There is a IR receiver with a built-in 38 kHz filter to be used as a RC compatible receiver.

RGB high intensity LED

A high intensity RGB LED can be used as a general purpose LED solution.

Analog inputs

A four channel analog to digital converter with SPI interface is connected to JP3. Pin 5 of JP3 is connected to 5V to enable direct attach of a user specific analog front end board.

The analog converter is a ADC124 from National Semiconductor. The digital interface is SPI compatible.

Pin no.	Symbol	Description
4-7	IN1 to IN4	Analog inputs. These signals can range from 0v to 3.3V
10	SCLK	Digital clock input. This clock directly controls the the conversion and readout processes.
9	DOUT	Digital data output. The output samples are clocked out of this pin on falling edges of the SCLK pin.
8	DIN	Digital data input. The control register is loaded through this pin on the rising edge of the SCLK pin.
1	CSn	Chip select. On the falling edge of CSn a conversion process

		begins. Conversion continues as long as CSn is held low.

SD FLASH / SDIO connector

On the bottom of the card there is a SD FLASH connector to be used with either SD FLASH card or with SDIO modules.

General purpose digital IO

Connector JP2 has seven general purpose digital IO together with 3.3V and 5V supply.

Supply

The board is powered over a USB type B connector, JP1. Connect to a computer host port, power USB Hub or other 5V supply.

Local DC/DC converters for 3.3V and 1.5V based on EP5382 from Enpirion supply the board.

Chapter 3 Connector pinout

Connector table

	Function	Connector type
JP1	5V power supply	USB type B connector
JP2	8 LVTTL digital IO	5x2 pin header 0.1”
Jp3	4 analog input	6x1 pin header 0.1”
JP4	AC'97, External Amplifier Power Down	2x1 pin header 0.1”
JP5	AC'97 microphone input	3.5 mm
JP6	AC'97 Line out	3.5 mm
JP7	AC'97 Line in	3.5 mm
JP8	USB 1.1 Host A	USB type A
JP9	USB 1.1 Host B	USB type A
JP10	GPS connector	DIN 6 pole
JP11	Ethernet 10/100, channel C	RJ45
JP12	Ethernet 10/100, channel B	RJ45
JP13	Ethernet 10/100, channel A	RJ45
JP14	Ethernet 10/100, channel D	RJ45

JP2 general purpose digital IO

JP2	Symbol	Description
1	5V	5V supply
2	3.3V	3.3V supply
3	GPIO6	
4	GPIO5	
5	GPIO4	
6	GPIO3	
7	GPIO2	
8	GPIO1	
9	GPIO0	
10	GND	Ground

JP3 analog inputs

JP3	Symbol	Description
1	5V	5V supply
2	AIN1	U2.7
3	AIN2	U2.6
4	AIN3	U2.5

5	AIN4	U2.4
6	GND	Ground

JP10 UART / GPS connector

JP10 can be used as a serial port for general purpose use or for a GPS receiver.

JP10	Symbol	Description
1	GND	Ground
2	VCC	5V supply
3	PPS	Pulse Per Second
4	RX	Receive
5	TX	Transmit
6	NC	

Chapter 4 On board interconnect

USB Host connectors

USB Host channel A

	Function	Local connection	ACTEL FPGA
IOB.1	OE	U12.2	205
IOB.2	SPD	U12.9	204
IOB.3	RX_VP	U12.4	4
IOB.4	RX_VM	U12.5	5
IOB.5	TX_VPO	U12.12	6
IOB.6	TX_VMO	U12.13	7

USB Host channel B

	Function	Local connection	ACTEL FPGA
IOB.7	OE	U13.2	8
IOB.8	SPD	U13.9	9
IOB.9	RX_VP	U13.4	10
IOB.10	RX_VM	U13.5	11
IOB.11	TX_VPO	U13.12	12
IOB.12	TX_VMO	U13.13	13

AC'97 audio codec

	Function	Local connection	ACTEL FPGA
IOB.13	SDATA_IN	U1.8, series resistor 27R	14
IOB.14	SDATA_OUT	U1.5	15
IOB.17	BIT_CLK	U1.6, series resistor 27R	21
IOB.18	SYNC	U1.10	22
IOB.19	RESET	U1.11	23

Analog inputs

	Function	Local connection	ACTEL FPGA
IOB.33	DOUT	U2.9	43
IOB.34	DIN	U2.8	44
IOB.35	SCLK	U2.10	45
IOB.36	CSn	U2.1	46

Digital general purpose IO

Note that JP2 and the SD/SDIO connector share the same signals. This means that you can

use either JP2 OR JP15 at the same time.

	Function	Local connection	ACTEL FPGA
IOB.25	GPIO0 / CD	JP2.9 / JP15.10	32
IOB.26	GPIO1 / DAT1	JP2.8 / JP15.8	33
IOB.27	GPIO2 / DO / DAT0	JP2.7 / JP15.7	34
IOB.28	GPIO3 / SCLK /CLK	JP2.6 / JP15.5	35
IOB.29	GPIO4 / DI / CMD	JP2.5 / JP15.2	37
IOB.30	GPIO5 / CS / DAT3	JP2.4 / JP15.1	38
IOB.31	GPIO6 / DAT2	JP2.3 / JP15.9	39

IR receiver

	Function	Local connection	ACTEL FPGA
IOB.32	RC5	U4.1	42

RGB LED

	Function	Local connection	ACTEL FPGA
IOB.20	R	D2.R	24
IOB.21	G	D2.G	26
IOB.22	B	D2.B	28

UART / GPS

	Function	Local connection	ACTEL FPGA
IOA.5	PPS	U11.9	149
IOA.6	RX	U11.11	148
IOA.7	TX	U11.12	147

Ethernet 10 /100

Channel A

	Function	Local connection	ACTEL FPGA
IOA.10	RX	U7.6	144
IOA.11	TX	U7.17	143
IOA.12	SYNC	U7.18	139
IOA.8	MDIO	U7.1	146
IOA.9	MDC	U7.2	145
IOA.14	MDINT	U7.25	138

Channel B

	Function	Local connection	ACTEL FPGA
IOA.18	RX	U6.6	134
IOA.19	TX	U6.17	132
IOA.20	SYNC	U6.18	129
IOA.16	MDIO	U6.1	137
IOA.17	MDC	U6.2	136
IOA.22	MDINT	U6.25	128

Channel C

	Function	Local connection	ACTEL FPGA
IOA.26	RX	U5.6	121
IOA.27	TX	U5.17	118
IOA.28	SYNC	U5.18	119
IOA.24	MDIO	U5.1	125
IOA.25	MDC	U5.2	120
IOA.29	MDINT	U5.25	116

Channel D

	Function	Local connection	ACTEL FPGA
IOA.32	RX	U8.6	115
IOA.33	TX	U8.17	112
IOA.34	SYNC	U8.18	113
IOA.30	MDIO	U8.1	117
IOA.31	MDC	U8.2	114

Common Ethernet signals

	Function	Local connection	ACTEL FPGA
IOA.1	CLK125A	U7.15	
IOA.2	CLK125B	U6.15	
IOA.3	CLK125C	U5.15	
IOA.4	CLK125D	U8.15	
IOB.24	RESETn	U7.48 U6.48 U5.48 U8.48	31

Recommended Resources

ORSoC – http://www.orsoc.se

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