Release 6.2i - xst G.28

--> Parameter TMPDIR set to __projnav
CPU : 0.00 / 2.92 s | Elapsed : 0.00 / 2.00 s

--> Parameter xsthdpdir set to ./xst
CPU : 0.00 / 2.92 s | Elapsed : 0.00 / 2.00 s

--> Reading design: encryptor.prj

TABLE OF CONTENTS

==========
*   Synthesis Options Summary   *
==========
---- Source Parameters
Input File Name   : encryptor.prj
Input Format   : mixed
Ignore Synthesis Constraint File   : NO
Verilog Include Directory   :

---- Target Parameters
Output File Name   : encryptor
Output Format   : NGC
Target Device   : xc3s400-5-pq208

---- Source Options
Top Module Name   : encryptor
Automatic FSM Extraction   : YES
FSM Encoding Algorithm   : Auto
FSM Style   : lut
RAM Extraction   : Yes
RAM Style   : Auto

ROM Extraction : Yes
ROM Style : Auto
Mux Extraction : YES
Mux Style : Auto
Decoder Extraction : YES
Priority Encoder Extraction : YES
Shift Register Extraction : YES
Logical Shifter Extraction : YES
XOR Collapsing : YES
Resource Sharing : YES
Multiplier Style : auto
Automatic Register Balancing : No

---- Target Options
Add IO Buffers : YES
Global Maximum Fanout : 500
Add Generic Clock Buffer(BUFG) : 8
Register Duplication : YES
Equivalent register Removal : YES
Slice Packing : YES
Pack IO Registers into IOBs : auto

---- General Options
Optimization Goal : Speed
Optimization Effort : 1
Keep Hierarchy : NO
Global Optimization : AllClockNets
RTL Output : Yes
Write Timing Constraints : NO
Hierarchy Separator : _
Bus Delimiter : <>
Case Specifier : maintain
Slice Utilization Ratio : 100
Slice Utilization Ratio Delta : 5

---- Other Options
lso : encryptor.lso
Read Cores : YES
cross_clock_analysis : NO
verilog2001 : YES
Optimize Instantiated Primitives : NO

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```
=========================================================================
*                     HDL Compilation                     *
=========================================================================
Compiling vhdl file g:/en1/../project/Encryptor_Design1/full_adder.vhd in Library work.
Architecture behavioral of Entity full_adder is up to date.
Compiling vhdl file g:/en1/../project/Encryptor_Design1/carrysave_adder.vhd in Library
work.
Architecture behavioral of Entity carrysave_adder is up to date.
Compiling vhdl file g:/en1/../project/Encryptor_Design1/carrylook_ahead2.vhd in
Library work.
Architecture behavioral of Entity carrylook_ahead2 is up to date.
Compiling vhdl file g:/en1/../project/Encryptor_Design1/wallace_structure.vhd in Library
work.
Architecture behavioral of Entity wallace_structure is up to date.
Compiling vhdl file g:/en1/../project/Encryptor_Design1/multiplier.vhd in Library work.
Architecture behavioral of Entity multiplier is up to date.
Compiling vhdl file g:/en1/en1.vhdl in Library work.
Architecture arch_encryptor of Entity encryptor is up to date.

=========================================================================
*                     HDL Analysis                        *
=========================================================================
Analyzing Entity <encryptor> (Architecture <arch_encryptor>).
WARNING:Xst:1610 - g:/en1/en1.vhdl line 303: Width mismatch. <A_temp2> has a
width of 16 bits but assigned expression is 31-bit wide.
WARNING:Xst:1610 - g:/en1/en1.vhdl line 306: Width mismatch. <C_temp2> has a
width of 16 bits but assigned expression is 31-bit wide.
INFO:Xst:1304 - Contents of register <last_round> in unit <encryptor> never changes
during circuit operation. The register is replaced by logic.
Entity <encryptor> analyzed. Unit <encryptor> generated.

Analyzing Entity <multiplier> (Architecture <behavioral>).
Entity <multiplier> analyzed. Unit <multiplier> generated.

Analyzing Entity <wallace_structure> (Architecture <behavioral>).
Entity <wallace_structure> analyzed. Unit <wallace_structure> generated.

Analyzing Entity <carrysave_adder> (Architecture <behavioral>).
Entity <carrysave_adder> analyzed. Unit <carrysave_adder> generated.

Analyzing Entity <full_adder> (Architecture <behavioral>).
Entity <full_adder> analyzed. Unit <full_adder> generated.
```

```
Analyzing Entity <carrylook_ahead2> (Architecture <behavioral>).
Entity <carrylook_ahead2> analyzed. Unit <carrylook_ahead2> generated.


=========================================================================
*                     HDL Synthesis                       *
=========================================================================
INFO:Xst:1304 - Contents of register <cleanup_A> in unit <encryptor> never changes
during circuit operation. The register is replaced by logic.
INFO:Xst:1304 - Contents of register <cleanup_C> in unit <encryptor> never changes
during circuit operation. The register is replaced by logic.

Synthesizing Unit <full_adder>.
   Related source file is g:/en1/../project/Encryptor_Design1/full_adder.vhd.
WARNING:Xst:646 - Signal <sig<15>> is assigned but never used.
   Found 16-bit xor3 for signal <sf>.
   Summary:
        inferred  16 Xor(s).
Unit <full_adder> synthesized.


Synthesizing Unit <carrylook_ahead2>.
   Related source file is g:/en1/../project/Encryptor_Design1/carrylook_ahead2.vhd.
WARNING:Xst:646 - Signal <c<16>> is assigned but never used.
   Found 15-bit xor2 for signal <s1<15:1>>.
   Found 16-bit xor2 for signal <p>.
Unit <carrylook_ahead2> synthesized.


Synthesizing Unit <carrysave_adder>.
   Related source file is g:/en1/../project/Encryptor_Design1/carrysave_adder.vhd.
Unit <carrysave_adder> synthesized.


Synthesizing Unit <wallace_structure>.
   Related source file is g:/en1/../project/Encryptor_Design1/wallace_structure.vhd.
WARNING:Xst:1780 - Signal <c_out> is never used or assigned.
Unit <wallace_structure> synthesized.


Synthesizing Unit <multiplier>.
   Related source file is g:/en1/../project/Encryptor_Design1/multiplier.vhd.
Unit <multiplier> synthesized.
```

```
Synthesizing Unit <encryptor>.
    Related source file is g:/en1/en1.vhdl.
WARNING:Xst:646 - Signal <ttemp1<15:4>> is assigned but never used.
WARNING:Xst:646 - Signal <utemp1<15:4>> is assigned but never used.
    Found finite state machine <FSM_0> for signal <state>.
    -----------------------------------------------------------------------
    | States             | 12                                             |
    | Transitions        | 14                                             |
    | Inputs             | 2                                              |
    | Outputs            | 11                                             |
    | Clock              | clock (rising_edge)                            |
    | Reset              | reset (positive)                               |
    | Reset type         | asynchronous                                   |
    | Reset State        | 000000000001                                   |
    | Encoding           | automatic                                      |
    | Implementation     | LUT                                            |
    -----------------------------------------------------------------------
    Found finite state machine <FSM_1> for signal <state_out>.
    -----------------------------------------------------------------------
    | States             | 5                                              |
    | Transitions        | 6                                              |
    | Inputs             | 1                                              |
    | Outputs            | 5                                              |
    | Clock              | clock (rising_edge)                            |
    | Reset              | reset (positive)                               |
    | Reset type         | asynchronous                                   |
    | Reset State        | 00001                                          |
    | Encoding           | automatic                                      |
    | Implementation     | LUT                                            |
    -----------------------------------------------------------------------
WARNING:Xst:737 - Found 16-bit latch for signal <ciphertext>.
    Found 1-bit register for signal <ready_e>.
    Found 16-bit 16-to-1 multiplexer for signal <$n0003> created at line 303.
    Found 16-bit 16-to-1 multiplexer for signal <$n0005> created at line 306.
    Found 8-bit comparator less for signal <$n0013> created at line 340.
    Found 16-bit xor2 for signal <$n0031> created at line 291.
    Found 16-bit xor2 for signal <$n0032> created at line 290.
    Found 16-bit adder for signal <$n0038> created at line 372.
    Found 16-bit adder for signal <$n0039> created at line 382.
    Found 16-bit adder for signal <$n0040> created at line 181.
    Found 16-bit adder for signal <$n0041> created at line 183.
    Found 16-bit adder for signal <$n0074>.
    Found 16-bit adder for signal <$n0075>.
    Found 16-bit adder for signal <$n0076>.
```

Found 16-bit adder for signal <$n0077>.
Found 16-bit adder for signal <$n0078>.
Found 16-bit adder for signal <$n0079>.
Found 16-bit adder for signal <$n0080>.
Found 16-bit adder for signal <$n0081>.
Found 16-bit adder for signal <$n0082>.
Found 16-bit adder for signal <$n0083>.
Found 16-bit adder for signal <$n0084>.
Found 16-bit adder for signal <$n0085>.
Found 16-bit adder for signal <$n0086>.
Found 16-bit adder for signal <$n0087>.
Found 16-bit adder for signal <$n0088>.
Found 16-bit adder for signal <$n0089>.
Found 16-bit adder for signal <$n0090>.
Found 16-bit adder for signal <$n0091>.
Found 16-bit adder for signal <$n0092>.
Found 16-bit adder for signal <$n0093>.
Found 16-bit adder for signal <$n0094>.
Found 16-bit adder for signal <$n0095>.
Found 16-bit adder for signal <$n0096>.
Found 16-bit adder for signal <$n0097>.
Found 16-bit adder for signal <$n0098>.
Found 16-bit adder for signal <$n0099>.
Found 16-bit adder for signal <$n0100>.
Found 16-bit adder for signal <$n0101>.
Found 16-bit adder for signal <$n0102>.
Found 16-bit adder for signal <$n0103>.
Found 16-bit adder for signal <$n0104>.
Found 16-bit adder for signal <$n0105>.
Found 16-bit adder for signal <$n0106>.
Found 16-bit adder for signal <$n0107>.
Found 16-bit adder for signal <$n0108>.
Found 16-bit adder for signal <$n0109>.
Found 16-bit adder for signal <$n0110>.
Found 16-bit adder for signal <$n0111>.
Found 16-bit adder for signal <$n0112>.
Found 16-bit adder for signal <$n0113>.
Found 7-bit adder for signal <$n0144> created at line 341.
Found 16-bit adder for signal <$n0145> created at line 311.
Found 16-bit adder for signal <$n0146> created at line 246.
Found 16-bit adder for signal <$n0147> created at line 312.
Found 16-bit adder for signal <$n0148> created at line 261.
Found 16-bit register for signal <A>.
Found 16-bit register for signal <A_final>.
Found 16-bit register for signal <A_temp1>.
Found 16-bit register for signal <B>.

```
    Found 16-bit register for signal <B_final>.
    Found 16-bit register for signal <C>.
    Found 16-bit register for signal <C_final>.
    Found 16-bit register for signal <C_temp1>.
    Found 7-bit register for signal <cnt>.
    Found 16-bit register for signal <D>.
    Found 16-bit register for signal <D_final>.
    Found 16-bit adder for signal <l<40:35>>.
    Found 16-bit adder for signal <l<33:25>>.
    Found 16-bit adder for signal <l<23:0>>.
    Found 16-bit adder for signal <s<43:1>>.
    Found 1-bit register for signal <start_d1>.
    Found 16-bit register for signal <ttemp1>.
    Found 16-bit register for signal <utemp1>.
    Summary:
        inferred   2 Finite State Machine(s).
        inferred 201 D-type flip-flop(s).
        inferred 131 Adder/Subtracter(s).
        inferred   1 Comparator(s).
        inferred  32 Multiplexer(s).
Unit <encryptor> synthesized.


=========================================================================
*                  Advanced HDL Synthesis                  *
=========================================================================

Advanced RAM inference ...
Advanced multiplier inference ...
Selecting encoding for FSM_1 ...
Optimizing FSM <FSM_1> on signal <state_out> with one-hot encoding.
Selecting encoding for FSM_0 ...
Optimizing FSM <FSM_0> on signal <state> with one-hot encoding.
Dynamic shift register inference ...

=========================================================================
HDL Synthesis Report

Macro Statistics
# FSMs                      : 2
# Adders/Subtractors        : 131
 7-bit adder                : 1
 16-bit adder               : 130
```

```
# Registers                      : 32
 1-bit register                 : 19
 16-bit register                : 12
 7-bit register                 : 1
# Latches                        : 1
 16-bit latch                   : 1
# Comparators                    : 1
 8-bit comparator less          : 1
# Multiplexers                   : 2
 16-bit 16-to-1 multiplexer     : 2
# Xors                          : 78
 16-bit xor3                    : 14
 16-bit xor2                    : 2
 1-bit xor2                     : 62

=========================================================================

=========================================================================
*                     Low Level Synthesis                               *
=========================================================================
WARNING:Xst:1426 - The value init of the FF/Latch start_d1 hinder the constant
cleaning in the block encryptor.
   You should achieve better results by setting this init to 1.
WARNING:Xst:1291 - FF/Latch <utemp1_15> is unconnected in block <encryptor>.
WARNING:Xst:1291 - FF/Latch <ttemp1_15> is unconnected in block <encryptor>.
WARNING:Xst:1291 - FF/Latch <utemp1_4> is unconnected in block <encryptor>.
WARNING:Xst:1291 - FF/Latch <utemp1_5> is unconnected in block <encryptor>.
WARNING:Xst:1291 - FF/Latch <utemp1_6> is unconnected in block <encryptor>.
WARNING:Xst:1291 - FF/Latch <utemp1_7> is unconnected in block <encryptor>.
WARNING:Xst:1291 - FF/Latch <utemp1_8> is unconnected in block <encryptor>.
WARNING:Xst:1291 - FF/Latch <utemp1_9> is unconnected in block <encryptor>.
WARNING:Xst:1291 - FF/Latch <utemp1_10> is unconnected in block <encryptor>.
WARNING:Xst:1291 - FF/Latch <utemp1_11> is unconnected in block <encryptor>.
WARNING:Xst:1291 - FF/Latch <utemp1_12> is unconnected in block <encryptor>.
WARNING:Xst:1291 - FF/Latch <utemp1_13> is unconnected in block <encryptor>.
WARNING:Xst:1291 - FF/Latch <utemp1_14> is unconnected in block <encryptor>.
WARNING:Xst:1291 - FF/Latch <ttemp1_4> is unconnected in block <encryptor>.
WARNING:Xst:1291 - FF/Latch <ttemp1_5> is unconnected in block <encryptor>.
WARNING:Xst:1291 - FF/Latch <ttemp1_6> is unconnected in block <encryptor>.
WARNING:Xst:1291 - FF/Latch <ttemp1_7> is unconnected in block <encryptor>.
WARNING:Xst:1291 - FF/Latch <ttemp1_8> is unconnected in block <encryptor>.
WARNING:Xst:1291 - FF/Latch <ttemp1_9> is unconnected in block <encryptor>.
WARNING:Xst:1291 - FF/Latch <ttemp1_10> is unconnected in block <encryptor>.
```

WARNING:Xst:1291 - FF/Latch <ttemp1_11> is unconnected in block <encryptor>.
WARNING:Xst:1291 - FF/Latch <ttemp1_12> is unconnected in block <encryptor>.
WARNING:Xst:1291 - FF/Latch <ttemp1_13> is unconnected in block <encryptor>.
WARNING:Xst:1291 - FF/Latch <ttemp1_14> is unconnected in block <encryptor>.

Optimizing unit <encryptor> ...

Optimizing unit <carrylook_ahead2> ...

Optimizing unit <full_adder> ...

Optimizing unit <multiplier> ...
Loading device for application Xst from file '3s400.nph' in environment C:/Xilinx.

Mapping all equations...
Building and optimizing final netlist ...
Found area constraint ratio of 100 (+ 5) on block encryptor, actual ratio is 47.
FlipFlop B_6 has been replicated 1 time(s)
FlipFlop B_1 has been replicated 1 time(s)
FlipFlop B_3 has been replicated 1 time(s)
FlipFlop B_2 has been replicated 1 time(s)
FlipFlop B_5 has been replicated 1 time(s)
FlipFlop B_0 has been replicated 1 time(s)
FlipFlop B_4 has been replicated 1 time(s)
FlipFlop D_3 has been replicated 1 time(s)
FlipFlop B_1 has been replicated 1 time(s)
FlipFlop D_1 has been replicated 1 time(s)
FlipFlop D_0 has been replicated 1 time(s)
FlipFlop D_2 has been replicated 1 time(s)

==========
*   Final Report   *
==========
Final Results
RTL Top Level Output File Name   : encryptor.ngr
Top Level Output File Name   : encryptor
Output Format   : NGC
Optimization Goal   : Speed
Keep Hierarchy   : NO

Design Statistics
IOs   : 52

Macro Statistics :

```
# Registers                      : 15
#      1-bit register            : 2
#      16-bit register           : 12
#      7-bit register            : 1
# Multiplexers                   : 2
#      16-bit 16-to-1 multiplexer  : 2
# Adders/Subtractors             : 131
#      16-bit adder              : 130
#      7-bit adder               : 1
# Comparators                    : 1
#      8-bit comparator less       : 1
# Xors                         : 14
#      16-bit xor3               : 14

Cell Usage :
# BELS                         : 6525
#      GND                       : 1
#      LUT1                      : 677
#      LUT2                      : 1328
#      LUT2_D                      : 5
#      LUT2_L                      : 23
#      LUT3                      : 93
#      LUT3_D                      : 9
#      LUT3_L                      : 5
#      LUT4                      : 547
#      LUT4_D                      : 34
#      LUT4_L                      : 8
#      MUXCY                       : 1886
#      VCC                       : 1
#      XORCY                       : 1908
# FlipFlops/Latches              : 222
#      FDC                       : 92
#      FDCE                      : 7
#      FDE                       : 105
#      FDP                       : 2
#      LD_1                      : 16
# Clock Buffers                  : 1
#      BUFGP                     : 1
# IO Buffers                     : 51
#      IBUF                      : 34
#      OBUF                      : 17
=========================================================================
==========

Device utilization summary:
---------------------------
```

Selected Device : 3s400pq208-5

Number of Slices:	1570	out of 3584	43%
Number of Slice Flip Flops:	222	out of 7168	3%
Number of 4 input LUTs:	2729	out of 7168	38%
Number of bonded IOBs:	51	out of 141	36%
Number of GCLKs:	1	out of 8	12%

==========
TIMING REPORT

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

Clock Signal	Clock buffer(FF name)	Load
state_out_FFd4-In(state_out_FFd4-In1:O)|	NONE(*)(ciphertext_13)	16
clock	BUFGP	206

(*) This 1 clock signal(s) are generated by combinatorial logic,
and XST is not able to identify which are the primary clock signals.
Please use the CLOCK_SIGNAL constraint to specify the clock signal(s) generated by combinatorial logic.

Timing Summary:

Speed Grade: -5

Minimum period: 6.074ns (Maximum Frequency: 164.636MHz)
Minimum input arrival time before clock: 49.814ns
Maximum output required time after clock: 5.714ns
Maximum combinational path delay: No path found

Timing Detail:

All values displayed in nanoseconds (ns)

Timing constraint: Default period analysis for Clock 'clock'
Delay: 6.074ns (Levels of Logic = 15)
Source: B_0 (FF)
Destination: A_temp1_3 (FF)
Source Clock: clock rising
Destination Clock: clock rising

Data Path: B_0 to A_temp1_3

Cell:in->out	Gate fanout	Net Delay	Delay	Logical Name (Net Name)
FDC:C->Q	13	0.000	0.895	B_0 (B_0)
LUT2:I0->O	3	0.000	0.577	a1__n00331 (a1_P2<5>)
LUT4_D:I1->O	1	0.000	0.240	a1_w1_ca1_fa0_Mxor_sf_Xo<11>1 (a1_w1_ca1_su1<5>)
LUT4_D:I0->O	4	0.000	0.629	a1_w1_ca1_fa3_Mxor_sf_Xo<11>1 (a1_w1_ca1_su4<5>)
LUT2:I1->O	1	0.000	0.240	a1_w1_ca1_fa5_Mxor_sf_Xo<11>1 (a1_w1_ca1_su6<5>)
LUT4:I2->O	3	0.000	0.577	a1_w1_ca2__n01091 (a1_w1_ca2_c<7>)
LUT3_L:I0->LO	1	0.000	0.100	a1_w1_ca2_Ker345061 (a1_w1_ca2_N34508)
LUT4:I1->O	2	0.000	0.465	a1_w1_ca2__n01191 (a1_w1_ca2_c<9>)
LUT4_D:I0->LO	1	0.000	0.100	a1_w1_ca2_Ker345111 (N47013)
LUT4:I1->O	3	0.000	0.577	a1_w1_ca2__n01291 (a1_w1_ca2_c<11>)
LUT3_L:I0->LO	1	0.000	0.100	a1_w1_ca2_Ker345161 (a1_w1_ca2_N34518)
LUT4:I3->O	4	0.000	0.629	a1_w1_ca2__n01391 (a1_w1_ca2_c<13>)
LUT4:I0->O	2	0.000	0.465	a1_w1_ca2_Ker345291 (a1_w1_ca2_N34531)
LUT3:I1->O	1	0.000	0.240	a1_w1_ca2_Mxor_s1<15>_Result_SW0 (N38387)
LUT4_D:I2->O	1	0.000	0.240	a1_w1_ca2_Mxor_s1<15>_Result (product1<15>)
LUT2_L:I0->LO	1	0.000	0.000	Mxor__n0032_Result<3>1 (_n0032<3>)
FDE:D		0.000		A_temp1_3
Total		6.074ns (0.000ns logic, 6.074ns route) (0.0% logic, 100.0% route)		

Timing constraint: Default OFFSET IN BEFORE for Clock 'clock'
Offset: 49.814ns (Levels of Logic = 266)
Source: round_keyse<0> (PAD)
Destination: C_final_15 (FF)
Destination Clock: clock rising

```
  Data Path: round_keyse<0> to C_final_15
                            Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O            33   0.518   1.322  round_keyse_0_IBUF (round_keyse_0_IBUF)
     LUT1:I0->O            1   0.000   0.000  Madd_l<0>_inst_lut2_161
(Madd_l<0>_inst_lut2_16)
     MUXCY:S->O            1   0.000   0.000  Madd_l<0>_inst_cy_15
(Madd_l<0>_inst_cy_15)
     MUXCY:CI->O           1   0.000   0.000  Madd_l<0>_inst_cy_16
(Madd_l<0>_inst_cy_16)
     MUXCY:CI->O           1   0.000   0.000  Madd_l<0>_inst_cy_17
(Madd_l<0>_inst_cy_17)
     XORCY:CI->O           3   0.000   0.577  Madd_l<0>_inst_sum_19 (l<0><3>)
     LUT1:I0->O            1   0.000   0.000  Madd_s<1>_inst_lut2_551
(Madd_s<1>_inst_lut2_55)
     MUXCY:S->O            1   0.000   0.000  Madd_s<1>_inst_cy_54
(Madd_s<1>_inst_cy_54)
     MUXCY:CI->O           1   0.000   0.000  Madd_s<1>_inst_cy_55
(Madd_s<1>_inst_cy_55)
     MUXCY:CI->O           1   0.000   0.000  Madd_s<1>_inst_cy_56
(Madd_s<1>_inst_cy_56)
     MUXCY:CI->O           1   0.000   0.000  Madd_s<1>_inst_cy_57
(Madd_s<1>_inst_cy_57)
     MUXCY:CI->O           1   0.000   0.000  Madd_s<1>_inst_cy_58
(Madd_s<1>_inst_cy_58)
     MUXCY:CI->O           1   0.000   0.000  Madd_s<1>_inst_cy_59
(Madd_s<1>_inst_cy_59)
     MUXCY:CI->O           1   0.000   0.000  Madd_s<1>_inst_cy_60
(Madd_s<1>_inst_cy_60)
     MUXCY:CI->O           1   0.000   0.000  Madd_s<1>_inst_cy_61
(Madd_s<1>_inst_cy_61)
     MUXCY:CI->O           1   0.000   0.000  Madd_s<1>_inst_cy_62
(Madd_s<1>_inst_cy_62)
     MUXCY:CI->O           1   0.000   0.000  Madd_s<1>_inst_cy_63
(Madd_s<1>_inst_cy_63)
     MUXCY:CI->O           1   0.000   0.000  Madd_s<1>_inst_cy_64
(Madd_s<1>_inst_cy_64)
     MUXCY:CI->O           0   0.000   0.000  Madd_s<1>_inst_cy_65
(Madd_s<1>_inst_cy_65)
     XORCY:CI->O           3   0.000   0.577  Madd_s<1>_inst_sum_67 (s<1><15>)
     LUT2:I0->O            0   0.000   0.000  Madd_l<1>_inst_lut2_151
(Madd_l<1>_inst_lut2_15)
     XORCY:LI->O           2   0.000   0.465  Madd_l<1>_inst_sum_15 (l<1><15>)
     LUT2:I1->O            0   0.000   0.000  Madd__n0074_inst_lut2_151
(Madd__n0074_inst_lut2_15)
```

```
    XORCY:LI->O           1   0.000   0.240  Madd__n0074_inst_sum_15 (_n0074<15>)
    LUT1:I0->O            0   0.000   0.000  Madd_s<2>_inst_lut2_541
(Madd_s<2>_inst_lut2_54)
    XORCY:LI->O           2   0.000   0.465  Madd_s<2>_inst_sum_54 (s<2><15>)
    LUT2:I0->O            0   0.000   0.000  Madd_l<2>_inst_lut2_151
(Madd_l<2>_inst_lut2_15)
    XORCY:LI->O           2   0.000   0.465  Madd_l<2>_inst_sum_15 (l<2><15>)
    LUT2:I1->O            0   0.000   0.000  Madd__n0075_inst_lut2_151
(Madd__n0075_inst_lut2_15)
    XORCY:LI->O           1   0.000   0.240  Madd__n0075_inst_sum_15 (_n0075<15>)
    LUT1:I0->O            0   0.000   0.000  Madd_s<3>_inst_lut2_541
(Madd_s<3>_inst_lut2_54)
    XORCY:LI->O           2   0.000   0.465  Madd_s<3>_inst_sum_54 (s<3><15>)
    LUT2:I0->O            0   0.000   0.000  Madd_l<3>_inst_lut2_151
(Madd_l<3>_inst_lut2_15)
    XORCY:LI->O           2   0.000   0.465  Madd_l<3>_inst_sum_15 (l<3><15>)
    LUT2:I1->O            0   0.000   0.000  Madd__n0076_inst_lut2_151
(Madd__n0076_inst_lut2_15)
    XORCY:LI->O           1   0.000   0.240  Madd__n0076_inst_sum_15 (_n0076<15>)
    LUT1:I0->O            0   0.000   0.000  Madd_s<4>_inst_lut2_541
(Madd_s<4>_inst_lut2_54)
    XORCY:LI->O           2   0.000   0.465  Madd_s<4>_inst_sum_54 (s<4><15>)
    LUT2:I0->O            0   0.000   0.000  Madd_l<4>_inst_lut2_151
(Madd_l<4>_inst_lut2_15)
    XORCY:LI->O           2   0.000   0.465  Madd_l<4>_inst_sum_15 (l<4><15>)
    LUT2:I1->O            0   0.000   0.000  Madd__n0077_inst_lut2_151
(Madd__n0077_inst_lut2_15)
    XORCY:LI->O           1   0.000   0.240  Madd__n0077_inst_sum_15 (_n0077<15>)
    LUT1:I0->O            0   0.000   0.000  Madd_s<5>_inst_lut2_541
(Madd_s<5>_inst_lut2_54)
    XORCY:LI->O           2   0.000   0.465  Madd_s<5>_inst_sum_54 (s<5><15>)
    LUT2:I0->O            0   0.000   0.000  Madd_l<5>_inst_lut2_151
(Madd_l<5>_inst_lut2_15)
    XORCY:LI->O           2   0.000   0.465  Madd_l<5>_inst_sum_15 (l<5><15>)
    LUT2:I1->O            0   0.000   0.000  Madd__n0078_inst_lut2_151
(Madd__n0078_inst_lut2_15)
    XORCY:LI->O           1   0.000   0.240  Madd__n0078_inst_sum_15 (_n0078<15>)
    LUT1:I0->O            0   0.000   0.000  Madd_s<6>_inst_lut2_541
(Madd_s<6>_inst_lut2_54)
    XORCY:LI->O           2   0.000   0.465  Madd_s<6>_inst_sum_54 (s<6><15>)
    LUT2:I0->O            0   0.000   0.000  Madd_l<6>_inst_lut2_151
(Madd_l<6>_inst_lut2_15)
    XORCY:LI->O           2   0.000   0.465  Madd_l<6>_inst_sum_15 (l<6><15>)
    LUT2:I1->O            0   0.000   0.000  Madd__n0079_inst_lut2_151
(Madd__n0079_inst_lut2_15)
    XORCY:LI->O           1   0.000   0.240  Madd__n0079_inst_sum_15 (_n0079<15>)
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LUT1:I0->O 0 0.000 0.000 Madd_s<7>_inst_lut2_541
(Madd_s<7>_inst_lut2_54)
XORCY:LI->O 2 0.000 0.465 Madd_s<7>_inst_sum_54 (s<7><15>)
LUT2:I0->O 0 0.000 0.000 Madd_l<7>_inst_lut2_151
(Madd_l<7>_inst_lut2_15)
XORCY:LI->O 2 0.000 0.465 Madd_l<7>_inst_sum_15 (l<7><15>)
LUT2:I1->O 0 0.000 0.000 Madd__n0080_inst_lut2_151
(Madd__n0080_inst_lut2_15)
XORCY:LI->O 1 0.000 0.240 Madd__n0080_inst_sum_15 (_n0080<15>)
LUT1:I0->O 0 0.000 0.000 Madd_s<8>_inst_lut2_541
(Madd_s<8>_inst_lut2_54)
XORCY:LI->O 2 0.000 0.465 Madd_s<8>_inst_sum_54 (s<8><15>)
LUT2:I0->O 0 0.000 0.000 Madd_l<8>_inst_lut2_151
(Madd_l<8>_inst_lut2_15)
XORCY:LI->O 2 0.000 0.465 Madd_l<8>_inst_sum_15 (l<8><15>)
LUT2:I1->O 0 0.000 0.000 Madd__n0081_inst_lut2_151
(Madd__n0081_inst_lut2_15)
XORCY:LI->O 1 0.000 0.240 Madd__n0081_inst_sum_15 (_n0081<15>)
LUT1:I0->O 0 0.000 0.000 Madd_s<9>_inst_lut2_541
(Madd_s<9>_inst_lut2_54)
XORCY:LI->O 2 0.000 0.465 Madd_s<9>_inst_sum_54 (s<9><15>)
LUT2:I0->O 0 0.000 0.000 Madd_l<9>_inst_lut2_151
(Madd_l<9>_inst_lut2_15)
XORCY:LI->O 2 0.000 0.465 Madd_l<9>_inst_sum_15 (l<9><15>)
LUT2:I1->O 0 0.000 0.000 Madd__n0082_inst_lut2_151
(Madd__n0082_inst_lut2_15)
XORCY:LI->O 1 0.000 0.240 Madd__n0082_inst_sum_15 (_n0082<15>)
LUT1:I0->O 0 0.000 0.000 Madd_s<10>_inst_lut2_541
(Madd_s<10>_inst_lut2_54)
XORCY:LI->O 2 0.000 0.465 Madd_s<10>_inst_sum_54 (s<10><15>)
LUT2:I0->O 0 0.000 0.000 Madd_l<10>_inst_lut2_151
(Madd_l<10>_inst_lut2_15)
XORCY:LI->O 2 0.000 0.465 Madd_l<10>_inst_sum_15 (l<10><15>)
LUT2:I1->O 0 0.000 0.000 Madd__n0083_inst_lut2_151
(Madd__n0083_inst_lut2_15)
XORCY:LI->O 1 0.000 0.240 Madd__n0083_inst_sum_15 (_n0083<15>)
LUT1:I0->O 0 0.000 0.000 Madd_s<11>_inst_lut2_541
(Madd_s<11>_inst_lut2_54)
XORCY:LI->O 2 0.000 0.465 Madd_s<11>_inst_sum_54 (s<11><15>)
LUT2:I0->O 0 0.000 0.000 Madd_l<11>_inst_lut2_151
(Madd_l<11>_inst_lut2_15)
XORCY:LI->O 2 0.000 0.465 Madd_l<11>_inst_sum_15 (l<11><15>)
LUT2:I1->O 0 0.000 0.000 Madd__n0084_inst_lut2_151
(Madd__n0084_inst_lut2_15)
XORCY:LI->O 1 0.000 0.240 Madd__n0084_inst_sum_15 (_n0084<15>)

LUT1:I0->O 0 0.000 0.000 Madd_s<12>_inst_lut2_541
(Madd_s<12>_inst_lut2_54)
XORCY:LI->O 2 0.000 0.465 Madd_s<12>_inst_sum_54 (s<12><15>)
LUT2:I0->O 0 0.000 0.000 Madd_l<12>_inst_lut2_151
(Madd_l<12>_inst_lut2_15)
XORCY:LI->O 2 0.000 0.465 Madd_l<12>_inst_sum_15 (l<12><15>)
LUT2:I1->O 0 0.000 0.000 Madd__n0085_inst_lut2_151
(Madd__n0085_inst_lut2_15)
XORCY:LI->O 1 0.000 0.240 Madd__n0085_inst_sum_15 (_n0085<15>)
LUT1:I0->O 0 0.000 0.000 Madd_s<13>_inst_lut2_541
(Madd_s<13>_inst_lut2_54)
XORCY:LI->O 2 0.000 0.465 Madd_s<13>_inst_sum_54 (s<13><15>)
LUT2:I0->O 0 0.000 0.000 Madd_l<13>_inst_lut2_151
(Madd_l<13>_inst_lut2_15)
XORCY:LI->O 2 0.000 0.465 Madd_l<13>_inst_sum_15 (l<13><15>)
LUT2:I1->O 0 0.000 0.000 Madd__n0086_inst_lut2_151
(Madd__n0086_inst_lut2_15)
XORCY:LI->O 1 0.000 0.240 Madd__n0086_inst_sum_15 (_n0086<15>)
LUT1:I0->O 0 0.000 0.000 Madd_s<14>_inst_lut2_541
(Madd_s<14>_inst_lut2_54)
XORCY:LI->O 2 0.000 0.465 Madd_s<14>_inst_sum_54 (s<14><15>)
LUT2:I0->O 0 0.000 0.000 Madd_l<14>_inst_lut2_151
(Madd_l<14>_inst_lut2_15)
XORCY:LI->O 2 0.000 0.465 Madd_l<14>_inst_sum_15 (l<14><15>)
LUT2:I1->O 0 0.000 0.000 Madd__n0087_inst_lut2_151
(Madd__n0087_inst_lut2_15)
XORCY:LI->O 1 0.000 0.240 Madd__n0087_inst_sum_15 (_n0087<15>)
LUT1:I0->O 0 0.000 0.000 Madd_s<15>_inst_lut2_541
(Madd_s<15>_inst_lut2_54)
XORCY:LI->O 2 0.000 0.465 Madd_s<15>_inst_sum_54 (s<15><15>)
LUT2:I0->O 0 0.000 0.000 Madd_l<15>_inst_lut2_151
(Madd_l<15>_inst_lut2_15)
XORCY:LI->O 2 0.000 0.465 Madd_l<15>_inst_sum_15 (l<15><15>)
LUT2:I1->O 0 0.000 0.000 Madd__n0088_inst_lut2_151
(Madd__n0088_inst_lut2_15)
XORCY:LI->O 1 0.000 0.240 Madd__n0088_inst_sum_15 (_n0088<15>)
LUT1:I0->O 0 0.000 0.000 Madd_s<16>_inst_lut2_541
(Madd_s<16>_inst_lut2_54)
XORCY:LI->O 2 0.000 0.465 Madd_s<16>_inst_sum_54 (s<16><15>)
LUT2:I0->O 0 0.000 0.000 Madd_l<16>_inst_lut2_151
(Madd_l<16>_inst_lut2_15)
XORCY:LI->O 2 0.000 0.465 Madd_l<16>_inst_sum_15 (l<16><15>)
LUT2:I1->O 0 0.000 0.000 Madd__n0089_inst_lut2_151
(Madd__n0089_inst_lut2_15)
XORCY:LI->O 1 0.000 0.240 Madd__n0089_inst_sum_15 (_n0089<15>)

LUT1:I0->O 0 0.000 0.000 Madd_s<17>_inst_lut2_541
(Madd_s<17>_inst_lut2_54)
XORCY:LI->O 2 0.000 0.465 Madd_s<17>_inst_sum_54 (s<17><15>)
LUT2:I0->O 0 0.000 0.000 Madd_l<17>_inst_lut2_151
(Madd_l<17>_inst_lut2_15)
XORCY:LI->O 2 0.000 0.465 Madd_l<17>_inst_sum_15 (l<17><15>)
LUT2:I1->O 0 0.000 0.000 Madd__n0090_inst_lut2_151
(Madd__n0090_inst_lut2_15)
XORCY:LI->O 1 0.000 0.240 Madd__n0090_inst_sum_15 (_n0090<15>)
LUT1:I0->O 0 0.000 0.000 Madd_s<18>_inst_lut2_541
(Madd_s<18>_inst_lut2_54)
XORCY:LI->O 2 0.000 0.465 Madd_s<18>_inst_sum_54 (s<18><15>)
LUT2:I0->O 0 0.000 0.000 Madd_l<18>_inst_lut2_151
(Madd_l<18>_inst_lut2_15)
XORCY:LI->O 2 0.000 0.465 Madd_l<18>_inst_sum_15 (l<18><15>)
LUT2:I1->O 0 0.000 0.000 Madd__n0091_inst_lut2_151
(Madd__n0091_inst_lut2_15)
XORCY:LI->O 1 0.000 0.240 Madd__n0091_inst_sum_15 (_n0091<15>)
LUT1:I0->O 0 0.000 0.000 Madd_s<19>_inst_lut2_541
(Madd_s<19>_inst_lut2_54)
XORCY:LI->O 2 0.000 0.465 Madd_s<19>_inst_sum_54 (s<19><15>)
LUT2:I0->O 0 0.000 0.000 Madd_l<19>_inst_lut2_151
(Madd_l<19>_inst_lut2_15)
XORCY:LI->O 2 0.000 0.465 Madd_l<19>_inst_sum_15 (l<19><15>)
LUT2:I1->O 0 0.000 0.000 Madd__n0092_inst_lut2_151
(Madd__n0092_inst_lut2_15)
XORCY:LI->O 1 0.000 0.240 Madd__n0092_inst_sum_15 (_n0092<15>)
LUT1:I0->O 0 0.000 0.000 Madd_s<20>_inst_lut2_541
(Madd_s<20>_inst_lut2_54)
XORCY:LI->O 2 0.000 0.465 Madd_s<20>_inst_sum_54 (s<20><15>)
LUT2:I0->O 0 0.000 0.000 Madd_l<20>_inst_lut2_151
(Madd_l<20>_inst_lut2_15)
XORCY:LI->O 2 0.000 0.465 Madd_l<20>_inst_sum_15 (l<20><15>)
LUT2:I1->O 0 0.000 0.000 Madd__n0093_inst_lut2_151
(Madd__n0093_inst_lut2_15)
XORCY:LI->O 1 0.000 0.240 Madd__n0093_inst_sum_15 (_n0093<15>)
LUT1:I0->O 0 0.000 0.000 Madd_s<21>_inst_lut2_541
(Madd_s<21>_inst_lut2_54)
XORCY:LI->O 2 0.000 0.465 Madd_s<21>_inst_sum_54 (s<21><15>)
LUT2:I0->O 0 0.000 0.000 Madd_l<21>_inst_lut2_151
(Madd_l<21>_inst_lut2_15)
XORCY:LI->O 2 0.000 0.465 Madd_l<21>_inst_sum_15 (l<21><15>)
LUT2:I1->O 0 0.000 0.000 Madd__n0094_inst_lut2_151
(Madd__n0094_inst_lut2_15)
XORCY:LI->O 1 0.000 0.240 Madd__n0094_inst_sum_15 (_n0094<15>)

LUT1:I0->O 0 0.000 0.000 Madd_s<22>_inst_lut2_541
(Madd_s<22>_inst_lut2_54)
XORCY:LI->O 2 0.000 0.465 Madd_s<22>_inst_sum_54 (s<22><15>)
LUT2:I0->O 0 0.000 0.000 Madd_l<22>_inst_lut2_151
(Madd_l<22>_inst_lut2_15)
XORCY:LI->O 2 0.000 0.465 Madd_l<22>_inst_sum_15 (l<22><15>)
LUT2:I1->O 0 0.000 0.000 Madd__n0095_inst_lut2_151
(Madd__n0095_inst_lut2_15)
XORCY:LI->O 1 0.000 0.240 Madd__n0095_inst_sum_15 (_n0095<15>)
LUT1:I0->O 0 0.000 0.000 Madd_s<23>_inst_lut2_541
(Madd_s<23>_inst_lut2_54)
XORCY:LI->O 2 0.000 0.465 Madd_s<23>_inst_sum_54 (s<23><15>)
LUT2:I0->O 0 0.000 0.000 Madd_l<23>_inst_lut2_151
(Madd_l<23>_inst_lut2_15)
XORCY:LI->O 2 0.000 0.465 Madd_l<23>_inst_sum_15 (l<23><15>)
LUT2:I1->O 0 0.000 0.000 Madd__n0096_inst_lut2_151
(Madd__n0096_inst_lut2_15)
XORCY:LI->O 1 0.000 0.240 Madd__n0096_inst_sum_15 (_n0096<15>)
LUT1:I0->O 0 0.000 0.000 Madd_s<24>_inst_lut2_541
(Madd_s<24>_inst_lut2_54)
XORCY:LI->O 2 0.000 0.465 Madd_s<24>_inst_sum_54 (s<24><15>)
LUT2:I0->O 0 0.000 0.000 Madd_l<29>_inst_lut2_151
(Madd_l<29>_inst_lut2_15)
XORCY:LI->O 4 0.000 0.629 Madd_l<29>_inst_sum_15 (l<29><15>)
LUT2:I1->O 0 0.000 0.000 Madd__n0097_inst_lut2_151
(Madd__n0097_inst_lut2_15)
XORCY:LI->O 1 0.000 0.240 Madd__n0097_inst_sum_15 (_n0097<15>)
LUT1:I0->O 0 0.000 0.000 Madd_s<25>_inst_lut2_541
(Madd_s<25>_inst_lut2_54)
XORCY:LI->O 2 0.000 0.465 Madd_s<25>_inst_sum_54 (s<25><15>)
LUT2:I0->O 0 0.000 0.000 Madd_l<25>_inst_lut2_151
(Madd_l<25>_inst_lut2_15)
XORCY:LI->O 2 0.000 0.465 Madd_l<25>_inst_sum_15 (l<25><15>)
LUT2:I1->O 0 0.000 0.000 Madd__n0098_inst_lut2_151
(Madd__n0098_inst_lut2_15)
XORCY:LI->O 1 0.000 0.240 Madd__n0098_inst_sum_15 (_n0098<15>)
LUT1:I0->O 0 0.000 0.000 Madd_s<26>_inst_lut2_541
(Madd_s<26>_inst_lut2_54)
XORCY:LI->O 2 0.000 0.465 Madd_s<26>_inst_sum_54 (s<26><15>)
LUT2:I0->O 0 0.000 0.000 Madd_l<26>_inst_lut2_151
(Madd_l<26>_inst_lut2_15)
XORCY:LI->O 2 0.000 0.465 Madd_l<26>_inst_sum_15 (l<26><15>)
LUT2:I1->O 0 0.000 0.000 Madd__n0099_inst_lut2_151
(Madd__n0099_inst_lut2_15)
XORCY:LI->O 1 0.000 0.240 Madd__n0099_inst_sum_15 (_n0099<15>)

LUT1:I0->O 0 0.000 0.000 Madd_s<27>_inst_lut2_541
(Madd_s<27>_inst_lut2_54)
XORCY:LI->O 2 0.000 0.465 Madd_s<27>_inst_sum_54 (s<27><15>)
LUT2:I0->O 0 0.000 0.000 Madd_l<27>_inst_lut2_151
(Madd_l<27>_inst_lut2_15)
XORCY:LI->O 2 0.000 0.465 Madd_l<27>_inst_sum_15 (l<27><15>)
LUT2:I1->O 0 0.000 0.000 Madd__n0100_inst_lut2_151
(Madd__n0100_inst_lut2_15)
XORCY:LI->O 1 0.000 0.240 Madd__n0100_inst_sum_15 (_n0100<15>)
LUT1:I0->O 0 0.000 0.000 Madd_s<28>_inst_lut2_541
(Madd_s<28>_inst_lut2_54)
XORCY:LI->O 2 0.000 0.465 Madd_s<28>_inst_sum_54 (s<28><15>)
LUT2:I0->O 0 0.000 0.000 Madd_l<28>_inst_lut2_151
(Madd_l<28>_inst_lut2_15)
XORCY:LI->O 1 0.000 0.240 Madd_l<28>_inst_sum_15 (l<28><15>)
LUT2:I1->O 0 0.000 0.000 Madd__n0101_inst_lut2_151
(Madd__n0101_inst_lut2_15)
XORCY:LI->O 1 0.000 0.240 Madd__n0101_inst_sum_15 (_n0101<15>)
LUT1:I0->O 0 0.000 0.000 Madd_s<29>_inst_lut2_541
(Madd_s<29>_inst_lut2_54)
XORCY:LI->O 1 0.000 0.240 Madd_s<29>_inst_sum_54 (s<29><15>)
LUT2:I0->O 0 0.000 0.000 Madd__n0102_inst_lut2_151
(Madd__n0102_inst_lut2_15)
XORCY:LI->O 1 0.000 0.240 Madd__n0102_inst_sum_15 (_n0102<15>)
LUT1:I0->O 0 0.000 0.000 Madd_s<30>_inst_lut2_541
(Madd_s<30>_inst_lut2_54)
XORCY:LI->O 2 0.000 0.465 Madd_s<30>_inst_sum_54 (s<30><15>)
LUT2:I0->O 0 0.000 0.000 Madd_l<30>_inst_lut2_151
(Madd_l<30>_inst_lut2_15)
XORCY:LI->O 2 0.000 0.465 Madd_l<30>_inst_sum_15 (l<30><15>)
LUT2:I1->O 0 0.000 0.000 Madd__n0103_inst_lut2_151
(Madd__n0103_inst_lut2_15)
XORCY:LI->O 1 0.000 0.240 Madd__n0103_inst_sum_15 (_n0103<15>)
LUT1:I0->O 0 0.000 0.000 Madd_s<31>_inst_lut2_541
(Madd_s<31>_inst_lut2_54)
XORCY:LI->O 2 0.000 0.465 Madd_s<31>_inst_sum_54 (s<31><15>)
LUT2:I0->O 0 0.000 0.000 Madd_l<31>_inst_lut2_151
(Madd_l<31>_inst_lut2_15)
XORCY:LI->O 2 0.000 0.465 Madd_l<31>_inst_sum_15 (l<31><15>)
LUT2:I1->O 0 0.000 0.000 Madd__n0104_inst_lut2_151
(Madd__n0104_inst_lut2_15)
XORCY:LI->O 1 0.000 0.240 Madd__n0104_inst_sum_15 (_n0104<15>)
LUT1:I0->O 0 0.000 0.000 Madd_s<32>_inst_lut2_541
(Madd_s<32>_inst_lut2_54)
XORCY:LI->O 2 0.000 0.465 Madd_s<32>_inst_sum_54 (s<32><15>)

LUT2:I0->O 0 0.000 0.000 Madd_l<32>_inst_lut2_151 (Madd_l<32>_inst_lut2_15)
XORCY:LI->O 2 0.000 0.465 Madd_l<32>_inst_sum_15 (l<32><15>)
LUT2:I1->O 0 0.000 0.000 Madd__n0105_inst_lut2_151 (Madd__n0105_inst_lut2_15)
XORCY:LI->O 1 0.000 0.240 Madd__n0105_inst_sum_15 (_n0105<15>)
LUT1:I0->O 0 0.000 0.000 Madd_s<33>_inst_lut2_541 (Madd_s<33>_inst_lut2_54)
XORCY:LI->O 2 0.000 0.465 Madd_s<33>_inst_sum_54 (s<33><15>)
LUT2:I0->O 0 0.000 0.000 Madd_l<33>_inst_lut2_151 (Madd_l<33>_inst_lut2_15)
XORCY:LI->O 2 0.000 0.465 Madd_l<33>_inst_sum_15 (l<33><15>)
LUT2:I1->O 0 0.000 0.000 Madd__n0106_inst_lut2_151 (Madd__n0106_inst_lut2_15)
XORCY:LI->O 1 0.000 0.240 Madd__n0106_inst_sum_15 (_n0106<15>)
LUT1:I0->O 0 0.000 0.000 Madd_s<34>_inst_lut2_541 (Madd_s<34>_inst_lut2_54)
XORCY:LI->O 2 0.000 0.465 Madd_s<34>_inst_sum_54 (s<34><15>)
LUT2:I0->O 0 0.000 0.000 Madd_l<39>_inst_lut2_151 (Madd_l<39>_inst_lut2_15)
XORCY:LI->O 4 0.000 0.629 Madd_l<39>_inst_sum_15 (l<39><15>)
LUT2:I1->O 0 0.000 0.000 Madd__n0107_inst_lut2_151 (Madd__n0107_inst_lut2_15)
XORCY:LI->O 1 0.000 0.240 Madd__n0107_inst_sum_15 (_n0107<15>)
LUT1:I0->O 0 0.000 0.000 Madd_s<35>_inst_lut2_541 (Madd_s<35>_inst_lut2_54)
XORCY:LI->O 2 0.000 0.465 Madd_s<35>_inst_sum_54 (s<35><15>)
LUT2:I0->O 0 0.000 0.000 Madd_l<35>_inst_lut2_151 (Madd_l<35>_inst_lut2_15)
XORCY:LI->O 2 0.000 0.465 Madd_l<35>_inst_sum_15 (l<35><15>)
LUT2:I1->O 0 0.000 0.000 Madd__n0108_inst_lut2_151 (Madd__n0108_inst_lut2_15)
XORCY:LI->O 1 0.000 0.240 Madd__n0108_inst_sum_15 (_n0108<15>)
LUT1:I0->O 0 0.000 0.000 Madd_s<36>_inst_lut2_541 (Madd_s<36>_inst_lut2_54)
XORCY:LI->O 2 0.000 0.465 Madd_s<36>_inst_sum_54 (s<36><15>)
LUT2:I0->O 0 0.000 0.000 Madd_l<36>_inst_lut2_151 (Madd_l<36>_inst_lut2_15)
XORCY:LI->O 2 0.000 0.465 Madd_l<36>_inst_sum_15 (l<36><15>)
LUT2:I1->O 0 0.000 0.000 Madd__n0109_inst_lut2_151 (Madd__n0109_inst_lut2_15)
XORCY:LI->O 1 0.000 0.240 Madd__n0109_inst_sum_15 (_n0109<15>)
LUT1:I0->O 0 0.000 0.000 Madd_s<37>_inst_lut2_541 (Madd_s<37>_inst_lut2_54)
XORCY:LI->O 2 0.000 0.465 Madd_s<37>_inst_sum_54 (s<37><15>)

LUT2:I0->O 0 0.000 0.000 Madd_l<37>_inst_lut2_151
(Madd_l<37>_inst_lut2_15)
XORCY:LI->O 2 0.000 0.465 Madd_l<37>_inst_sum_15 (l<37><15>)
LUT2:I1->O 0 0.000 0.000 Madd__n0110_inst_lut2_151
(Madd__n0110_inst_lut2_15)
XORCY:LI->O 1 0.000 0.240 Madd__n0110_inst_sum_15 (_n0110<15>)
LUT1:I0->O 0 0.000 0.000 Madd_s<38>_inst_lut2_541
(Madd_s<38>_inst_lut2_54)
XORCY:LI->O 2 0.000 0.465 Madd_s<38>_inst_sum_54 (s<38><15>)
LUT2:I0->O 0 0.000 0.000 Madd_l<38>_inst_lut2_151
(Madd_l<38>_inst_lut2_15)
XORCY:LI->O 1 0.000 0.240 Madd_l<38>_inst_sum_15 (l<38><15>)
LUT2:I1->O 0 0.000 0.000 Madd__n0111_inst_lut2_151
(Madd__n0111_inst_lut2_15)
XORCY:LI->O 1 0.000 0.240 Madd__n0111_inst_sum_15 (_n0111<15>)
LUT1:I0->O 0 0.000 0.000 Madd_s<39>_inst_lut2_541
(Madd_s<39>_inst_lut2_54)
XORCY:LI->O 1 0.000 0.240 Madd_s<39>_inst_sum_54 (s<39><15>)
LUT2:I0->O 0 0.000 0.000 Madd__n0112_inst_lut2_151
(Madd__n0112_inst_lut2_15)
XORCY:LI->O 1 0.000 0.240 Madd__n0112_inst_sum_15 (_n0112<15>)
LUT1:I0->O 0 0.000 0.000 Madd_s<40>_inst_lut2_541
(Madd_s<40>_inst_lut2_54)
XORCY:LI->O 3 0.000 0.577 Madd_s<40>_inst_sum_54 (s<40><15>)
LUT2:I0->O 0 0.000 0.000 Madd_l<40>_inst_lut2_151
(Madd_l<40>_inst_lut2_15)
XORCY:LI->O 1 0.000 0.240 Madd_l<40>_inst_sum_15 (l<40><15>)
LUT2:I1->O 0 0.000 0.000 Madd__n0040_inst_lut2_151
(Madd__n0040_inst_lut2_15)
XORCY:LI->O 2 0.000 0.465 Madd__n0040_inst_sum_15 (l<41><15>)
LUT1:I0->O 0 0.000 0.000 Madd_s<41>_inst_lut2_541
(Madd_s<41>_inst_lut2_54)
XORCY:LI->O 2 0.000 0.465 Madd_s<41>_inst_sum_54 (s<41><15>)
LUT2:I0->O 0 0.000 0.000 Madd__n0041_inst_lut2_151
(Madd__n0041_inst_lut2_15)
XORCY:LI->O 2 0.000 0.465 Madd__n0041_inst_sum_15 (l<42><15>)
LUT1:I0->O 0 0.000 0.000 Madd_s<42>_inst_lut2_541
(Madd_s<42>_inst_lut2_54)
XORCY:LI->O 2 0.000 0.465 Madd_s<42>_inst_sum_54 (s<42><15>)
LUT2:I0->O 0 0.000 0.000 Madd__n0113_inst_lut2_151
(Madd__n0113_inst_lut2_15)
XORCY:LI->O 1 0.000 0.240 Madd__n0113_inst_sum_15 (_n0113<15>)
LUT1:I0->O 0 0.000 0.000 Madd_s<43>_inst_lut2_541
(Madd_s<43>_inst_lut2_54)
XORCY:LI->O 1 0.000 0.240 Madd_s<43>_inst_sum_54 (s<43><15>)

```
    LUT2:I0->O            0   0.000   0.000  Madd__n0039_inst_lut2_151
(Madd__n0039_inst_lut2_15)
    XORCY:LI->O           1   0.000   0.000  Madd__n0039_inst_sum_15 (_n0039<15>)
    FDE:D                     0.000          C_final_15
    ----------------------------------------
    Total                    49.814ns (0.518ns logic, 49.296ns route)
                                 (1.0% logic, 99.0% route)

--------------------------------------------------------------------------------
Timing constraint: Default OFFSET OUT AFTER for Clock 'clock'
Offset:              5.714ns (Levels of Logic = 1)
  Source:            ready_e (FF)
  Destination:       ready_e (PAD)
  Source Clock:      clock rising

  Data Path: ready_e to ready_e
                            Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
    FDC:C->Q              3   0.000   0.577  ready_e (ready_e_OBUF)
    OBUF:I->O                 5.137          ready_e_OBUF (ready_e)
    ----------------------------------------
    Total                     5.714ns (5.137ns logic, 0.577ns route)
                                 (89.9% logic, 10.1% route)

--------------------------------------------------------------------------------
Timing constraint: Default OFFSET OUT AFTER for Clock 'state_out_FFd4-In1:O'
Offset:              5.377ns (Levels of Logic = 1)
  Source:            ciphertext_15 (LATCH)
  Destination:       ciphertext<15> (PAD)
  Source Clock:      state_out_FFd4-In1:O rising

  Data Path: ciphertext_15 to ciphertext<15>
                            Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
    LD_1:G->Q             1   0.000   0.240  ciphertext_15 (ciphertext_15)
    OBUF:I->O                 5.137          ciphertext_15_OBUF (ciphertext<15>)
    ----------------------------------------
    Total                     5.377ns (5.137ns logic, 0.240ns route)
                                 (95.5% logic, 4.5% route)

==========================================================================
==========
CPU : 37.73 / 41.44 s | Elapsed : 38.00 / 40.00 s
```

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Total memory usage is 99100 kilobytes