Release 6.2i - xst G.28

--> Parameter TMPDIR set to __projnav
CPU : 0.00 / 0.59 s | Elapsed : 0.00 / 0.00 s

--> Parameter xsthdpdir set to ./xst
CPU : 0.00 / 0.59 s | Elapsed : 0.00 / 0.00 s

--> Reading design: decryptor.prj

TABLE OF CONTENTS

===
*   Synthesis Options Summary   *
===
---- Source Parameters
Input File Name   : decryptor.prj
Input Format   : mixed
Ignore Synthesis Constraint File   : NO
Verilog Include Directory   :

---- Target Parameters
Output File Name   : decryptor
Output Format   : NGC
Target Device   : xc3s400-5-pq208

---- Source Options
Top Module Name   : decryptor
Automatic FSM Extraction   : YES
FSM Encoding Algorithm   : Auto
FSM Style   : lut
RAM Extraction   : Yes
RAM Style   : Auto

ROM Extraction : Yes
ROM Style : Auto
Mux Extraction : YES
Mux Style : Auto
Decoder Extraction : YES
Priority Encoder Extraction : YES
Shift Register Extraction : YES
Logical Shifter Extraction : YES
XOR Collapsing : YES
Resource Sharing : YES
Multiplier Style : auto
Automatic Register Balancing : No

---- Target Options
Add IO Buffers : YES
Global Maximum Fanout : 500
Add Generic Clock Buffer(BUFG) : 8
Register Duplication : YES
Equivalent register Removal : YES
Slice Packing : YES
Pack IO Registers into IOBs : auto

---- General Options
Optimization Goal : Speed
Optimization Effort : 1
Keep Hierarchy : NO
Global Optimization : AllClockNets
RTL Output : Yes
Write Timing Constraints : NO
Hierarchy Separator : _
Bus Delimiter : <>
Case Specifier : maintain
Slice Utilization Ratio : 100
Slice Utilization Ratio Delta : 5

---- Other Options
lso : decryptor.lso
Read Cores : YES
cross_clock_analysis : NO
verilog2001 : YES
Optimize Instantiated Primitives : NO

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```
=========================================================================
*                     HDL Compilation                     *
=========================================================================
Compiling vhdl file g:/try/decry/../../project/Encryptor_Design1/full_adder.vhd in Library
work.
Architecture behavioral of Entity full_adder is up to date.
Compiling vhdl file g:/try/decry/../../project/Encryptor_Design1/carrysave_adder.vhd in
Library work.
Architecture behavioral of Entity carrysave_adder is up to date.
Compiling vhdl file g:/try/decry/../../project/Encryptor_Design1/carrylook_ahead2.vhd in
Library work.
Architecture behavioral of Entity carrylook_ahead2 is up to date.
Compiling vhdl file g:/try/decry/../../project/Encryptor_Design1/wallace_structure.vhd in
Library work.
Architecture behavioral of Entity wallace_structure is up to date.
Compiling vhdl file g:/try/decry/../../project/Encryptor_Design1/multiplier.vhd in Library
work.
Architecture behavioral of Entity multiplier is up to date.
Compiling vhdl file g:/try/decry/decry.vhdl in Library work.
Architecture arch_decryptor of Entity decryptor is up to date.

=========================================================================
*                     HDL Analysis                        *
=========================================================================
Analyzing Entity <decryptor> (Architecture <arch_decryptor>).
WARNING:Xst:1610 - g:/try/decry/decry.vhdl line 303: Width mismatch. <A_pre> has a
width of 16 bits but assigned expression is 31-bit wide.
WARNING:Xst:1610 - g:/try/decry/decry.vhdl line 307: Width mismatch. <C_pre> has a
width of 16 bits but assigned expression is 31-bit wide.
INFO:Xst:1304 - Contents of register <last_round> in unit <decryptor> never changes
during circuit operation. The register is replaced by logic.
INFO:Xst:1304 - Contents of register <cleanup> in unit <decryptor> never changes
during circuit operation. The register is replaced by logic.
INFO:Xst:1304 - Contents of register <ready_d_pre> in unit <decryptor> never changes
during circuit operation. The register is replaced by logic.
Entity <decryptor> analyzed. Unit <decryptor> generated.

Analyzing Entity <multiplier> (Architecture <behavioral>).
Entity <multiplier> analyzed. Unit <multiplier> generated.

Analyzing Entity <wallace_structure> (Architecture <behavioral>).
Entity <wallace_structure> analyzed. Unit <wallace_structure> generated.
```

```
Analyzing Entity <carrysave_adder> (Architecture <behavioral>).
Entity <carrysave_adder> analyzed. Unit <carrysave_adder> generated.

Analyzing Entity <full_adder> (Architecture <behavioral>).
Entity <full_adder> analyzed. Unit <full_adder> generated.

Analyzing Entity <carrylook_ahead2> (Architecture <behavioral>).
Entity <carrylook_ahead2> analyzed. Unit <carrylook_ahead2> generated.


=========================================================================
*                     HDL Synthesis                       *
=========================================================================

Synthesizing Unit <full_adder>.
    Related source file is g:/try/decry/../../project/Encryptor_Design1/full_adder.vhd.
WARNING:Xst:646 - Signal <sig<15>> is assigned but never used.
    Found 16-bit xor3 for signal <sf>.
    Summary:
        inferred  16 Xor(s).
Unit <full_adder> synthesized.


Synthesizing Unit <carrylook_ahead2>.
    Related source file is
g:/try/decry/../../project/Encryptor_Design1/carrylook_ahead2.vhd.
WARNING:Xst:646 - Signal <c<16>> is assigned but never used.
    Found 15-bit xor2 for signal <s1<15:1>>.
    Found 16-bit xor2 for signal <p>.
Unit <carrylook_ahead2> synthesized.


Synthesizing Unit <carrysave_adder>.
    Related source file is g:/try/decry/../../project/Encryptor_Design1/carrysave_adder.vhd.
Unit <carrysave_adder> synthesized.


Synthesizing Unit <wallace_structure>.
    Related source file is
g:/try/decry/../../project/Encryptor_Design1/wallace_structure.vhd.
WARNING:Xst:1780 - Signal <c_out> is never used or assigned.
Unit <wallace_structure> synthesized.
```

```
Synthesizing Unit <multiplier>.
    Related source file is g:/try/decry/../../project/Encryptor_Design1/multiplier.vhd.
Unit <multiplier> synthesized.


Synthesizing Unit <decryptor>.
    Related source file is g:/try/decry/decry.vhdl.
WARNING:Xst:646 - Signal <ttemp1<15:4>> is assigned but never used.
WARNING:Xst:646 - Signal <utemp1<15:4>> is assigned but never used.
WARNING:Xst:646 - Signal <last_round> is assigned but never used.
    Register <utemp1> equivalent to <u> has been removed
    Register <ttemp1> equivalent to <t> has been removed
    Found finite state machine <FSM_0> for signal <state>.
    -----------------------------------------------------------------------
    | States            | 12                                    |
    | Transitions       | 14                                    |
    | Inputs            | 2                                     |
    | Outputs           | 12                                    |
    | Clock             | clock (rising_edge)                   |
    | Reset             | reset (positive)                      |
    | Reset type        | asynchronous                          |
    | Reset State       | 000000000001                          |
    | Encoding          | automatic                             |
    | Implementation    | LUT                                   |
    -----------------------------------------------------------------------
    Found finite state machine <FSM_1> for signal <state_out>.
    -----------------------------------------------------------------------
    | States            | 5                                     |
    | Transitions       | 5                                     |
    | Inputs            | 0                                     |
    | Outputs           | 5                                     |
    | Clock             | clock (rising_edge)                   |
    | Reset             | reset (positive)                      |
    | Reset type        | asynchronous                          |
    | Reset State       | 00001                                 |
    | Encoding          | automatic                             |
    | Implementation    | LUT                                   |
    -----------------------------------------------------------------------
    Found 16-bit register for signal <plaintext_d>.
    Found 1-bit register for signal <ready_d>.
    Found 16-bit subtractor for signal <$n0003> created at line 297.
    Found 16-bit shifter logical right for signal <$n0005> created at line 303.
    Found 16-bit subtractor for signal <$n0006> created at line 298.
    Found 16-bit shifter logical right for signal <$n0008> created at line 307.
    Found 8-bit comparator less for signal <$n0014> created at line 314.
```

Found 16-bit adder for signal <$n0039> created at line 165.
Found 16-bit adder for signal <$n0040> created at line 167.
Found 16-bit adder for signal <$n0041>.
Found 16-bit adder for signal <$n0042>.
Found 16-bit adder for signal <$n0043>.
Found 16-bit adder for signal <$n0044>.
Found 16-bit adder for signal <$n0045>.
Found 16-bit adder for signal <$n0046>.
Found 16-bit adder for signal <$n0047>.
Found 16-bit adder for signal <$n0048>.
Found 16-bit adder for signal <$n0049>.
Found 16-bit adder for signal <$n0050>.
Found 16-bit adder for signal <$n0051>.
Found 16-bit adder for signal <$n0052>.
Found 16-bit adder for signal <$n0053>.
Found 16-bit adder for signal <$n0054>.
Found 16-bit adder for signal <$n0055>.
Found 16-bit adder for signal <$n0056>.
Found 16-bit adder for signal <$n0057>.
Found 16-bit adder for signal <$n0058>.
Found 16-bit adder for signal <$n0059>.
Found 16-bit adder for signal <$n0060>.
Found 16-bit adder for signal <$n0061>.
Found 16-bit adder for signal <$n0062>.
Found 16-bit adder for signal <$n0063>.
Found 16-bit adder for signal <$n0064>.
Found 16-bit adder for signal <$n0065>.
Found 16-bit adder for signal <$n0066>.
Found 16-bit adder for signal <$n0067>.
Found 16-bit adder for signal <$n0068>.
Found 16-bit adder for signal <$n0069>.
Found 16-bit adder for signal <$n0070>.
Found 16-bit adder for signal <$n0071>.
Found 16-bit adder for signal <$n0072>.
Found 16-bit adder for signal <$n0073>.
Found 16-bit adder for signal <$n0074>.
Found 16-bit adder for signal <$n0075>.
Found 16-bit adder for signal <$n0076>.
Found 16-bit adder for signal <$n0077>.
Found 16-bit adder for signal <$n0078>.
Found 16-bit adder for signal <$n0079>.
Found 16-bit adder for signal <$n0080>.
Found 7-bit adder for signal <$n0081> created at line 315.
Found 16-bit subtractor for signal <$n0082> created at line 244.
Found 16-bit subtractor for signal <$n0083> created at line 338.
Found 16-bit subtractor for signal <$n0084> created at line 245.

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    Found 16-bit subtractor for signal <$n0085> created at line 330.
    Found 16-bit xor2 for signal <$n0087> created at line 305.
    Found 16-bit xor2 for signal <$n0088> created at line 309.
    Found 16-bit register for signal <A>.
    Found 16-bit register for signal <A_final>.
    Found 16-bit register for signal <B>.
    Found 16-bit register for signal <B_final>.
    Found 16-bit register for signal <C>.
    Found 16-bit register for signal <C_final>.
    Found 7-bit register for signal <cnt>.
    Found 16-bit register for signal <D>.
    Found 16-bit register for signal <D_final>.
    Found 16-bit adder for signal <l<40:35>>.
    Found 16-bit adder for signal <l<33:25>>.
    Found 16-bit adder for signal <l<23:0>>.
    Found 16-bit adder for signal <s<43:1>>.
    Found 16-bit register for signal <t>.
    Found 16-bit register for signal <u>.
    Summary:
        inferred   2 Finite State Machine(s).
        inferred 184 D-type flip-flop(s).
        inferred 131 Adder/Subtracter(s).
        inferred   1 Comparator(s).
        inferred   2 Combinational logic shifter(s).
Unit <decryptor> synthesized.


=========================================================================
*                  Advanced HDL Synthesis                  *
=========================================================================

Advanced RAM inference ...
Advanced multiplier inference ...
Selecting encoding for FSM_1 ...
Optimizing FSM <FSM_1> on signal <state_out> with one-hot encoding.
Selecting encoding for FSM_0 ...
Optimizing FSM <FSM_0> on signal <state> with one-hot encoding.
Dynamic shift register inference ...

=========================================================================
HDL Synthesis Report

Macro Statistics
```

```
# FSMs                          : 2
# Adders/Subtractors            : 131
 16-bit subtractor              : 6
 7-bit adder                    : 1
 16-bit adder                   : 124
# Registers                     : 30
 1-bit register                 : 18
 16-bit register                : 11
 7-bit register                 : 1
# Comparators                   : 1
 8-bit comparator less          : 1
# Logic shifters                : 2
 16-bit shifter logical right   : 2
# Xors                          : 78
 16-bit xor3                    : 14
 16-bit xor2                    : 2
 1-bit xor2                     : 62

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=========================================================================
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*                      Low Level Synthesis                              *
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Optimizing unit <decryptor> ...

Optimizing unit <carrylook_ahead2> ...

Optimizing unit <full_adder> ...

Optimizing unit <multiplier> ...
Loading device for application Xst from file '3s400.nph' in environment C:/Xilinx.

Mapping all equations...
Building and optimizing final netlist ...
Found area constraint ratio of 100 (+ 5) on block decryptor, actual ratio is 45.
FlipFlop D_3 has been replicated 1 time(s)
FlipFlop B_3 has been replicated 1 time(s)
FlipFlop B_5 has been replicated 1 time(s)
FlipFlop B_1 has been replicated 1 time(s)
FlipFlop B_2 has been replicated 1 time(s)
FlipFlop D_4 has been replicated 1 time(s)
FlipFlop B_0 has been replicated 1 time(s)
```

FlipFlop D_0 has been replicated 1 time(s)
FlipFlop B_4 has been replicated 1 time(s)
FlipFlop B_0 has been replicated 1 time(s)
FlipFlop D_3 has been replicated 1 time(s)
FlipFlop B_1 has been replicated 1 time(s)
FlipFlop B_6 has been replicated 1 time(s)
FlipFlop D_1 has been replicated 1 time(s)
FlipFlop D_2 has been replicated 1 time(s)
FlipFlop D_5 has been replicated 1 time(s)
FlipFlop B_2 has been replicated 1 time(s)
FlipFlop B_3 has been replicated 1 time(s)

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* Final Report *
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Final Results
RTL Top Level Output File Name : decryptor.ngr
Top Level Output File Name : decryptor
Output Format : NGC
Optimization Goal : Speed
Keep Hierarchy : NO

Design Statistics
IOs : 52

Macro Statistics :
Registers : 13
1-bit register : 1
16-bit register : 11
7-bit register : 1
Logic shifters : 2
16-bit shifter logical right: 2
Adders/Subtractors : 131
16-bit adder : 124
16-bit subtractor : 6
7-bit adder : 1
Comparators : 1
8-bit comparator less : 1
Xors : 14
16-bit xor3 : 14

Cell Usage :
BELS : 6498
GND : 1

```
#      LUT1                : 681
#      LUT2                : 1358
#      LUT2_D               : 1
#      LUT2_L               : 16
#      LUT3                : 177
#      LUT3_D               : 8
#      LUT3_L               : 5
#      LUT4                : 382
#      LUT4_D               : 32
#      LUT4_L               : 12
#      MUXCY                : 1890
#      MUXF5                : 16
#      VCC                 : 1
#      XORCY                : 1918
# FlipFlops/Latches         : 219
#      FDC                 : 113
#      FDCE                : 8
#      FDE                 : 96
#      FDP                 : 1
#      FDPE                : 1
# Clock Buffers             : 1
#      BUFGP               : 1
# IO Buffers                : 51
#      IBUF                : 34
#      OBUF                : 17
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Device utilization summary:
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Selected Device : 3s400pq208-5

 Number of Slices:              1533  out of   3584    42%
 Number of Slice Flip Flops:     219  out of   7168     3%
 Number of 4 input LUTs:        2672  out of   7168    37%
 Number of bonded IOBs:           51  out of    141    36%
 Number of GCLKs:                  1  out of      8    12%


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TIMING REPORT

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
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FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

Clock Signal	Clock buffer(FF name)	Load
clock	BUFGP	219

Timing Summary:

Speed Grade: -5

Minimum period: 5.217ns (Maximum Frequency: 191.681MHz)
Minimum input arrival time before clock: 50.968ns
Maximum output required time after clock: 5.602ns
Maximum combinational path delay: No path found

Timing Detail:

All values displayed in nanoseconds (ns)

Timing constraint: Default period analysis for Clock 'clock'
Delay: 5.217ns (Levels of Logic = 14)
Source: B_0 (FF)
Destination: t_3 (FF)
Source Clock: clock rising
Destination Clock: clock rising

Data Path: B_0 to t_3

Cell:in->out	Gate fanout	Net Delay	Delay	Logical Name (Net Name)
FDC:C->Q	10	0.000	0.806	B_0 (B_0)
LUT2:I0->O	3	0.000	0.577	a1__n00331 (a1_P2<5>)
LUT4_D:I2->O	1	0.000	0.240	a1_w1_ca1_fa0_Mxor_sf_Xo<11>1 (a1_w1_ca1_su1<5>)
LUT4_D:I3->O	5	0.000	0.658	a1_w1_ca1_fa3_Mxor_sf_Xo<11>1 (a1_w1_ca1_su4<5>)
LUT4_D:I1->LO	1	0.000	0.100	a1_w1_ca1_fa6_Mxor_sf_Xo<13>1 (N45137)
LUT4:I2->O	1	0.000	0.240	a1_w1_ca2_Ker329351_SW0 (N44798)

```
    LUT4_D:I1->LO         1   0.000   0.100  a1_w1_ca2_Ker329351 (N45084)
    LUT4:I1->O            3   0.000   0.577  a1_w1_ca2__n01191 (a1_w1_ca2_c<9>)
    LUT4_L:I0->LO         1   0.000   0.100  a1_w1_ca2_Ker329401
(a1_w1_ca2_N32942)
    LUT4:I1->O            3   0.000   0.577  a1_w1_ca2__n01291 (a1_w1_ca2_c<11>)
    LUT4_L:I0->LO         1   0.000   0.100  a1_w1_ca2_Ker329451
(a1_w1_ca2_N32947)
    LUT4:I3->O            3   0.000   0.577  a1_w1_ca2__n01391 (a1_w1_ca2_c<13>)
    LUT4:I0->O            2   0.000   0.465  a1_w1_ca2_Ker329501 (a1_w1_ca2_N32952)
    LUT3_L:I0->LO         1   0.000   0.100  a1_w1_ca2_Mxor_s1<15>_Result_SW0
(N36838)
    LUT4_L:I2->LO         1   0.000   0.000  a1_w1_ca2_Mxor_s1<15>_Result
(product1<15>)
    FDE:D                     0.000          t_3
    ----------------------------------------
    Total                     5.217ns (0.000ns logic, 5.217ns route)
                                (0.0% logic, 100.0% route)

--------------------------------------------------------------------------------
Timing constraint: Default OFFSET IN BEFORE for Clock 'clock'
Offset:              50.968ns (Levels of Logic = 260)
  Source:            round_keys_d<0> (PAD)
  Destination:       C_1 (FF)
  Destination Clock: clock rising

  Data Path: round_keys_d<0> to C_1
                            Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
    IBUF:I->O             33   0.518   1.322  round_keys_d_0_IBUF
(round_keys_d_0_IBUF)
    LUT1:I0->O             1   0.000   0.000  Madd_l<0>_inst_lut2_841
(Madd_l<0>_inst_lut2_84)
    MUXCY:S->O             1   0.000   0.000  Madd_l<0>_inst_cy_83
(Madd_l<0>_inst_cy_83)
    MUXCY:CI->O            1   0.000   0.000  Madd_l<0>_inst_cy_84
(Madd_l<0>_inst_cy_84)
    MUXCY:CI->O            1   0.000   0.000  Madd_l<0>_inst_cy_85
(Madd_l<0>_inst_cy_85)
    XORCY:CI->O            3   0.000   0.577  Madd_l<0>_inst_sum_87 (l<0><3>)
    LUT1:I0->O             1   0.000   0.000  Madd_s<1>_inst_lut2_711
(Madd_s<1>_inst_lut2_71)
    MUXCY:S->O             1   0.000   0.000  Madd_s<1>_inst_cy_70
(Madd_s<1>_inst_cy_70)
    MUXCY:CI->O            1   0.000   0.000  Madd_s<1>_inst_cy_71
(Madd_s<1>_inst_cy_71)
```

```
    MUXCY:CI->O           1   0.000   0.000  Madd_s<1>_inst_cy_72
(Madd_s<1>_inst_cy_72)
    MUXCY:CI->O           1   0.000   0.000  Madd_s<1>_inst_cy_73
(Madd_s<1>_inst_cy_73)
    MUXCY:CI->O           1   0.000   0.000  Madd_s<1>_inst_cy_74
(Madd_s<1>_inst_cy_74)
    MUXCY:CI->O           1   0.000   0.000  Madd_s<1>_inst_cy_75
(Madd_s<1>_inst_cy_75)
    MUXCY:CI->O           1   0.000   0.000  Madd_s<1>_inst_cy_76
(Madd_s<1>_inst_cy_76)
    MUXCY:CI->O           1   0.000   0.000  Madd_s<1>_inst_cy_77
(Madd_s<1>_inst_cy_77)
    XORCY:CI->O           3   0.000   0.577  Madd_s<1>_inst_sum_79 (s<1><11>)
    LUT2:I0->O            1   0.000   0.000  Madd_l<1>_inst_lut2_501
(Madd_l<1>_inst_lut2_50)
    XORCY:LI->O           2   0.000   0.465  Madd_l<1>_inst_sum_50 (l<1><11>)
    LUT2:I1->O            1   0.000   0.000  Madd__n0041_inst_lut2_501
(Madd__n0041_inst_lut2_50)
    XORCY:LI->O           1   0.000   0.240  Madd__n0041_inst_sum_50 (_n0041<11>)
    LUT1:I0->O            1   0.000   0.000  Madd_s<2>_inst_lut2_661
(Madd_s<2>_inst_lut2_66)
    XORCY:LI->O           2   0.000   0.465  Madd_s<2>_inst_sum_66 (s<2><11>)
    LUT2:I0->O            1   0.000   0.000  Madd_l<2>_inst_lut2_501
(Madd_l<2>_inst_lut2_50)
    XORCY:LI->O           2   0.000   0.465  Madd_l<2>_inst_sum_50 (l<2><11>)
    LUT2:I1->O            1   0.000   0.000  Madd__n0042_inst_lut2_501
(Madd__n0042_inst_lut2_50)
    XORCY:LI->O           1   0.000   0.240  Madd__n0042_inst_sum_50 (_n0042<11>)
    LUT1:I0->O            1   0.000   0.000  Madd_s<3>_inst_lut2_661
(Madd_s<3>_inst_lut2_66)
    XORCY:LI->O           2   0.000   0.465  Madd_s<3>_inst_sum_66 (s<3><11>)
    LUT2:I0->O            1   0.000   0.000  Madd_l<3>_inst_lut2_501
(Madd_l<3>_inst_lut2_50)
    XORCY:LI->O           2   0.000   0.465  Madd_l<3>_inst_sum_50 (l<3><11>)
    LUT2:I1->O            1   0.000   0.000  Madd__n0043_inst_lut2_501
(Madd__n0043_inst_lut2_50)
    XORCY:LI->O           1   0.000   0.240  Madd__n0043_inst_sum_50 (_n0043<11>)
    LUT1:I0->O            1   0.000   0.000  Madd_s<4>_inst_lut2_661
(Madd_s<4>_inst_lut2_66)
    XORCY:LI->O           2   0.000   0.465  Madd_s<4>_inst_sum_66 (s<4><11>)
    LUT2:I0->O            1   0.000   0.000  Madd_l<4>_inst_lut2_501
(Madd_l<4>_inst_lut2_50)
    XORCY:LI->O           2   0.000   0.465  Madd_l<4>_inst_sum_50 (l<4><11>)
    LUT2:I1->O            1   0.000   0.000  Madd__n0044_inst_lut2_501
(Madd__n0044_inst_lut2_50)
    XORCY:LI->O           1   0.000   0.240  Madd__n0044_inst_sum_50 (_n0044<11>)
```

LUT1:I0->O 1 0.000 0.000 Madd_s<5>_inst_lut2_661
(Madd_s<5>_inst_lut2_66)
XORCY:LI->O 2 0.000 0.465 Madd_s<5>_inst_sum_66 (s<5><11>)
LUT2:I0->O 1 0.000 0.000 Madd_l<5>_inst_lut2_501
(Madd_l<5>_inst_lut2_50)
XORCY:LI->O 2 0.000 0.465 Madd_l<5>_inst_sum_50 (l<5><11>)
LUT2:I1->O 1 0.000 0.000 Madd__n0045_inst_lut2_501
(Madd__n0045_inst_lut2_50)
XORCY:LI->O 1 0.000 0.240 Madd__n0045_inst_sum_50 (_n0045<11>)
LUT1:I0->O 1 0.000 0.000 Madd_s<6>_inst_lut2_661
(Madd_s<6>_inst_lut2_66)
XORCY:LI->O 2 0.000 0.465 Madd_s<6>_inst_sum_66 (s<6><11>)
LUT2:I0->O 1 0.000 0.000 Madd_l<6>_inst_lut2_501
(Madd_l<6>_inst_lut2_50)
XORCY:LI->O 2 0.000 0.465 Madd_l<6>_inst_sum_50 (l<6><11>)
LUT2:I1->O 1 0.000 0.000 Madd__n0046_inst_lut2_501
(Madd__n0046_inst_lut2_50)
XORCY:LI->O 1 0.000 0.240 Madd__n0046_inst_sum_50 (_n0046<11>)
LUT1:I0->O 1 0.000 0.000 Madd_s<7>_inst_lut2_661
(Madd_s<7>_inst_lut2_66)
XORCY:LI->O 2 0.000 0.465 Madd_s<7>_inst_sum_66 (s<7><11>)
LUT2:I0->O 1 0.000 0.000 Madd_l<7>_inst_lut2_501
(Madd_l<7>_inst_lut2_50)
XORCY:LI->O 2 0.000 0.465 Madd_l<7>_inst_sum_50 (l<7><11>)
LUT2:I1->O 1 0.000 0.000 Madd__n0047_inst_lut2_501
(Madd__n0047_inst_lut2_50)
XORCY:LI->O 1 0.000 0.240 Madd__n0047_inst_sum_50 (_n0047<11>)
LUT1:I0->O 1 0.000 0.000 Madd_s<8>_inst_lut2_661
(Madd_s<8>_inst_lut2_66)
XORCY:LI->O 2 0.000 0.465 Madd_s<8>_inst_sum_66 (s<8><11>)
LUT2:I0->O 1 0.000 0.000 Madd_l<8>_inst_lut2_501
(Madd_l<8>_inst_lut2_50)
XORCY:LI->O 2 0.000 0.465 Madd_l<8>_inst_sum_50 (l<8><11>)
LUT2:I1->O 1 0.000 0.000 Madd__n0048_inst_lut2_501
(Madd__n0048_inst_lut2_50)
XORCY:LI->O 1 0.000 0.240 Madd__n0048_inst_sum_50 (_n0048<11>)
LUT1:I0->O 1 0.000 0.000 Madd_s<9>_inst_lut2_661
(Madd_s<9>_inst_lut2_66)
XORCY:LI->O 2 0.000 0.465 Madd_s<9>_inst_sum_66 (s<9><11>)
LUT2:I0->O 1 0.000 0.000 Madd_l<9>_inst_lut2_501
(Madd_l<9>_inst_lut2_50)
XORCY:LI->O 2 0.000 0.465 Madd_l<9>_inst_sum_50 (l<9><11>)
LUT2:I1->O 1 0.000 0.000 Madd__n0049_inst_lut2_501
(Madd__n0049_inst_lut2_50)
XORCY:LI->O 1 0.000 0.240 Madd__n0049_inst_sum_50 (_n0049<11>)

LUT1:I0->O 1 0.000 0.000 Madd_s<10>_inst_lut2_661 (Madd_s<10>_inst_lut2_66)
XORCY:LI->O 2 0.000 0.465 Madd_s<10>_inst_sum_66 (s<10><11>)
LUT2:I0->O 1 0.000 0.000 Madd_l<10>_inst_lut2_501 (Madd_l<10>_inst_lut2_50)
XORCY:LI->O 2 0.000 0.465 Madd_l<10>_inst_sum_50 (l<10><11>)
LUT2:I1->O 1 0.000 0.000 Madd__n0050_inst_lut2_501 (Madd__n0050_inst_lut2_50)
XORCY:LI->O 1 0.000 0.240 Madd__n0050_inst_sum_50 (_n0050<11>)
LUT1:I0->O 1 0.000 0.000 Madd_s<11>_inst_lut2_661 (Madd_s<11>_inst_lut2_66)
XORCY:LI->O 2 0.000 0.465 Madd_s<11>_inst_sum_66 (s<11><11>)
LUT2:I0->O 1 0.000 0.000 Madd_l<11>_inst_lut2_501 (Madd_l<11>_inst_lut2_50)
XORCY:LI->O 2 0.000 0.465 Madd_l<11>_inst_sum_50 (l<11><11>)
LUT2:I1->O 1 0.000 0.000 Madd__n0051_inst_lut2_501 (Madd__n0051_inst_lut2_50)
XORCY:LI->O 1 0.000 0.240 Madd__n0051_inst_sum_50 (_n0051<11>)
LUT1:I0->O 1 0.000 0.000 Madd_s<12>_inst_lut2_661 (Madd_s<12>_inst_lut2_66)
XORCY:LI->O 2 0.000 0.465 Madd_s<12>_inst_sum_66 (s<12><11>)
LUT2:I0->O 1 0.000 0.000 Madd_l<12>_inst_lut2_501 (Madd_l<12>_inst_lut2_50)
XORCY:LI->O 2 0.000 0.465 Madd_l<12>_inst_sum_50 (l<12><11>)
LUT2:I1->O 1 0.000 0.000 Madd__n0052_inst_lut2_501 (Madd__n0052_inst_lut2_50)
XORCY:LI->O 1 0.000 0.240 Madd__n0052_inst_sum_50 (_n0052<11>)
LUT1:I0->O 1 0.000 0.000 Madd_s<13>_inst_lut2_661 (Madd_s<13>_inst_lut2_66)
XORCY:LI->O 2 0.000 0.465 Madd_s<13>_inst_sum_66 (s<13><11>)
LUT2:I0->O 1 0.000 0.000 Madd_l<13>_inst_lut2_501 (Madd_l<13>_inst_lut2_50)
XORCY:LI->O 2 0.000 0.465 Madd_l<13>_inst_sum_50 (l<13><11>)
LUT2:I1->O 1 0.000 0.000 Madd__n0053_inst_lut2_501 (Madd__n0053_inst_lut2_50)
XORCY:LI->O 1 0.000 0.240 Madd__n0053_inst_sum_50 (_n0053<11>)
LUT1:I0->O 1 0.000 0.000 Madd_s<14>_inst_lut2_661 (Madd_s<14>_inst_lut2_66)
XORCY:LI->O 2 0.000 0.465 Madd_s<14>_inst_sum_66 (s<14><11>)
LUT2:I0->O 1 0.000 0.000 Madd_l<14>_inst_lut2_501 (Madd_l<14>_inst_lut2_50)
XORCY:LI->O 2 0.000 0.465 Madd_l<14>_inst_sum_50 (l<14><11>)
LUT2:I1->O 1 0.000 0.000 Madd__n0054_inst_lut2_501 (Madd__n0054_inst_lut2_50)
XORCY:LI->O 1 0.000 0.240 Madd__n0054_inst_sum_50 (_n0054<11>)

LUT1:I0->O 1 0.000 0.000 Madd_s<15>_inst_lut2_661
(Madd_s<15>_inst_lut2_66)
XORCY:LI->O 2 0.000 0.465 Madd_s<15>_inst_sum_66 (s<15><11>)
LUT2:I0->O 1 0.000 0.000 Madd_l<15>_inst_lut2_501
(Madd_l<15>_inst_lut2_50)
XORCY:LI->O 2 0.000 0.465 Madd_l<15>_inst_sum_50 (l<15><11>)
LUT2:I1->O 1 0.000 0.000 Madd__n0055_inst_lut2_501
(Madd__n0055_inst_lut2_50)
XORCY:LI->O 1 0.000 0.240 Madd__n0055_inst_sum_50 (_n0055<11>)
LUT1:I0->O 1 0.000 0.000 Madd_s<16>_inst_lut2_661
(Madd_s<16>_inst_lut2_66)
XORCY:LI->O 2 0.000 0.465 Madd_s<16>_inst_sum_66 (s<16><11>)
LUT2:I0->O 1 0.000 0.000 Madd_l<16>_inst_lut2_501
(Madd_l<16>_inst_lut2_50)
XORCY:LI->O 2 0.000 0.465 Madd_l<16>_inst_sum_50 (l<16><11>)
LUT2:I1->O 1 0.000 0.000 Madd__n0056_inst_lut2_501
(Madd__n0056_inst_lut2_50)
XORCY:LI->O 1 0.000 0.240 Madd__n0056_inst_sum_50 (_n0056<11>)
LUT1:I0->O 1 0.000 0.000 Madd_s<17>_inst_lut2_661
(Madd_s<17>_inst_lut2_66)
XORCY:LI->O 2 0.000 0.465 Madd_s<17>_inst_sum_66 (s<17><11>)
LUT2:I0->O 1 0.000 0.000 Madd_l<17>_inst_lut2_501
(Madd_l<17>_inst_lut2_50)
XORCY:LI->O 2 0.000 0.465 Madd_l<17>_inst_sum_50 (l<17><11>)
LUT2:I1->O 1 0.000 0.000 Madd__n0057_inst_lut2_501
(Madd__n0057_inst_lut2_50)
XORCY:LI->O 1 0.000 0.240 Madd__n0057_inst_sum_50 (_n0057<11>)
LUT1:I0->O 1 0.000 0.000 Madd_s<18>_inst_lut2_661
(Madd_s<18>_inst_lut2_66)
XORCY:LI->O 2 0.000 0.465 Madd_s<18>_inst_sum_66 (s<18><11>)
LUT2:I0->O 1 0.000 0.000 Madd_l<18>_inst_lut2_501
(Madd_l<18>_inst_lut2_50)
XORCY:LI->O 2 0.000 0.465 Madd_l<18>_inst_sum_50 (l<18><11>)
LUT2:I1->O 1 0.000 0.000 Madd__n0058_inst_lut2_501
(Madd__n0058_inst_lut2_50)
XORCY:LI->O 1 0.000 0.240 Madd__n0058_inst_sum_50 (_n0058<11>)
LUT1:I0->O 1 0.000 0.000 Madd_s<19>_inst_lut2_661
(Madd_s<19>_inst_lut2_66)
XORCY:LI->O 2 0.000 0.465 Madd_s<19>_inst_sum_66 (s<19><11>)
LUT2:I0->O 1 0.000 0.000 Madd_l<19>_inst_lut2_501
(Madd_l<19>_inst_lut2_50)
XORCY:LI->O 2 0.000 0.465 Madd_l<19>_inst_sum_50 (l<19><11>)
LUT2:I1->O 1 0.000 0.000 Madd__n0059_inst_lut2_501
(Madd__n0059_inst_lut2_50)
XORCY:LI->O 1 0.000 0.240 Madd__n0059_inst_sum_50 (_n0059<11>)

LUT1:I0->O 1 0.000 0.000 Madd_s<20>_inst_lut2_661
(Madd_s<20>_inst_lut2_66)
XORCY:LI->O 2 0.000 0.465 Madd_s<20>_inst_sum_66 (s<20><11>)
LUT2:I0->O 1 0.000 0.000 Madd_l<20>_inst_lut2_501
(Madd_l<20>_inst_lut2_50)
XORCY:LI->O 2 0.000 0.465 Madd_l<20>_inst_sum_50 (l<20><11>)
LUT2:I1->O 1 0.000 0.000 Madd__n0060_inst_lut2_501
(Madd__n0060_inst_lut2_50)
XORCY:LI->O 1 0.000 0.240 Madd__n0060_inst_sum_50 (_n0060<11>)
LUT1:I0->O 1 0.000 0.000 Madd_s<21>_inst_lut2_661
(Madd_s<21>_inst_lut2_66)
XORCY:LI->O 2 0.000 0.465 Madd_s<21>_inst_sum_66 (s<21><11>)
LUT2:I0->O 1 0.000 0.000 Madd_l<21>_inst_lut2_501
(Madd_l<21>_inst_lut2_50)
XORCY:LI->O 2 0.000 0.465 Madd_l<21>_inst_sum_50 (l<21><11>)
LUT2:I1->O 1 0.000 0.000 Madd__n0061_inst_lut2_501
(Madd__n0061_inst_lut2_50)
XORCY:LI->O 1 0.000 0.240 Madd__n0061_inst_sum_50 (_n0061<11>)
LUT1:I0->O 1 0.000 0.000 Madd_s<22>_inst_lut2_661
(Madd_s<22>_inst_lut2_66)
XORCY:LI->O 2 0.000 0.465 Madd_s<22>_inst_sum_66 (s<22><11>)
LUT2:I0->O 1 0.000 0.000 Madd_l<22>_inst_lut2_501
(Madd_l<22>_inst_lut2_50)
XORCY:LI->O 2 0.000 0.465 Madd_l<22>_inst_sum_50 (l<22><11>)
LUT2:I1->O 1 0.000 0.000 Madd__n0062_inst_lut2_501
(Madd__n0062_inst_lut2_50)
XORCY:LI->O 1 0.000 0.240 Madd__n0062_inst_sum_50 (_n0062<11>)
LUT1:I0->O 1 0.000 0.000 Madd_s<23>_inst_lut2_661
(Madd_s<23>_inst_lut2_66)
XORCY:LI->O 2 0.000 0.465 Madd_s<23>_inst_sum_66 (s<23><11>)
LUT2:I0->O 1 0.000 0.000 Madd_l<23>_inst_lut2_501
(Madd_l<23>_inst_lut2_50)
XORCY:LI->O 2 0.000 0.465 Madd_l<23>_inst_sum_50 (l<23><11>)
LUT2:I1->O 1 0.000 0.000 Madd__n0063_inst_lut2_501
(Madd__n0063_inst_lut2_50)
XORCY:LI->O 1 0.000 0.240 Madd__n0063_inst_sum_50 (_n0063<11>)
LUT1:I0->O 1 0.000 0.000 Madd_s<24>_inst_lut2_661
(Madd_s<24>_inst_lut2_66)
XORCY:LI->O 2 0.000 0.465 Madd_s<24>_inst_sum_66 (s<24><11>)
LUT2:I0->O 1 0.000 0.000 Madd_l<29>_inst_lut2_501
(Madd_l<29>_inst_lut2_50)
XORCY:LI->O 4 0.000 0.629 Madd_l<29>_inst_sum_50 (l<29><11>)
LUT2:I1->O 1 0.000 0.000 Madd__n0064_inst_lut2_501
(Madd__n0064_inst_lut2_50)
XORCY:LI->O 1 0.000 0.240 Madd__n0064_inst_sum_50 (_n0064<11>)

LUT1:I0->O 1 0.000 0.000 Madd_s<25>_inst_lut2_661 (Madd_s<25>_inst_lut2_66)
XORCY:LI->O 2 0.000 0.465 Madd_s<25>_inst_sum_66 (s<25><11>)
LUT2:I0->O 1 0.000 0.000 Madd_l<25>_inst_lut2_501 (Madd_l<25>_inst_lut2_50)
XORCY:LI->O 2 0.000 0.465 Madd_l<25>_inst_sum_50 (l<25><11>)
LUT2:I1->O 1 0.000 0.000 Madd__n0065_inst_lut2_501 (Madd__n0065_inst_lut2_50)
XORCY:LI->O 1 0.000 0.240 Madd__n0065_inst_sum_50 (_n0065<11>)
LUT1:I0->O 1 0.000 0.000 Madd_s<26>_inst_lut2_661 (Madd_s<26>_inst_lut2_66)
XORCY:LI->O 2 0.000 0.465 Madd_s<26>_inst_sum_66 (s<26><11>)
LUT2:I0->O 1 0.000 0.000 Madd_l<26>_inst_lut2_501 (Madd_l<26>_inst_lut2_50)
XORCY:LI->O 2 0.000 0.465 Madd_l<26>_inst_sum_50 (l<26><11>)
LUT2:I1->O 1 0.000 0.000 Madd__n0066_inst_lut2_501 (Madd__n0066_inst_lut2_50)
XORCY:LI->O 1 0.000 0.240 Madd__n0066_inst_sum_50 (_n0066<11>)
LUT1:I0->O 1 0.000 0.000 Madd_s<27>_inst_lut2_661 (Madd_s<27>_inst_lut2_66)
XORCY:LI->O 2 0.000 0.465 Madd_s<27>_inst_sum_66 (s<27><11>)
LUT2:I0->O 1 0.000 0.000 Madd_l<27>_inst_lut2_501 (Madd_l<27>_inst_lut2_50)
XORCY:LI->O 2 0.000 0.465 Madd_l<27>_inst_sum_50 (l<27><11>)
LUT2:I1->O 1 0.000 0.000 Madd__n0067_inst_lut2_501 (Madd__n0067_inst_lut2_50)
XORCY:LI->O 1 0.000 0.240 Madd__n0067_inst_sum_50 (_n0067<11>)
LUT1:I0->O 1 0.000 0.000 Madd_s<28>_inst_lut2_661 (Madd_s<28>_inst_lut2_66)
XORCY:LI->O 2 0.000 0.465 Madd_s<28>_inst_sum_66 (s<28><11>)
LUT2:I0->O 1 0.000 0.000 Madd_l<28>_inst_lut2_501 (Madd_l<28>_inst_lut2_50)
XORCY:LI->O 1 0.000 0.240 Madd_l<28>_inst_sum_50 (l<28><11>)
LUT2:I1->O 1 0.000 0.000 Madd__n0068_inst_lut2_501 (Madd__n0068_inst_lut2_50)
XORCY:LI->O 1 0.000 0.240 Madd__n0068_inst_sum_50 (_n0068<11>)
LUT1:I0->O 1 0.000 0.000 Madd_s<29>_inst_lut2_661 (Madd_s<29>_inst_lut2_66)
XORCY:LI->O 1 0.000 0.240 Madd_s<29>_inst_sum_66 (s<29><11>)
LUT2:I0->O 1 0.000 0.000 Madd__n0069_inst_lut2_501 (Madd__n0069_inst_lut2_50)
XORCY:LI->O 1 0.000 0.240 Madd__n0069_inst_sum_50 (_n0069<11>)
LUT1:I0->O 1 0.000 0.000 Madd_s<30>_inst_lut2_661 (Madd_s<30>_inst_lut2_66)
XORCY:LI->O 2 0.000 0.465 Madd_s<30>_inst_sum_66 (s<30><11>)

LUT2:I0->O 1 0.000 0.000 Madd_l<30>_inst_lut2_501 (Madd_l<30>_inst_lut2_50)
XORCY:LI->O 2 0.000 0.465 Madd_l<30>_inst_sum_50 (l<30><11>)
LUT2:I1->O 1 0.000 0.000 Madd__n0070_inst_lut2_501 (Madd__n0070_inst_lut2_50)
XORCY:LI->O 1 0.000 0.240 Madd__n0070_inst_sum_50 (_n0070<11>)
LUT1:I0->O 1 0.000 0.000 Madd_s<31>_inst_lut2_661 (Madd_s<31>_inst_lut2_66)
XORCY:LI->O 2 0.000 0.465 Madd_s<31>_inst_sum_66 (s<31><11>)
LUT2:I0->O 1 0.000 0.000 Madd_l<31>_inst_lut2_501 (Madd_l<31>_inst_lut2_50)
XORCY:LI->O 2 0.000 0.465 Madd_l<31>_inst_sum_50 (l<31><11>)
LUT2:I1->O 1 0.000 0.000 Madd__n0071_inst_lut2_501 (Madd__n0071_inst_lut2_50)
XORCY:LI->O 1 0.000 0.240 Madd__n0071_inst_sum_50 (_n0071<11>)
LUT1:I0->O 1 0.000 0.000 Madd_s<32>_inst_lut2_661 (Madd_s<32>_inst_lut2_66)
XORCY:LI->O 2 0.000 0.465 Madd_s<32>_inst_sum_66 (s<32><11>)
LUT2:I0->O 1 0.000 0.000 Madd_l<32>_inst_lut2_501 (Madd_l<32>_inst_lut2_50)
XORCY:LI->O 2 0.000 0.465 Madd_l<32>_inst_sum_50 (l<32><11>)
LUT2:I1->O 1 0.000 0.000 Madd__n0072_inst_lut2_501 (Madd__n0072_inst_lut2_50)
XORCY:LI->O 1 0.000 0.240 Madd__n0072_inst_sum_50 (_n0072<11>)
LUT1:I0->O 1 0.000 0.000 Madd_s<33>_inst_lut2_661 (Madd_s<33>_inst_lut2_66)
XORCY:LI->O 2 0.000 0.465 Madd_s<33>_inst_sum_66 (s<33><11>)
LUT2:I0->O 1 0.000 0.000 Madd_l<33>_inst_lut2_501 (Madd_l<33>_inst_lut2_50)
XORCY:LI->O 2 0.000 0.465 Madd_l<33>_inst_sum_50 (l<33><11>)
LUT2:I1->O 1 0.000 0.000 Madd__n0073_inst_lut2_501 (Madd__n0073_inst_lut2_50)
XORCY:LI->O 1 0.000 0.240 Madd__n0073_inst_sum_50 (_n0073<11>)
LUT1:I0->O 1 0.000 0.000 Madd_s<34>_inst_lut2_661 (Madd_s<34>_inst_lut2_66)
XORCY:LI->O 2 0.000 0.465 Madd_s<34>_inst_sum_66 (s<34><11>)
LUT2:I0->O 1 0.000 0.000 Madd_l<39>_inst_lut2_501 (Madd_l<39>_inst_lut2_50)
XORCY:LI->O 4 0.000 0.629 Madd_l<39>_inst_sum_50 (l<39><11>)
LUT2:I1->O 1 0.000 0.000 Madd__n0074_inst_lut2_501 (Madd__n0074_inst_lut2_50)
XORCY:LI->O 1 0.000 0.240 Madd__n0074_inst_sum_50 (_n0074<11>)
LUT1:I0->O 1 0.000 0.000 Madd_s<35>_inst_lut2_661 (Madd_s<35>_inst_lut2_66)
XORCY:LI->O 2 0.000 0.465 Madd_s<35>_inst_sum_66 (s<35><11>)

LUT2:I0->O 1 0.000 0.000 Madd_l<35>_inst_lut2_501 (Madd_l<35>_inst_lut2_50)
XORCY:LI->O 2 0.000 0.465 Madd_l<35>_inst_sum_50 (l<35><11>)
LUT2:I1->O 1 0.000 0.000 Madd__n0075_inst_lut2_501 (Madd__n0075_inst_lut2_50)
XORCY:LI->O 1 0.000 0.240 Madd__n0075_inst_sum_50 (_n0075<11>)
LUT1:I0->O 1 0.000 0.000 Madd_s<36>_inst_lut2_661 (Madd_s<36>_inst_lut2_66)
XORCY:LI->O 2 0.000 0.465 Madd_s<36>_inst_sum_66 (s<36><11>)
LUT2:I0->O 1 0.000 0.000 Madd_l<36>_inst_lut2_501 (Madd_l<36>_inst_lut2_50)
XORCY:LI->O 2 0.000 0.465 Madd_l<36>_inst_sum_50 (l<36><11>)
LUT2:I1->O 1 0.000 0.000 Madd__n0076_inst_lut2_501 (Madd__n0076_inst_lut2_50)
XORCY:LI->O 1 0.000 0.240 Madd__n0076_inst_sum_50 (_n0076<11>)
LUT1:I0->O 1 0.000 0.000 Madd_s<37>_inst_lut2_661 (Madd_s<37>_inst_lut2_66)
XORCY:LI->O 2 0.000 0.465 Madd_s<37>_inst_sum_66 (s<37><11>)
LUT2:I0->O 1 0.000 0.000 Madd_l<37>_inst_lut2_501 (Madd_l<37>_inst_lut2_50)
XORCY:LI->O 2 0.000 0.465 Madd_l<37>_inst_sum_50 (l<37><11>)
LUT2:I1->O 1 0.000 0.000 Madd__n0077_inst_lut2_501 (Madd__n0077_inst_lut2_50)
XORCY:LI->O 1 0.000 0.240 Madd__n0077_inst_sum_50 (_n0077<11>)
LUT1:I0->O 1 0.000 0.000 Madd_s<38>_inst_lut2_661 (Madd_s<38>_inst_lut2_66)
XORCY:LI->O 2 0.000 0.465 Madd_s<38>_inst_sum_66 (s<38><11>)
LUT2:I0->O 1 0.000 0.000 Madd_l<38>_inst_lut2_501 (Madd_l<38>_inst_lut2_50)
XORCY:LI->O 1 0.000 0.240 Madd_l<38>_inst_sum_50 (l<38><11>)
LUT2:I1->O 1 0.000 0.000 Madd__n0078_inst_lut2_501 (Madd__n0078_inst_lut2_50)
XORCY:LI->O 1 0.000 0.240 Madd__n0078_inst_sum_50 (_n0078<11>)
LUT1:I0->O 1 0.000 0.000 Madd_s<39>_inst_lut2_661 (Madd_s<39>_inst_lut2_66)
XORCY:LI->O 1 0.000 0.240 Madd_s<39>_inst_sum_66 (s<39><11>)
LUT2:I0->O 1 0.000 0.000 Madd__n0079_inst_lut2_501 (Madd__n0079_inst_lut2_50)
XORCY:LI->O 1 0.000 0.240 Madd__n0079_inst_sum_50 (_n0079<11>)
LUT1:I0->O 1 0.000 0.000 Madd_s<40>_inst_lut2_661 (Madd_s<40>_inst_lut2_66)
XORCY:LI->O 3 0.000 0.577 Madd_s<40>_inst_sum_66 (s<40><11>)
LUT2:I0->O 1 0.000 0.000 Madd_l<40>_inst_lut2_501 (Madd_l<40>_inst_lut2_50)
XORCY:LI->O 1 0.000 0.240 Madd_l<40>_inst_sum_50 (l<40><11>)

```
    LUT2:I1->O            1   0.000   0.000  Madd__n0039_inst_lut2_501
(Madd__n0039_inst_lut2_50)
    XORCY:LI->O           2   0.000   0.465  Madd__n0039_inst_sum_50 (l<41><11>)
    LUT1:I0->O            1   0.000   0.000  Madd_s<41>_inst_lut2_661
(Madd_s<41>_inst_lut2_66)
    XORCY:LI->O           2   0.000   0.465  Madd_s<41>_inst_sum_66 (s<41><11>)
    LUT2:I1->O            1   0.000   0.000  Msub__n0006_inst_lut2_111
(Msub__n0006_inst_lut2_11)
    XORCY:LI->O           3   0.000   0.577  Msub__n0006_inst_sum_11 (_n0006<11>)
    LUT3:I0->O            3   0.000   0.577  Ker295971 (N29599)
    LUT3:I2->O            2   0.000   0.465  Mshift__n0008_Sh<9>
(Mshift__n0008_Sh<9>)
    LUT3:I2->O            2   0.000   0.465  Ker297931 (N29795)
    LUT3:I1->O            1   0.000   0.240  Mshift__n0008_Result<1>37 (_n0265<17>)
    LUT3:I0->O            1   0.000   0.240  _n0035<1>17 (CHOICE1055)
    LUT4:I0->O            1   0.000   0.000  _n0035<1>39 (_n0035<1>)
    FDC:D                 0.000          C_1
    ----------------------------------------
    Total                    50.968ns (0.518ns logic, 50.450ns route)
                                 (1.0% logic, 99.0% route)

--------------------------------------------------------------------------------
Timing constraint: Default OFFSET OUT AFTER for Clock 'clock'
Offset:              5.602ns (Levels of Logic = 1)
  Source:            ready_d (FF)
  Destination:       ready_d (PAD)
  Source Clock:      clock rising

  Data Path: ready_d to ready_d
                            Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
    FDC:C->Q              2   0.000   0.465  ready_d (ready_d_OBUF)
    OBUF:I->O                 5.137          ready_d_OBUF (ready_d)
    ----------------------------------------
    Total                    5.602ns (5.137ns logic, 0.465ns route)
                                 (91.7% logic, 8.3% route)

==========================================================================
==========
CPU : 35.13 / 36.26 s | Elapsed : 35.00 / 36.00 s

-->

Total memory usage is 98908 kilobytes
```