The Huffman decoder Core

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Introduction:

In the follow document a decoder is described for baseline jpeg pictures. The code is written for real time video streaming. Some efforts are made in optimization for speed and dynamic huffman table and dynamic quantization tables load.

Language: VHDL

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Generally explanation:

This core analyses jpeg baseline makers is the incoming data stream. A state machine switch in the correct state. The incoming picture header information is analyzed and is applied in the decoding process. All tables are dynamic.

Actual are this:

0xFFD8	Start of image	
0xFFE0	App0 application segment	
0xFFDB	define quantization table	
0xFFC0	SOF0 Baseline DCT	
0xFFC4	define huffman table	
0xFFDA	start of scan	
0xFFD9	End of image	

Interface: entity huffman decoder is port(clk :in std logic; --interface data input :in std logic; --write wr : in unsigned (7 downto 0); --data jpeg stream input data in : out std logic:='1'; --write enable wr en --interface data out output valid : buffer std logic; --use it as write signal in the follow IDCT : out signed (15 downto 0); --decoded and dequantized coefficient data out : buffer std logic:='0'; --the next data is the last coefficient of block next eob --all higher zigzag coeficients are zero : out std logic:='0'; --start of picture sop : out std logic:='0'; --end of picture eop : out unsigned (3 downto 0); -- number of consecutive zeros before the next zrl --coefficient decoder enable : in std logic);

end huffman decoder;

first picture:

header information

- quantization tables
- huffman tables

Pixel information in the stream: sop (start of picture) goes high

> switch to the valid table decode and dequantizered output the value in zigzag order

eop (end of picture) goes high

second picture:

header information

- quantization tables
- huffman tables

Pixel information in the stream: sop (start of picture) goes high

> switch to the valid table decode and dequantizered output the value in zigzag order

eop (end of picture) goes high

Internal FSM state	Output Interface sop data_out[15:0] output_valid zrl[3:0] next_eob	Signals Input Interface clk data_in[7:0] wr_en wr
app0dqt_acti+dqt_ac		Waves
<mark>/dqt_acti+_dqt_acti+++++++++++++++++++++++++++++++++++</mark>		2 us 3 us
sos scan		
Жаррб Д		6 us 7 us
(dqt_acti+) 🗘 🕂		=====================================
:+ <mark>dqt_acti+ + + + + + (+ +) + (d+ + + sos_sca</mark> n		9 us 10 us
		11 us 12 us
)eo i		