GRIVA BASIC version 1.2

Document version A

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Short description what is on board, with real pictures.

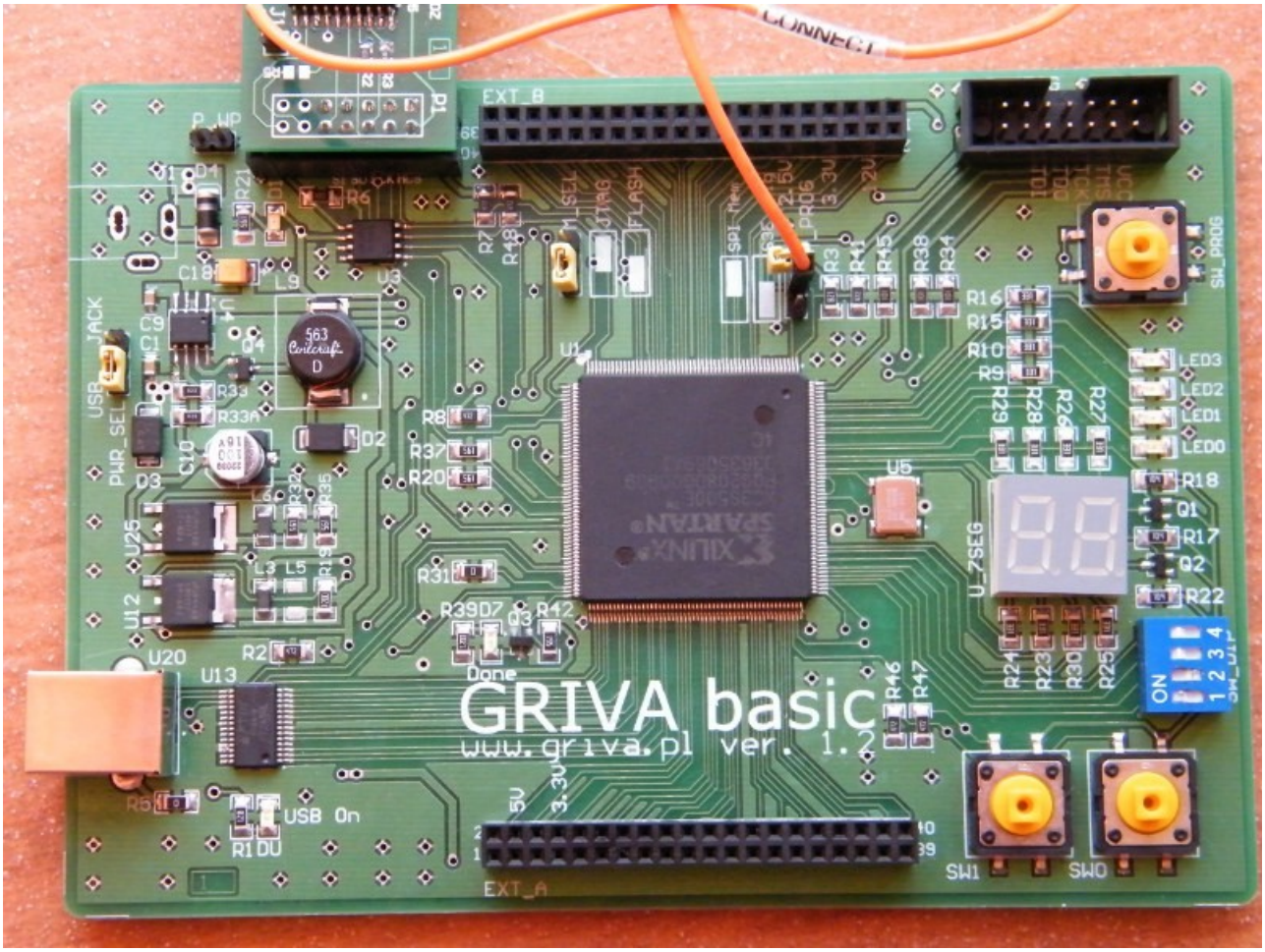

Figure 1. - Griva BASIC 1.2 - Top view

- **FPGA Xilinx Spartan3E XS3S500E-PQG208-4C (there is possibility to use smaller FPGA in the same package XC3S250E)**

500 000 system gates, 1 164 Configurable Logic Blocks, 360Kb Block RAM, 20 Multiplier Blocks, 4 Digital Clock Manager (DCM) Blocks. More details you can find in datasheet on Xilinx website : http://www.xilinx.com/support/documentation/data_sheets/ds312.pdf

Figure 2. - Xilinx FPGA Spartan 3E 500E - PQFP208Figure 3. - FT245R

- **USB interface**

From www.ftdichip.com website : "The FT232R is a USB to serial UART interface with optional clock generator output, and the new FTDIChip-ID™ security dongle feature. In addition, asynchronous and synchronous bit bang interface modes are available. USB to serial designs using the FT232R have been further simplified by fully integrating the external EEPROM, clock circuit and USB resistors onto the device." http://www.ftdichip.com/Products/ICs/FT232R.htm. About FT245RL "The FT245R is a USB to parallel FIFO interface, with the new FTDIChip-ID™ security dongle feature. In addition, asynchronous and synchronous bit bang interface modes are available. USB to parallel designs using the FT245R have been further simplified by fully integrating the external EEPROM, clock circuit and USB resistors onto the device."

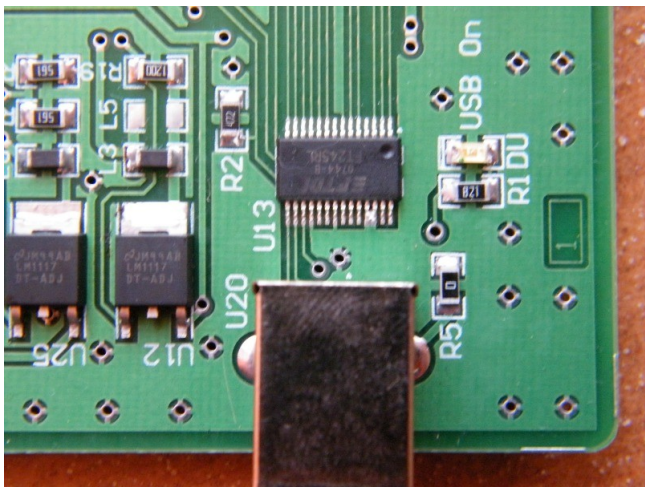

Figure 3. - USB FT245R

- **Atmel AT45DB041D**

Atmel AT45DB041D - 4Mbit SPI Flash memory to store bitstream for FPGA and there is also a free space for user data. More data you can find on Atmel website: http://www.atmel.com/atmel/acrobat/doc1938.pdf

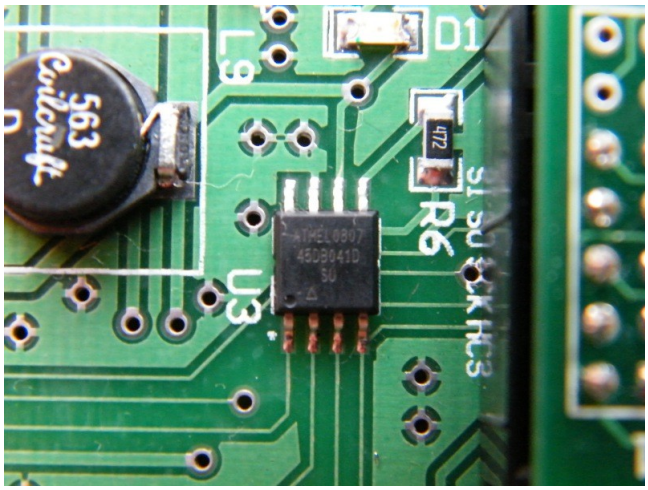

Figure 4. - SPI Flash memory

- **Double 7 segment and LEDs**

Double 7 segment LED is muxed by 2 pMOSFET transisotrs. Four red LEDs are direct through resistors connected to FPGA IO.

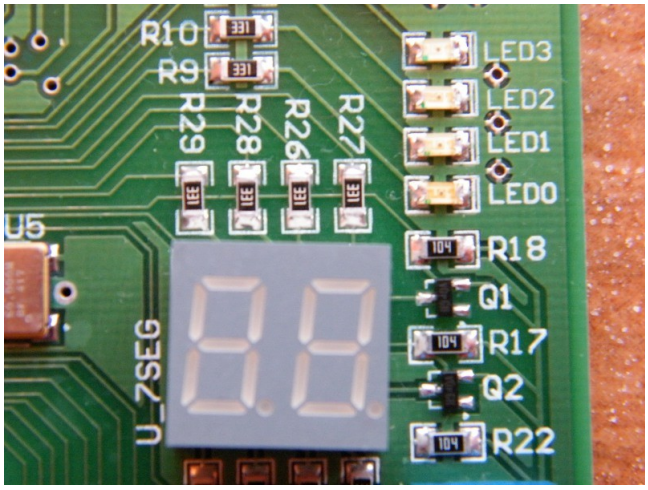

Figure 4. - LEDs and 7Seg

- **DIP switch and Buttons.**

DIP switch and buttons are direct connected to FPGA IO. They are both active high.

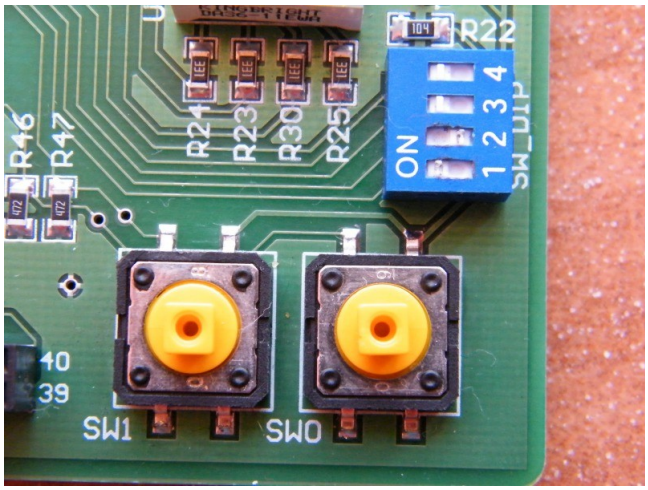

Figure 5. - DIP switch and 2 buttons

- **JTAG header**

JTAG header is compatible with all XILINX programmers and 3rd party with <3.3V interfaces.
Note: Spartan 3E does NOT allow to use LPT programmers with 74HC125 buffers. PROG button triggers reload FPGA configuration.

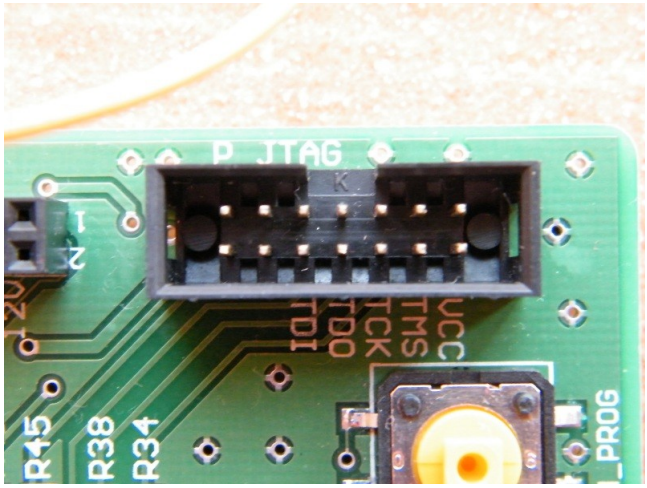

Figure 6. - JTAG header and PROG button

- **Header used to load FPGA configuration to Atmel SPI memory**

Header is used to load FPGA configuration using USB Griva Programmer to FPGA.

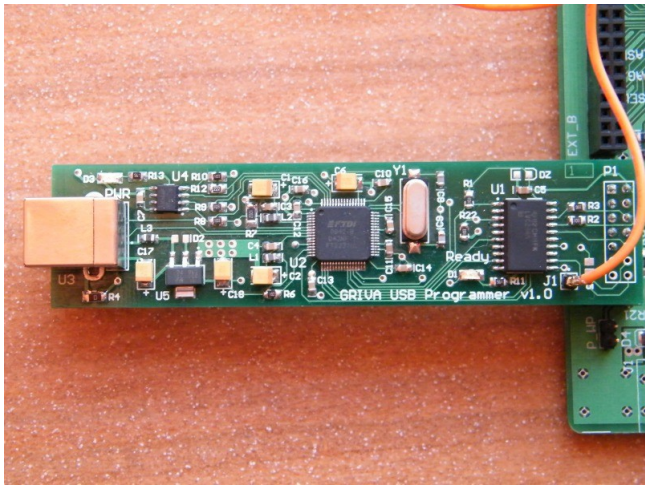

Figure 7. - Griva Programmer

- **Generator 50MHz**

It is 3v3 volt oscillator with 50ppm stability, connected directly to FPGA IOCLK pin.

Figure 8. 50MHz oscillator

- **Power supplies**

Input supply can be delivered by USB connector or standard JACK connector. Source is choosed by jumper PWR_SEL. Main 3.3V supply comes from DC/DC (chip MAX1626, inductor 56uH, diode 40V/1A MBR), supply 2.5V and 1.2V comes from LM1117-ADJ.

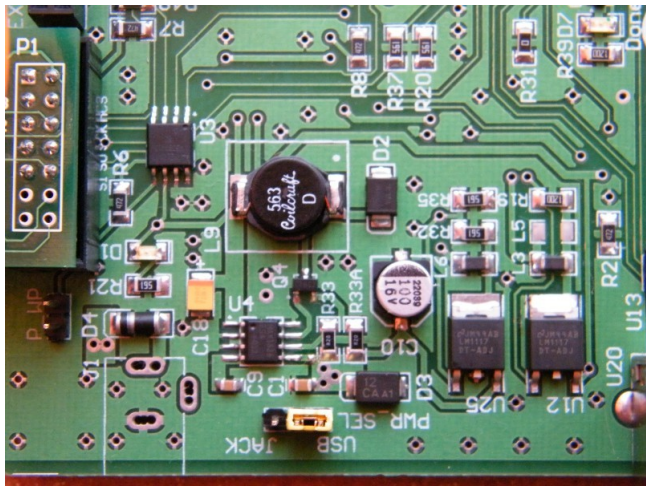

Figure 9. - DC/DC circuit and LDOs

- **GPIO headers**

There are 2 headers 2x20. Every header contains FPGA IOs (2 of them are GCLK), 3.3v, 5v and GND pins.

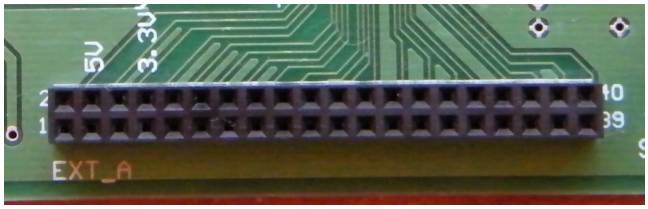

Figure 10. - GPIO header

- **M select**

That jumper controlls if bitstream will be loaded using JTAG interface or SPI mem/Griva Programmer.

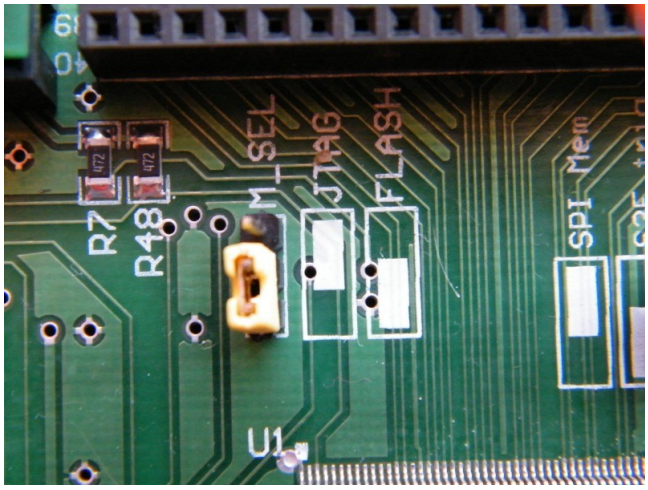

Figure 11. - M_SEL header