The double error correcting (DEC) BCH encoder / decoder IP cores.

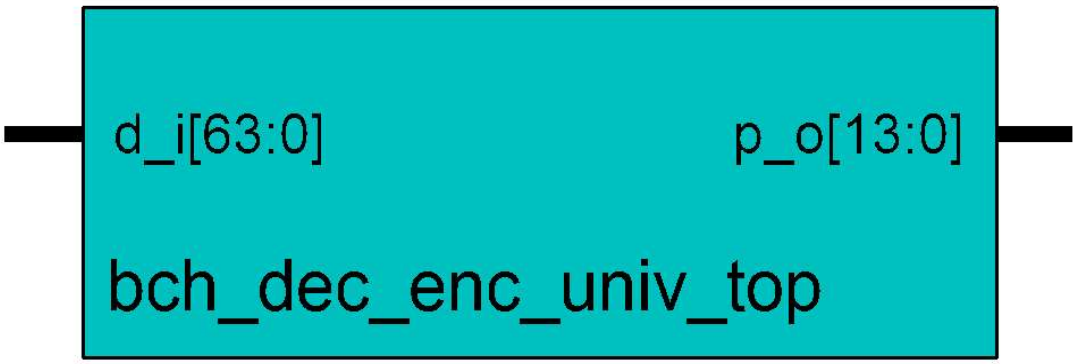
Features :

- allows to correct up to 2 errors.
- supports 16/32/64/128 bit memories (typical memory word sizes).
- operates on complete memory words in a single cycle.
- pure combinational logic design.

Memory word size	*Num. of ECC bits*
16	10
32	12
64	14
128	16

1 . BCH DEC encoder

Figure 1: BCH DEC encoder IP core.



1.1 BCH DEC encoder parameters

Name	*Allowable range*	*Description*
P_D_WIDTH	1... 239	Specifies the width of the data bus. Standard values are : 16/32/64/128

1.2 BCH DEC encoder I/O Signals

Name	*Direction*	*Width*	*Description*
d_i	In	P_D_WIDTH	Data input
p_o	Out	10 if P_D_WIDTH <= 21, 12 if 21 < P_D_WIDTH < = 51, 14 if 51 < P_D_WIDTH < = 113, 16 if 113 < P_D_WIDTH < = 239.	ECC output

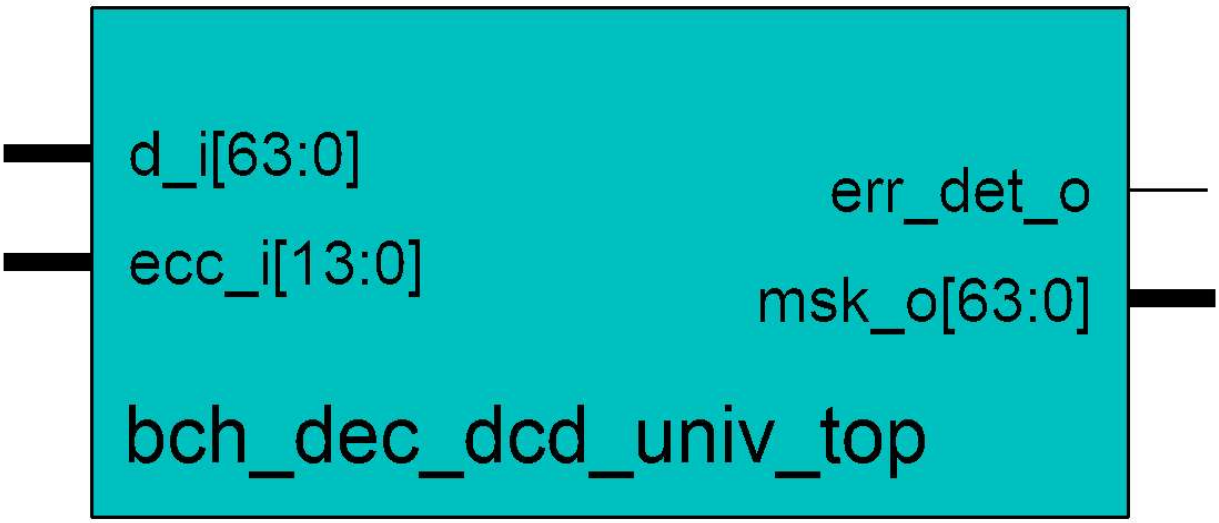
1.3. BCH DEC encoder synthesis results

P_D_WIDTH	*Number of occupied LUTs*	*Notes*
16	22	1
32	48	1
64	94	1
128	200	1

Notes:
1 – Xilinx XC3S5000

2 . BCH DEC decoder

Figure 2: BCH DEC Decoder IP core.



2.1 1.1 BCH DEC decoder parameters

Name	*Allowable range*	*Description*
P_D_WIDTH	1... 239	Specifies the width of the data bus. Standard values are : 16/32/64/128

2.2 1.2 BCH DEC decoder I/O Signals

Name	*Direction*	*Width*	*Description*
d_i	In	P_D_WIDTH	Data input
ecc_i	In	10 if P_D_WIDTH <= 21, 12 if 21 < P_D_WIDTH < = 51, 14 if 51 < P_D_WIDTH < = 113, 16 if 113 < P_D_WIDTH < = 239.	ECC input
msk_0		P_D_WIDTH	Error mask (should be XORed with the read data)
err_det_o	Out	1	Error(s) detected

1.3. BCH DEC decoder synthesis results

P_D_WIDTH	*Number of occupied LUTs*	*Notes*
16	613	1
32	2357	1
64	8986	1
128	39385	1

Notes:
1 – Xilinx XC3S5000

3. Revision history

Revision	***Author***	***Date***
0.1 (Initial)	Ruslan Lepetenok	