“General-purpose pulse-processing algorithm”

Users guide for SIS3302

v 1.0

General notes:

- registers, responsible for the general configuration of the SIS3302 module and memory mapping are preserved (see the original manual of the SIS3302 SADC)
- the feature-extraction firmware was tested for sampling frequency of 50 MHz and below
- in order to update parameters of the feature-extraction algorithm with the current values of the registers, the **program** bit of the **Algorithm-control register** has to be flipped (sequentially writing 1 and 0 into the register bit)
- Extra registers are introduced for each data-handling FPGA, therefore the address offsets, mentioned in this document, have to be combined with a group-offset (one of the following: 0x01000000, 0x02000000, 0x02800000, 0x03000000 or 0x03800000; see the manual of the standard firmware of the SIS3302 module)
- External LEMO connectors “start sampling” and “stop sampling” should be connected to the stop and start acquisition signals of the feature-extraction algorithm. However, for the current firmware-version this does not work.

Extra registers:

- **0x04**: Algorithm-control register

Bits	Meaning	Effected ADC	Read/Write
0	–	–	–
1	–	–	–
2	**start acquisition**	1/2	R/W
3	**stop acquisition**	1/2	R/W
4-7	output selection	1/2	R/W
8	invert ADC data	1/2	R/W
9	enable base-line follower	1/2	R/W
10	enable feature-extraction	1	R/W
11	enable feature-extraction	2	R/W
12	fraction value ½ or ¼ (CFT filter)	1/2	R/W
13	**program parameters**	1/2	R/W
14	bypass MWD-I filter	1/2	R/W
15	bypass MWD-II filter	1/2	R/W
16-31	–	–	–

Output-selection values

Value	Meaning	Value	Meaning
0	Echo mode (SADC data)	6	CF filter output
1	Combined output of MWD-I and MWD-II filters	7	MA output
2	Baseline value	9	Event detection
3	Baseline-subtracted signal	**15**	**Feature-extraction mode**

- **0x08** (bits 31:0, ADC 1/2): Decay-correction value τ for the MWD-I filter
  - Needs to be longer, in order of 10^3 sampling-clock cycles
  - The register value (integer) should be pre-calculated as: $2^{20+pMWD}/(\tau$ (samples)), where pMWD is the value of the MWD-I power register (0x48)

- **0x0C** (bits 31:0, ADC 1/2): Decay-correction value τ for the MWD-II filter
  - Needs to be shorter, in order of few sampling-clock cycles
  - The register value (integer) should be pre-calculated as: $2^{20}/(\tau$ (samples))

- **0x40** (bits 31:0, ADC 1/2): Buffer size
  - defines the memory size in short words for output of evens

- **0x44** (bits 15:0, ADC 1/2): Triggering threshold

- **0x48** (bits 15:0, ADC 1/2): Length of the MWD-I filter (MWD-I power)
  - values are given as a power of 2; possible values are: 3, 4, 5 and 6, which correspond to the length of 8, 16, 32 and 64 samples, respectively

- **0x4C** (bits 15:0, ADC 1/2): Length of the Constant Fraction filter
  - values are given as a power of 2; possible values are: 2, 3, 4, 5 and 6, which correspond to the length of 4, 8, 16, 32 and 64 samples, respectively

- **0x50** (bits 15:0, ADC 1/2): Length of the MA filter
  - values are given as a power of 2; possible values are: 2, 3, 4, 5 and 6, which correspond to the length of 4, 8, 16, 32 and 64 samples, respectively

- **0x54** (bits 15:0, ADC 1/2): Length of the base-line inhibit signal
  - possible values are in a range of 0..255
  - This value should be larger that the width of the pulse (in samples), after filtering

- **0x58** (bits 15:0, ADC 1/2): Length of the event-detection inhibit signal
  - possible values are in a range of 0..255

- **0x5C** (bits 15:0, ADC 1/2): Length of the base-line averaging
  - values are given as a power of 2; possible values are in a range of 2..9, which correspond to the length between 4 and 512 samples, respectively (default 512 samples)

- **0x94** (bits 15:0, ADC 1, Read only): Write count ADC1 – informs how many short words with hit data were stored by the feature-extraction algorithm in the memory. This number is always proportional to 8 (length of the data, related to one hit)

- **0x98** (bits 15:0, ADC 2, Read only): Write count ADC2 – informs how many short words with hit data were stored by the feature-extraction algorithm in the memory. This number is always proportional to 8 (length of the data, related to one hit)

Event structure:

Short word #	Bits 15:8	Bits 7:0		Short word #	Bits 15:8	Bits 7:0
1	0xAA	0xAA		5	T (15:8)	T (7:0)
2	T (63:56)	T (55:48)		6	F(10:8)	F(7:0)
3	T (47:40)	T (39:32)		7	E(15:8)	E(7:0)
4	T (31:24)	T (23:16)		8	0x55	0x55

- **T** and **F** – an integer and fractional parts of a time stamp (number of SADC clock cycles, starting from the start acquisition signal):

  time stamp = T + F/2^{11}
- **E** – an amplitude of the detected pulse

Example of usage (operation sequence):

- Initialization:
  - SIS3302 standard registers:
    - Acquisition Control Status (0x010) = 0x1100 // operating at 50 MHz
    - Offset DAC values
  - Algorithm-control register
  - Length of the MWD-I filter (MWD-I power)
  - Decay-correction value τ for the MWD-I filter
  - Decay-correction value τ for the MWD-II filter
  - Length of the Constant Fraction filter
  - Length of the MA filter
  - Triggering threshold
  - Length of the base-line inhibit signal
  - Length of the event-detection inhibit signal
  - **Flip "program parameters" bit of the Algorithm-control register** (actually programs the feature-extraction block, using values, stored in the registers)
- Start acquisition: flip "**start acquisition**" bit of the Algorithm-control register
- Stop acquisition and readout sequence:
  - flip "**stop acquisition**" bit of the Algorithm-control register
  - Check content of the "Write count ADC" register and read out the corresponding number of short words from the buffer memory, starting from the beginning of the buffer.
    - The memory buffer operates in the "wrapping" mode. Once the end of the buffer is reached, the new data will be written to the beginning of the buffer, overriding the old data. In this case,the Write count ADC value is larger than the value of the "Buffer size" register.