FlexyICE II
DATA SHEET

Artec Group OÜ, Teaduspargi 6/1,
Tallinn, 11313 Estonia, European Union
Tel: (+372) 6718 550
Fax: (+372) 6718 555
www.artecgroup.com
info@artecgroup.com

FPGA based hardware debugger platform

Ver. 23

FlexyICE II Version 23 Features:

- Supports LPC memory read (can be disabled), LPC Firmware Hub memory read and IO write for POST Code capture
- Post code peek mode (LPC reads from FlexyICE II are disabled)
- Post code logger (sends all postcodes to USB serial port as hexadecimal bytes in ASCII)
- UART 16550 with selectable base address
- 4 segment LED display for debug purposes
- 8 LEDs near GPIO pins debug purpose writeable on IO address 0x84
- EEPROM 1024 bits for non-volatile settings
- 2x16bit GPIO headers (with optional tailored development for debug purposes)
- Automatically selected voltage source either USB or LPC bus
- 8 rotary switch selectable boot images for LPC (4 flash images, 4 PSRAM images
- UltraCap for short-term PSRAM image retention (up to 2 hours)
- Third party free USB drivers for
    - Windows (98,2000,ME,XP)
    - Linux 2.4 and greater

Included:

- FlexyICE II
- Python based software with source (Linux and Windows supported)
- USB cable
- LPC cable

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FlexyICE II version

FlexyICE II version number can be seen on the postcode byte if reset button is held down while USB cable is connected or FlexyICE II is connected to a host system by LPC bus. This document deals with FlexyICE II version 23.

Additions from FlexyICE to FlexyICE II:

- LPC Firmware Hub read capability and disable jumper to disable the new mode.
- Post code peek mode (post code IO writes are shown but read requests are ignored)

Performance estimates for FlexyICE II:

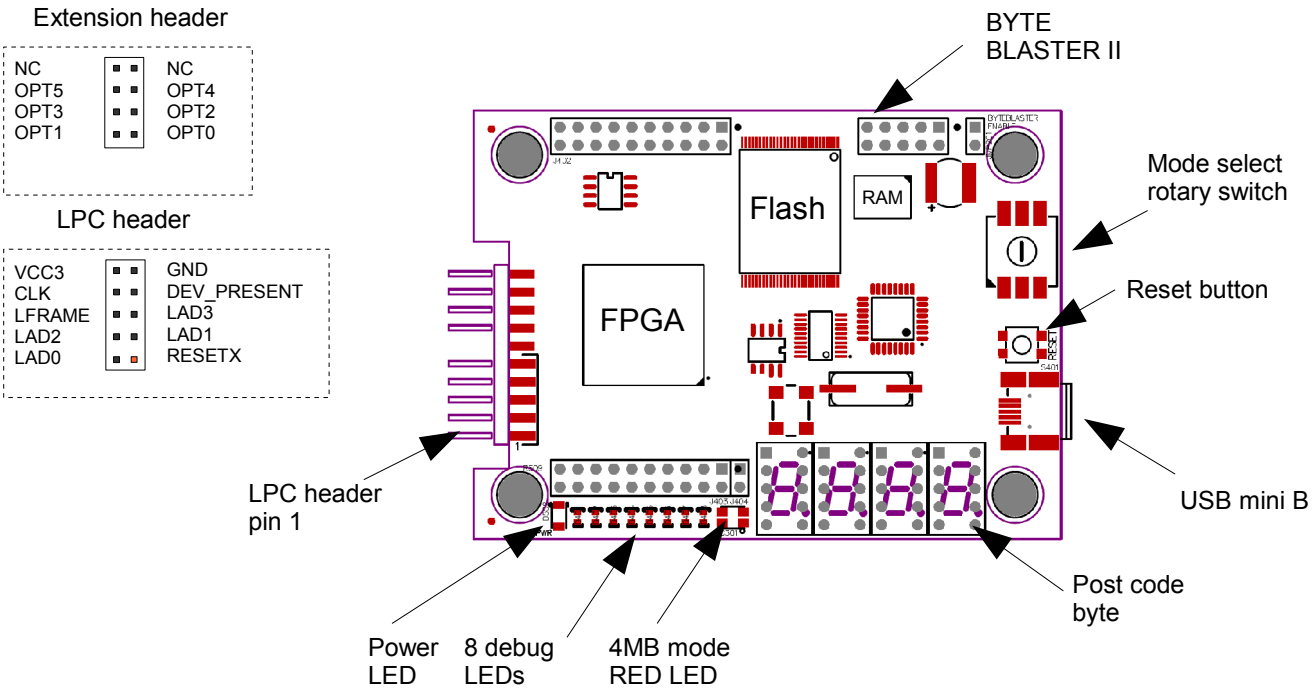
(PSRAM area Linux 4096K write time 4s, read time 10s)

(Flash area Linux 4096K write time 59s includes erase time 27s, read time 10s)

(PSRAM area Windows XP 4096K write time 7, read time 7s)

(Flash area Windows XP 4096K write time 2m37s includes erase time 27s , read time 7s)

FlexyICE II PCB interfaces



Drawing 1: PCB top layout

LPC

LPC header provides 7 IO pins used for LPC signal (see FlexyICE II schematic) and DEV_PRESENT signal driven low to indicate that FlexyICE II is connected. By default 1MB of flash can be accessed over LPC bus (highest MB of 4 MB available in each mode configuration). This can be changed by IO command to full 4 MB (or forced to 4M with jumper setting).

LPC IO write to address 0x0088 data 0xF4 turn on 4MB addressing

LPC IO write to address 0x0088 data 0xF1 turn off 4MB addressing

LPC IO write to address 0x0080 will be displayed on Post code byte

GPIO and LEDS

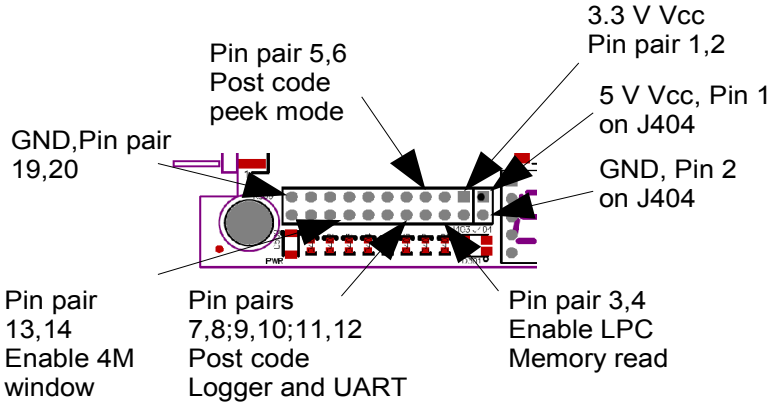
GPIO Jumper status on J403 header can be read from IO port address 0x84. Make sure the access is volatile to access the hw register as the write to the same address writes LED indicator register. The LEDs are located under the J403 header.

Mode Select

Mode select rotary switch is intended for internal image selection from Flash memory divided into 4 separate 4 MB sections or PSRAM also divided into 4 separate 4 MB sections. PSRAM provides shot-term storage when power is removed with fast write and read capability. With approximately 99% charged capacitor PSRAM content is maintained over 2h. (The charge time to 99% of capacitor depends on initial charge, but should not be longer than 2 minutes)

Jumper settings on GPIO header

The GPIO header J403 with jumper status LEDs is by default used for jumpers. Pin pairs 3-4, 5-6 and 7-8 from the header are used as jumper pins. Pin pair 1-2 is 3.3V and can't be used as a jumper pins. Jumper on header pin pair:



- 3-4 is “Enable LPC Memory read” this is legacy option to allow booting from devices that don't support LPC Firmware Hub read cycles although LPC Firmware read cycles are also responded in this configuration. If pins 1-2 are left open only LPC Firmware read cycles are responded.
- 5-6 is Post code peek mode enable jumper. In this mode FlexyICE II is not a memory device and accepts only IO write commands to addresses 0x0080 (post code) and 0x0088 (memory size command register) the post code bytes are displayed on lower two segments of 4 segment

display.

- 7-8 , 9-10 , 11-12 Encode modes Post code logger and 16550 UART base addresses

  The LPC UART implementation has selectable base address. The base address can be selected via Jumpers on J403 header or the jumper selection overridden by LPC IO write to address 0x88. The override is volatile and is used until FlexyICE device is continuously powered.

  IO write commands for UART base address selection are:

Command to 0x88	UART base address selected	IRQ on SERIRQ
0xC0	0x3F8	4
0xC1	0x2F8	3
0xC2	0x3E8	4
0xC3	0x2E8	3

Jumper settings on J403 pins 7-8, 9-10 and 11-12 for UART base address selection are:

Jumper settings pins |7,8|9,10|11,12|	Feature selected	IRQ
[Off,Off,Off]	PC utility access enabled	
[Off,Off,On]	UART on base address 0x3F8	SERIRQ 4
[Off,On,Off]	UART on base address 0x2F8	SERIRQ 3
[Off,On,On]	UART on base address 0x3E8	SERIRQ 4
[On,Off,Off]	Post code serial logger enabled	
[On,On,On]	UART on base address 0x2E8	SERIRQ 3

Post code logger mode enable jumper. In this mode all post codes are sent to USB serial port. Open serial terminal to the FTDI USB serial port with settings: baud=115200, data=8 bit, parity=none, stop=1 bit, Flow=none. Post codes are displayed in hexadecimal format 16 bytes per line (\r\n as line separators) all bytes are prefixed by “x” and byte separator is space character. For example:

“x80 x11 x55 x10 x80 x11 x55 x10 x80 x11 x55 x10 x80 x11 x55 x10\r\n”

The 4 segment display in this mode will show internal FIFO byte count. If the byte count reaches “x1F40” the FlexyICE II will start to flow control LPC IO write cycles to avoid data loss. This may affect boot time if post code IO writes are heavily used (no data loss should occur).

- 13-14 Force the boot window to be 4MB this can be supported by newer architectures

GPIO pins are platform pins that are not used in the standard LPC version of the FlexyICE II but are target for tailored development for specific functions.

VCC source select

FlexyICE II has automatic VCC source selection. When USB cable is used at the same time with target board LPC connection, the power will be drawn from USB cable.

When target board is used as voltage source the POR (power on reset) time along with the FPGA configuration time (~ 30 ms) has to be taken into account when using the FlexyICE II as a boot device. It is recommended to use target board reset to initiate clean boot after power up.

USB

USB interface is used to program FlexyICE II flash or read back flash content. This can be done by Artec USB FlexyICE II programming utility.

Usage:

Write file	dongle.py [-vq] -c <name> <file> <offset>
Readback file	dongle.py [-vq] -c <name> [-vq] -r <offset> <length> <file>

Options:

<file> <offset>	When file and offset are given file will be written to device
file:	File name to be written to device
offset:	Specifies data writing starting point in bytes to 4M window
	For ThinCan boot code the offset = 4M - filesize. To write
	256K file the offset must be 3840K
-c <name>	Indicate port name where the USB Serial Device is
name:	COM port name in Windows or Linux Examples: COM3,/dev/ttyS3
	See Device Manager in windows for USB Serial Port number
-v	Enable verbose mode. Displays more progress information
-q	Perform flash query to see if device flash is responding
-r <offset> <length> <file>	Readback data. Available window size is 4MB
offset:	Offset byte addres inside 4MB window. Example: 1M
	use M for MegaBytes, K for KiloBytes, none for bytes
	use 0x prefix to indicate hexadecimal number format.
length:	Amount in bytes to read starting from offset. Example: 1M
	use M for MegaBytes, K for KiloBytes, none for bytes
file:	Filename where data will be written
-e	Erase device. Erases Full 4 MegaBytes

Board test options:

-t	Marching one and zero test. Device must be empty
	To test device erase the flash with command -e

	Enables device memory tests to be executed by user
-b	Leave flash blank after test. Used with option -t

Examples:

dongle.py -c COM3 loader.bin 0

dongle.py -c /dev/ttyS3 boot.bin 3840K

dongle.py -c COM3 -r 0x3C0000 256K flashcontent.bin

USB programming utility can address all of the 4 MB available in any mode that is selected. It must be remembered that only 3072KB to 4096 KB in each mode configuration is directly accessible over LPC and is repeated in LPC memory address space (x86 legacy 1M window) without using the 0xF4 command first (see LPC paragraph).

FAQ

Q: Why does the FlexyICE II give error code when opening serial port in Ubuntu Linux?

A: If you use Ubuntu, make sure to uninstall brltty (apt-get remove brltty --purge) before you hook up the FlexyICE II; otherwise it will hijack the FlexyICE II and you won't be able to talk to it. Brltty is a software Braille terminal.
(http://www.coreboot.org/Artecgroup_programmable_LPC_dongle)

Source code

Source SVN repository is available at

http://www.opencores.org/project,artec_dongle_ii_fpga

Contains:

- Python USB application source code
- VHDL LPC slave (supporting IO write and Memory read)
- VHDL Flash Waveform generator
- VHDL FTDI parallel interface to on-board flash (supports block write)
- VHDL Scanning LED segment display coder
- Project files with pin location constraints (for Altera Quartus™ Web Edition)