Small soft core uP Inventory ©2014 James Brakefield

Opencore and other soft core processors

_uP_cores_test folder	opencores name	status	author	style / clone	data size	inst size	FPGA	reporter	comment	LUTs ALM	LUT?	mults	blk ram	F max	tool ver	MIPS /clk	clks/ inst	KIPS /LUT	src code	# src files	top file	doc	tool chain	fltg pt	Hard	max data	max inst	byte adrs	# inst	# reg	pipe len	start year	last revis	reference	note worthy	comments
1664	1664 microproce	sim?	Denis Godinho																C										26			2010	2010		C based simulation only	
8051	8051	alpha	Simon Teran, Jakas	8051	8	8													verilog	32	oc8051_t	yes	yes	N		64K	64K	Y				2001	2009	8051 data sheets	not fully tested	
6502_verilog	6502_verilog_de	sim?	Hyungok Tak	6502	8	8x													verilog				yes	N	N	64K	64K	Y				2010	2010	6502 data sheets	no files, simulated	
6502vhdl	6502vhdl	planning	Huyvo	6502	8	8x													C				yes	N	N	64K	64K	Y				2003	2009	6502 data sheets	to have a C program generate VHDL	
6809_6309	6809_6309_com	beta	Alejandro Paz Schmidt	6809	8x	8x	spartan-6-3	James Brakef		2061	6			109	14.7	0.33	1.0	17	verilog	5	MC6809_cpu		yes	N	N	64K	64K	Y				2012	2013	6809 data sheets	includes 6309 op-codes, xilinx & lattice projects	
6809_6309	6809_6309_com	beta	Alejandro Paz Schmidt	6809	8x	8x	kintex-7-3	James Brakef		2207	6			212	14.7	0.33	1.0	32	verilog	5	MC6809_cpu		yes	N	N	64K	64K	Y				2012	2013	6809 data sheets	includes 6309 op-codes, xilinx & lattice projects	
68hc05	68hc05	stable	Ulrich Riedel	6805	8	8x	kintex-7-3	James Brakef		1225	6			300	14.7	0.33	1.0	81	vhdl	1	6805		yes	N	N	64K	64K	Y				2007	2009	6805 data sheets		
68hc08	68hc08	stable	Ulrich Riedel	6808	8	8x	kintex-7-3	James Brakef		2290	6			101	14.7	0.33	1.0	15	vhdl	1	x68ur08		yes	N	N	64K	64K	Y				2007	2009	6808 data sheets		
8bit_chapman		beta	Rob Chapman, Steven	forth	8	8	kintex-7-3	James	syntax errors		6				14.7	0.33	1.0	####	vhdl	10	top	yes		N		256	256					1998			course work	
ae18	ae18	beta	Shawn Tan	PIC18	16	24	arria-2	James Brakef		1084	A	1		207	13.1	0.67	1.0	128	verilog	1	ae18_core		yes	N	Y	4K	1M					2003	2009	PIC18 data sheets	not 100% compatable	negative edge reset "clock"
ae18	ae18	beta	Shawn Tan	PIC18	16	24	spartan-6-3	James Brakef		1176	6	1		81	14.7	0.67	1.0	46	verilog	1	ae18_core		yes	N	Y	4K	1M					2003	2009	PIC18 data sheets	not 100% compatable	negative edge reset "clock"
ae18	ae18	beta	Shawn Tan	PIC18	16	24	virtex-6-3	James Brakef		1133	6	1		117	14.7	0.67	1.0	69	verilog	1	ae18_core		yes	N	Y	4K	1M					2003	2009	PIC18 data sheets	not 100% compatable	negative edge reset "clock"
ae18	ae18	beta	Shawn Tan	PIC18	16	24	kintex-7-3	James Brakef		1131	6	1		68	14.7	0.67	1.0	41	verilog	1	ae18_core		yes	N	Y	4K	1M					2003	2009	PIC18 data sheets	not 100% compatable	negative edge reset "clock"
aeMB	aeMB	beta	Shawn Tan	uBlaze	32	32	kintex-7-3	James Brakef		1018	6	3		131	14.7	1.30	1.0	167	verilog	29	aeMB_co	yes	yes	N		4G	4G	Y				2004	2009	xilinx documentation	not 100% compatable	
af65k		alpha	Andre Fachat	6502	16	8x													vhdl			yes		N	N							2011			extended 6502 with 16, 32 or 64 bit data	
ag_6502	ag_6502 soft cor	beta	Oleg Odintsov	6502	8	8x	spartan-6-3	James Brakef		807	6	0	0	80	14.7	0.33	1.0	33	verilog	2	ag_6502		yes	N	N	64K	64K	Y				2012	2012	6502 data sheets	verilog code generation, "phase level accurate", 978 LUTs	
agcnorm	Apollo Guidance	beta	Dave Roberts	?	16	16											1.0		vhdl	5	AGC	some		N		32M	32M					2010	2012		Apollo Guidance Computer via NOR gate emulation	
altor32	AltOr32	stable	Ultra Embedded	OpenRISC	32	32											1.0		verilog	19	altor32		yes	N		4G	4G	Y				2012	2014	OpenRISC 1000	simplified OpenRISC 1000	
alwcpu	Alwcpu	alpha	Andreas Hilvarsson	RISC	16	16	kintex-7-3	James Brakef		298	6			237	14.7	0.67	1.0	533	vhdl	7	top	some		N		64K	64K	Y		16		2009	2009		400 LUTs	
amber	Amber ARM-con	stable	Conor Santifort	ARM7	32	32	kintex-7-3	James	slow,	12450	6		4	98	14.7	0.90	1.0	7	verilog	25	a25_core	yes	yes	N		4G	4G	Y				2010	2013	ARM7 data sheets	no MMU	4096 single port RAM LUTs
ao68000	ao68000	beta	Aleksander Osman	68000	8x	16x	arria-2	James Brakef		3479	A		6	169	13.1	1.00	1.0	49	verilog	1	ao68000	some	yes	N		4G	4G	Y				2010	2011	68000 data sheets	uses microcode, 4750 LUTs	
aquarius	aquarius	stable	Thorn Aitch	SuperH-2	32	16	kintex-7-3	James Brakef		3958	6	2		86	14.7	1.00	1.0	22	verilog	21	top	yes	yes	N		4G	4G	Y				2003	2009	SuperH data sheets		
ARC		proprieta	Synopsys		32	16											1.0		not avail							4G	4G								range of reduced SPARC? uP	
ARM_Cortex_A9		ASIC	ARM	ARM a9	32	16	zynq	xilinx		4500	6			1000		2.50	1.0	556	asic			yes	yes	Y		4G	4G	Y	80	16	10		2012	xilinx plan ahead: an a	uses pro-rated LC area	dual issue, includes fltg-pt & MMU & caches
ARM_Cortex_A9		ASIC	ARM	ARM a9	32	16	arria V	altera		4500	A			1050		2.50	1.0	583	asic			yes	yes	Y		4G	4G	Y	80	16	10		2012	altera data sheets	uses pro-rated LC area	dual issue, includes fltg-pt & MMU & caches
ARM_Cortex_A9		ASIC	ARM	ARM a9	32	16	cyclone V	altera		4500	A			925		2.50	1.0	514	asic			yes	yes	Y		4G	4G	Y	80	16	10		2012	altera data sheets	uses pro-rated LC area	dual issue, includes fltg-pt & MMU & caches
aspida	ASPIDA DLX core	stable	Sotiriou	DLX	32	32	kintex-7-3	James Brakef		3586	6			257	14.7	1.00	1.0	72	verilog	10	DLX_top	yes	yes			4G	4G					2002	2009	Knuth DLX		compiled sync version
atlas_core	Atlas Processor (	beta	Stephan Nolting	RISC	16	16	arria-2	James Brakef		906	A	2	2	138	14.7	0.80	1.0	122	vhdl	13	ATLAS_C(	yes	asm	N		4G	4G	N	80	8		2013	2013		ARM thumb like inst set, also X2 versic	both MMU and non-MMU versions
atlas_core	Atlas Processor (	beta	Stephan Nolting	RISC	16	16	spartan-6	James Brakef		677	6	1	1	103	14.7	0.80	1.0	122	vhdl	13	ATLAS_C(	yes	asm	N		4G	4G	N	80	8		2013	2013		ARM thumb like inst set, also X2 versic	both MMU and non-MMU versions
atlas_core	Atlas Processor (	beta	Stephan Nolting	RISC	16	16	kintex-7-3	James Brakef		655	6	1	1	192	14.7	0.80	1.0	235	vhdl	13	ATLAS_C(	yes	asm	N		4G	4G	N	80	8		2013	2013		ARM thumb like inst set, also X2 versic	both MMU and non-MMU versions
atlas_x2	Atlas Processor (	beta	Stephan Nolting	RISC	16	16	kintex-7-3	James	missing define		6	1	1		14.7	0.80	1.0	####	vhdl	13	ATLAS_X2	yes	asm	N		4G	4G	N	80	8		2013	2013		ARM thumb like inst set	has MMU & full SOC features
avr_core	avr_core	stable	Rusian Lepetenok	AVR	8	16	kintex-7-3	James	errors	2135	6			127	14.7	0.33	1.0	20	verilog		avr_core		yes	N		64K	128K	Y		32		2002	2012	AVR data sheets	VHDL core included	
avr_hp	avr_hp	stable	Strauch Tobias	AVR	8	16	kintex-7-3	James	1 slot	1199	6			127	14.7	0.33	1.0	35	vhdl	9	avr_core	some	yes	N		64K	128K	Y		32		2010	2010	AVR data sheets	hyper pipelined (eg barrel) AVR	
avr_hp	avr_hp	stable	Strauch Tobias	AVR	8	16	kintex-7-3	James	2 slot	1554	6			223	14.7	0.33	1.0	47	vhdl	10	avr_core	some	yes	N		64K	128K	Y		32		2010	2010	AVR data sheets	hyper pipelined (eg barrel) AVR	
avr_hp	avr_hp	stable	Strauch Tobias	AVR	8	16	kintex-7-3	James	3 slot	1812	6			243	14.7	0.33	1.0	44	vhdl	10	avr_core	some	yes	N		64K	128K	Y		32		2010	2010	AVR data sheets	hyper pipelined (eg barrel) AVR	
avr_hp	avr_hp	stable	Strauch Tobias	AVR	8	16	kintex-7-3	James	4 slot	2054	6			278	14.7	0.33	1.0	45	vhdl	10	avr_core	some	yes	N		64K	128K	Y		32		2010	2010	AVR data sheets	hyper pipelined (eg barrel) AVR	
avr8	Reduced AVR Co	beta	Nick Kovach	AVR	8	16	kintex-7-3	James Brakef		174	6			418	14.7	0.33	1.0	792	verilog	1	rAVR	yes	yes	N		64K	64K	Y	17	4		2010	2010	AVR data sheets	not a full clone, doc is opencores page	
avrtinyx61co	avrtinyx61core	beta	Andreas Hilvarsson	AVR	8	16	kintex-7-3	James Brakef		1243	6			194	14.7	0.33	1.0	51	vhdl	1	mcu_core		yes	N		64K	128K	Y		32		2008	2009	AVR data sheets		
ax8	AX8 MCU	stable	Daniel Wallner	AVR	8	16	spartan-6-3	James	missing ROM		6				14.7		1.0		vhdl	14	A90S1200			N		64K	128K	Y		32		2002	2009	AVR data sheets	both A90S1200 & A90S2313	
b16		stable	Bernd Paysan	forth	16	5	spartan-6-3	James Brakef		554	6			134		0.67	1.0	162	verilog	1	b16	yes	yes	N								2002	2011	bernd-paysan.de/b16	two versions: one/15 source files, derived from c18	
ba22		proprieta	CAST Inc	RISC	32	16x	spartan-6	CAST Inc		1800	6		32	72		1.00	1.0	40	not avail							4G	4G			32				www.cast-inc.com		
blue	16-bit CPU Blue	stable	Al Williams	accum	16	16	spartan-6-3	James	missing file		6					0.67	1.0	####	verilog	16	top	web		N		4K	4K	N	16	2		2009	2010		Caxton Foster's Blue derivative	http://www.youtube.com/watch?v=dt4zezZP8v
bobcat		beta	Stan Drey		16	24	kintex-7-3	James Brakef		1622	6	1		107	14.7	0.67	1.0	44	vhdl							64K	64K					1998			appears to be a DSP	
c0or1k	Codezero OpenR	planning	Drasko Draskovic	RISC															no code													2010			C code for simulation	
c16	16 Bit Microcont	stable	Jsauermann	C	16	8x	spartan-3-5	James Brakef		1850	4		16	57	14.7	0.33	1.0	10	vhdl	22	Board_cp	min	C,asm	N		64K	64K	Y		5		2003	2012		8080 derivative, optional UART, 8-bit memory port	
cf_ssp	CF State Space P	stable	Tom Hawkins	?															vhdl													2003	2009		confluence to VHDL	
copyblaze	copyBlaze	stable	Abdallah Ellbrahimi	picoBlaze	8	18	spartan-6-3	James Brakef		619	6			86		0.33	1.0	46	vhdl	16	cp_copyb	yes	asm	N		256	2K	Y				2011	2013	microBlaze data shee	wishbone extras	LUT count high, Fmax low: see picoblaze
cortex_m3	cortex_m3	?	Strauch Tobias	ARM c3	32	16													no files													2013		cortex M3 data sheet	claims to be mature	
cowgirl	Cowgirl	beta	Thebeekeeper		16	16	kintex-7-3	James	empty design		6				14.7	0.67	1.0	####	vhdl	14	cowgirl						64K					2006	2009			
cpu16		beta	C. H. Ting	forth	16	5	kintex-7-3	James	case c	367	6			355	14.7	0.67	1.0	648	vhdl	1	cpu16	yes	asm	N		64K	64K					2000			part of eForth?	
cpu6502_tru	cpu6502_tc	stable	Jens Gutschmidt	6502	8	8x	kintex-7-3	James Brakef		1678	6			159	14.7	0.33	1.0	31	vhdl	7	r6502_tc		yes	N	N	64K	64K	Y				2008	2010	6502 data sheets		
cpu65c02_tru	cpu65c02_tc	stable	Jens Gutschmidt	6502	8	8x	spartan-6-3	James	latch v	4794	6			47	14.7	0.33	1.0	3	vhdl	8	core		yes	N	N	64K	64K	Y				2008	2013	6502 data sheets		
cpu8080	8080 Compativle	stable	Scott Moore	8080	8	8x	spartan-6-3	James Brakef		1269	6			129	14.7	0.33	1.0	34	verilog	1	m8080	yes	yes	N	N	64K	64K	Y				2006	2009	8080 data sheets	includes VGA display generator, three variants	
cpu86		beta	ht-lab.com	8086	8	8x	kintex-7-3	James Brakef		3421	6	1		127	14.7	0.17	1.0	6	vhdl	23	cpu86_to	yes	yes	N	N	1M	1M	Y				2002	2010	x86 data sheets	8088 clone	www.ht-lab.com
cpugen	Cpu Generator	stable	Giovanni Ferrante																													2003	2009		x86 executable that generates VHDL uP	
cray1		alpha	Christopher Fenton	cray1	64	16													verilog	42	cray_top	yes	yes	Y	N	4M	4M	N				2010		CRAY data sheets	homebrew Cray1	www.chrisfenton.com/homebrew-cray-1a/
crisc_cpu	CRISC CPU	planning	Andre Adrian	68000 like	8x	16x													no files					N		4G	4G	Y	20	15		2011			see opencores web page: both 16-bit & 32-bit registers, 11 addressing modes	
dalton_8051		stable	Tony Givargis	8051	8	8x	kintex-7-3	James Brakef		2725	6	1	1	105	14.7	0.33	1.0	13	vhdl	7	i8051_all	yes	yes	N	N	64K	64K	Y				1999	2003	8051 data sheets	ASIC	www.cs.ucr.edu/~dalton/
dataflow_chapman		alpha	Rob Chapman, Steven	forth			kintex-7-3	James	file WebCase		6				14.7	0.33	1.0	####	vhdl	27	DataFlow	yes		N		256	256					2003			course work	
df6805		proprietar	Hitech Global	6805	8	8x	stratix-1	Hitech Globa		1690	4			83		0.33	1.0	16	not avail				yes	yes	N	N	64K	64K	Y						6805 data sheets		www.hitechglobal.com/IPCores/DF6805.htm
dfp	dfp	stable	Ron Chapman	forth	X	Y	spartan-6-3	James Brakef		334	6			112	14.7	0.33	1.0	111	vhdl	25	top	yes										2003	2009		8-bitter, generates a custom VHDL stack machine, compiler is in Forth	
diogenes	diogenes	beta	Fekknhifer	RISC	16	16	kintex-7-3	James	missing file "t		6				14.7	0.67	1.0	####	vhdl	11	cpu						1K					2008	2009			
distributed_i	Distributed limit	planning	Leo Ger		16	16													vhdl	11	mini_uP_x16			N		64K	64K					2009	2009		single stack and 4 data registers	
dragonfly		beta	LEOX team	MISC	16	16	kintex-7-3	James Brakef		788	6			164	14.7	0.67	1.0	139	vhdl	6	dgf_core	yes		N		256	2K					2001		www.leox.org	unusual, uses FIFOs	
eco32	SOC:ECO32	alpha	Hellwing Geisse	RISC	32	32	cyclone-4-6	James Brakef		5153	4			84	13.1	1.00	1.0	16	verilog	23	cpu	yes	yes	N		512M	256M	Y	61	32		2003	2014		MIPS like, MMU	
eco32	SOC:ECO32	alpha	Hellwing Geisse	RISC	32	32	arria-2	James Brakef		2711	A			129	13.1	1.00	1.0	48	verilog	23	cpu	yes	yes	N		512M	256M	Y	61	32		2003	2014		MIPS like, MMU	
eco32	SOC:ECO32	alpha	Hellwing Geisse	RISC	32	32	spartan-3-5	James Brakef		3034	4		2	55	14.7	1.00	1.0	18	verilog	23	cpu	yes	yes	N		512M	256M	Y	61	32		2003	2014		MIPS like, MMU	
eco32	SOC:ECO32	alpha	Hellwing Geisse	RISC	32	32	spartan-6-3	James Brakef		2271	6		1	92	14.7	1.00	1.0	41	verilog	23	cpu	yes	yes	N		512M	256M	Y	61	32		2003	2014		MIPS like, MMU	
eco32	SOC:ECO32	alpha	Hellwing Geisse	RISC	32	32	kintex-7-3	James Brakef		2210	6		1	160	14.7	1.00	1.0	72	verilog	23	cpu	yes	yes	N		512M	256M	Y	61	32		2003	2014		MIPS like, MMU	
ecpu	ecpu	planning	Sahrfili Matturi																verilog													2009	2009			
edu_3bus_ar	Educational 3 Bu	spec	Ayman Mohamed	RISC	32	32													no files										33	32		2012	2013			
eight_bit_uc		stable	Synplicity	RISC	8	12	kintex-7-3	James	signal/variable		6				14.7	0.67	1.0	####	vhdl	10	eight_bit_uc						2K	Y		32					part of Amplify documentation	
elm	ELM Embedded	alpha	David Sheffield, Curt Harting																no files													2010	2010			
encore	Encore	planning	Aloy Ambergen																no files													2010	2011			
ensilica		proprieta	ensilica.com	eSi-1600	16		virtex-5	ensilica		1100	6			160		0.67	1.0	97	not avail			yes	yes	N		64K	64K			16				www.ensilica.com	verilog source included with license	10 addressing modes
ensilica		proprieta	ensilica.com	eSi-3200	32		stratix-4	ensilica		1800	A			200		1.00	1.0	111	not avail			yes	yes			4G	4G			16	5			www.ensilica.com	verilog source included with license	10 addressing modes
eric5		proprieta	enter-electronics.com	forth	9	9	cyclone-4-6	enter-electronics.com			4	opt		60		0.67	1.0		not avail							512	128K			3-4		2007			40 MIPS: ERIC5+, ERIC5Q+	
eric5		proprieta	enter-electronics.com	forth	9	8	cyclone-4-6	enter-electro		110	4	opt		60		0.42	1.0	229	not avail							512	1K			3-4		2007			25 MIPS: ERIC5xs, ERIC5Q	
erp	Educational RISC	stable	Shahzadjk	RISC	8	16	kintex-7-3	James	syntax errors		6				14.7	0.33	1.0	####	verilog	1	ERPverilo	yes							15	6		2004	2009		two report PDFs & one Verilog file	
fpgammix		stable	Tommy Thorn	RISC	64	32			system verilog								1.0		system v	12	core	yes							256	256		2006	2008		clone of Knuth's MMIX	
free_risc8		stable	Thomas Coonan	PIC16	8	14	kintex-7-3	James Brakef		355	6			142	14.7	0.33	1.0	132	verilog	8	cpu	yes	yes	N		256	4K	Y				2002	2011	PIC16 data sheets		
free6502		stable	David Kessner	6502	8	8x	spartan-6-3	James Brakef		663	6			89	14.7	0.33	1.0	44	vhdl	5	free6502	yes	yes	N	N	64K	64K	Y				1999	2000	6502 data sheets	microcoded	
gl85		stable	Alex Miczo	8085	8	8x	kintex-7-3	James	gate level des		6				14.7	0.33	1.0	####	vhdl	1	i8085	yes	yes	N	N	64K	64K	Y				1993		8085 data sheets	also a TTL implementation in VHDL	
gullwing		simulatior	Charles LaForest	forth	32	5													no code			yes	asm	N		4K	4K					2007		BS thesis	virtual stack machines vs RISC	MuP21 clone
gumnut		stable	Peter Ashenden	RISC	8	18	kintex-7-3	James	missing file		6				14.7	0.33	1.0	####	vhdl	20	gumnut s	yes		N		256	4K	Y		8		2007			see Digital Design: An Embedded Systems Approach Using VHDL	
gup	HC11 Compatibl	stable	Kevin Phillipson	68C11	8x	8x	kintex-7-3	James	missing uP file		6				14.7	0.67	1.0	####	vhdl	25	?	yes	yes	N	N	64K	64K	N				2008	2009	6811 data sheets	68HC11 compatible	
Hay4Stk32_16m		defined	James Brakefield	4 stack	16	32			incomplete VH		6	1	1				1.0		vhdl			yes		opt	Y	64K	64K	N	53	8	2	2013	2013		four accumulator/stack & C machine, 16-bit word size & 32-bit instruction size, no LUT	

_uP_cores_test folder	opencores name	status	author	style / clone	data size	inst size	FPGA	reporter	comment	LUTs ALM	LUT?	mults	blk ram	F max	tool ver	MIPS /clk	clks/ inst	KIPS /LUT	src code	# src files	top file	doc	tool chain	fltg pt	Hard	max data	max inst	byte adrs	# inst	# reg	pipe len	start year	last revis	reference	note worthy	comments
hc11core		stable	Green Mountain Comp	68HC11	8x	8x	kintex-7-3	James Brakef		2014	6			125	14.7	0.33	1.0	21	vhdl	1	hc11rtl	yes	yes	N	N	64K	64K	N	53	8	2	2000		6811 data sheets	restricted use license, no divide inst	
hd63701	HD63701 compa	planning	Tsuyoshi Hasegawa	6801	8	8x	spartan-3-5	James Brakef		1937	4	1	3	20	14.7	0.33	1.0	3	verilog	6	HD63701_CORE			N	N	64K	64K	Y				2014			Used in Atari game console, 6801 clone?	
hd63701	HD63701 compa	planning	Tsuyoshi Hasegawa	6801	8	8x	spartan-6-3	James Brakef		1412	6	1	3	31	14.7	0.33	1.0	7	verilog	6	HD63701_CORE			N	N	64K	64K	Y				2014			Used in Atari game console, 6801 clone?	
hicovec	HiCoVec a config	beta	Harald Manske, Gundo	RISC	32	32	kintex-7-3	James	compiler erro		6				14.7	1.00	1.0	####	vhdl	28	cpu	yes	asm	N				Y				2008	2010		hybrid scalar & vector processor	
hive	hive	stable	Eric Wallin	4-8 stack	32	16	cyclone-3	Eric Wallin		1800	4	4	3	200		1.00	1.0	111	verilog			yes		N				N	40	10	8	2013	2014		4-8 symetrical stacks, eight threads via pipeline barrel	
hive	hive	stable	Eric Wallin	4-8 stack	32	16	cyclone-5	Eric Wallin		1877	4	4	3	226		1.00	1.0	120	verilog			yes		N				N	40	10	8	2013	2014		4-8 symetrical stacks, eight threads via pipeline barrel	
hivek		alpha	Hadley Magno	VLIW	32												1.0		vhdl	18	hivek											2013			two inst per clock	incomplete source code
hmta	HyperMTA	planning	Alikat etal																no files					Y						64		2002	2009		up to 256 threads	
hpc-16	HPC-16	beta	Umair Siddiqui	RISC	16	16	kintex-7-3	James Brakef		875	6			136	14.7	0.67	1.0	104	vhdl	20	cpu	yes	asm	N		64K	64K			16		2005	2009			
ic6821	vhdl core of IC68	beta	Ttsenis		8												1.0		vhdl	1	VHDL682	yes										2005	2009	6800 data sheets	VHDL for M6821	
iDEA		proprietar	Liu Cheah etal	RISC	16	32	virtex-6	Liu Cheah		190	6	1	1	534		0.67	1.0	1883	not avail										20	32	9		2011	A Lean FPGA Soft Pro	uses DSP slice in barrel mode for ALU	by Xilinx, no source
ignite_ptsc		proprietar	George Shaw	forth	32	8											1.0		not avail					N		4G	4G					1995	2002		ShBoom clone, fast ASIC with high coding density	
ion	Ion MIPS compa	mature	Jose Ruiz	MIPS	32	32	virtex-5	Jose Ruiz		2017	6			104		1.00	1.0	52	vhdl	12	mips_soc	yes	yes	N		4G	4G	Y		32		2011	2014		MIPS R3000 clone	
ion	Ion MIPS compa	mature	Jose Ruiz	MIPS	32	32	kintex-7-3	James Brakef		1533	6			163	14.7	1.00	1.0	106	vhdl	12	mips_soc	yes	yes	N		4G	4G	Y		32		2011	2014		MIPS R3000 clone	
J1		stable	James Bowman	forth	16	16	spartan-6	James Brakef		333	6		1	117	14.7	0.80	1.0	280	vhdl	1	j1	yes	forth	N		64K	64K		16		2	2006	2010	excamera.com/sphinx	uCode inst, dual port block RAM	32 deep data & return stacks
J1		stable	James Bowman	forth	16	16	kintex-7-3	James Brakef		387	6		4	133	14.7	0.80	1.0	275	verilog	1	j1	yes	forth	N		64K	64K		16		2	2006	2010	excamera.com/sphinx	uCode inst, dual port block RAM	32 deep data & return stacks
J1		stable	James Bowman	forth	16	16	kintex-7-3	James	syntax errors		6				14.7	0.80	1.0	####	vhdl	1	j1	yes	forth	N		64K	64K		16		2	2006	2010	excamera.com/sphinx	uCode inst, dual port block RAM	32 deep data & return stacks
jam		stable	Johan Thelin etal	RISC	64	32	kintex-7-3	James Brakef		1369	6			143	14.7	1.00	1.0	104	vhdl	17	cpu	yes		N		128K	128K			32	5	2002				
jane_nn		stable	Suresh Devanathan	RISC	4	8	kintex-7-3	James Brakef		723	6			178	14.7	0.33	1.0	81	vhdl	3	Processor	yes							27	16		2002			neural network microprocessor, specialized registers	
jmr16f84	JMP16F84 PIC M	stable	Julio Rodriguez	PIC16	8	14											1.0		no files						Y							2013		PIC16 data sheets		
jop	JOP a Java Optim	stable	Martin Schoeberl etal	forth	16	16	cyclone-1	Martin Schoe		2000	4			100	10	0.67	1.0	34	vhdl	11	core	yes	yes	N		256K	256K					2004	2014		opencores download is empty	https://github.com/jop-devel/jop
jpu16		stable	Joksan Alvarado	RISC	16	26	kintex-7-3	James	missing define		6				14.7	0.67	1.0	####	vhdl	9	JPU16	yes	asm	N		64K	64K			16		2012			32 deep call stack, 8 addressing modes	
k68	K68	alpha	Shawn Tan	68000	8x	16x													verilog	15	k68_cpu	yes	yes	N	N	4K	4G	Y		16		2003	2009	68000 data sheets	68K binary compatible	
klc32	KLC32	planning	Robert Finch	RISC	32	32													verilog	25	KLC32	yes		N		4G	4G	Y		32		2011	2012			
lattice6502	Lattice 6502	beta	Ian Chapman	6502	8	8x	kintex-7-3	James Brakef		4942	6			214	14.7	0.33	1.0	14	vhdl	3	ghdl_prod	yes	yes	N	N	64K	64K	Y				2010	2010	6502 data sheets	targeted to LCMXO2280	huge LUT count
latticemicro32		stable	Yann Siommeau, Micha	RISC	32	32	spartan-6	James Brakef		2093	6	3	15	85	14.7	0.80	1.0	32	verilog	24	lm32_cpu	yes	yes	N		4G	4G	Y		32		2006	2012	en.wikipedia.org/wiki	optional data & inst caches	
latticemicro32		stable	Yann Siommeau, Micha	RISC	32	32	kintex-7-3	James Brakef		2292	6	3	8	155	14.7	0.80	1.0	54	verilog	24	lm32_cpu	yes	yes	N		4G	4G	Y		32		2006	2012	en.wikipedia.org/wiki	optional data & inst caches	
latticemicro8		stable	Lattice Semiconductor	RISC	8	18	LFE2	Lattice Semic		265	4			104			1.0		vhdl	10	isp8_core	yes	yes	N		256	4K	Y		32		2005	2010	en.wikipedia.org/wiki	16 deep call stack, four configurations	
lem1_9	lem1_9	stable	James Brakefield	accum	1	9	kintex-7	James Brakef		40	6		1	357	14.5	0.04	1.0	357	vhdl	3	lem1_9m	yes	asm	N	Y	6	11	N	8	64	1	2003	2009		very small, 2 pipe stage is twice as fast	"logic emulation machine"
lem16_18m		alpha	James Brakefield	accum	16	18	spartan-6-3	James	incom	471	6		1	178	14.7	0.67	1.0	253	vhdl	2	lem16_18	yes		N	Y	16	16	Y	100	3	1	2009	2013		LUT instructions, bit fields to/from data memory	
lem16_18m		alpha	James Brakefield	accum	16	18	kintex-7-3	James	incom	483	6		1	295	14.7	0.67	1.0	409	vhdl	2	lem16_18	yes		N	Y	16	16	Y	100	3	1	2009	2013		LUT instructions, bit fields to/from data memory	
lemberg		stable	Wolfgang Puffitsch	VLIW	32	32	cyclone-4-6	James	fitter failed		4				13.1	1.00	1.0	####	vhdl	32	core	yes	yes	Y		4G	2M	Y		32	4	2011		www2.imm.dtu.dk/~	upto 4 inst/clock	
leon		stable	Jiri Gaisler, Jan Anderss	SPARC	32	32			hard to find min configuration								1.0		vhdl	100s	leon3x	yes	yes	Y		4G	4G			64		2003	2013	SPARC data sheets	customized for ~20 FPGA boards, configurable	
leros	Leros	stable	Martin Schoeberl	accum	16	16	cyclone-4-6	Martin Schoe		189	4		1	160		0.67	1.0	567	vhdl	6	leros "top	yes	yes	N		64K	64K			2	2	2008	2012	Leros: A Tiny Microco	short LUT inst ROM	256 word data RAM, PIC like
leros	Leros	stable	Martin Schoeberl	accum	16	16	spartan-3	Martin Schoe		188	4		1	129		0.67	1.0	460	vhdl	6	leros "top	yes	yes	N		64K	64K			2	2	2008	2012	Leros: A Tiny Microco	short LUT inst ROM	256 word data RAM, PIC like
leros	Leros	stable	Martin Schoeberl	accum	16	16	spartan-6	Martin Schoe		112	6		1	182	14.7	0.67	1.0	1089	vhdl	6	leros "top	yes	yes	N		64K	64K			2	2	2008	2012	Leros: A Tiny Microco	short LUT inst ROM	256 word data RAM, PIC like
leros	Leros	stable	Martin Schoeberl	accum	16	16	cyclone-4-6	James Brakef		132	4		1	199	13.1	0.67	1.0	1010	vhdl	6	leros "top	yes	yes	N		64K	64K			2	2	2008	2012	Leros: A Tiny Microco	short LUT inst ROM	256 word data RAM, PIC like
leros	Leros	stable	Martin Schoeberl	accum	16	16	spartan-3-5	James	proba	116	4		1	155	14.7	0.67	1.0	898	vhdl	6	leros "top	yes	yes	N		64K	64K			2	2	2008	2012	Leros: A Tiny Microco	short LUT inst ROM	256 word data RAM, PIC like
leros	Leros	stable	Martin Schoeberl	accum	16	16	spartan-6	James	proba	66	6		1	222	14.7	0.67	1.0	2257	vhdl	6	leros "top	yes	yes	N		64K	64K			2	2	2008	2012	Leros: A Tiny Microco	short LUT inst ROM	256 word data RAM, PIC like
leros	Leros	stable	Martin Schoeberl	accum	16	16	kintex-7-3	James	adjust	115	6		1	277	14.7	0.67	1.0	1614	vhdl	6	leros "top	yes	yes	N		64K	64K			2	2	2008	2012	Leros: A Tiny Microco	short LUT inst ROM	256 word data RAM, PIC like
leros32	Leros-32	alpha	Jon Pry	forth	32														no files					N		4G	4G					2013			see Leros entry	
light52	Lightweight 8051	beta	Jose Ruiz	8051	8	8x	kintex-7-3	James Brakef		1027	6	1	1	148	14.7	0.17	1.0	24	vhdl	8	light52_c	yes	yes	N	N	64K	64K	Y				2012	2013	8051 data sheets	targeted to area	
light8080	Lightweight 8080	stable	Jose Ruiz, Moti Litoche	8080	8	8x	kintex-7-3	James Brakef		154	6		1	247	14.7	0.17	1.0	265	verilog	5	i80soc	yes	yes	N	N	64K	64K	Y				2007	2012	8080 data sheets	targeted to area, includes UART, interrupt ctlr & RAM	
light8080	Lightweight 8080	stable	Jose Ruiz, Moti Litoche	8080	8	8x	spartan-6	James Brakef		148	6		3	172	14.7	0.17	1.0	192	verilog	5	light8080	yes	yes	N	N	64K	64K	Y				2007	2012	8080 data sheets	targeted to area, bare core	
light8080	Lightweight 8080	stable	Jose Ruiz, Moti Litoche	8080	8	8x	kintex-7-3	James Brakef		154	6		1	247	14.7	0.17	1.0	265	verilog	5	light8080	yes	yes	N	N	64K	64K	Y				2007	2012	8080 data sheets	targeted to area, bare core	
light8080	Lightweight 8080	stable	Jose Ruiz, Moti Litoche	8080	8	8x	spartan-6	James Brakef		150	6		3	142	14.7	0.17	1.0	156	vhdl	5	light8080	yes	yes	N	N	64K	64K	Y				2007	2012	8080 data sheets	targeted to area, bare core	
lpu	LocationPU	planning	Bkorsedal																no files													2002	2009		very early: minimal doc	
Lutiac		custom	David Galloway, David	2 reg	16	NA	stratix-4	David Gallow		140	A	4		198		0.67	1.0	948	either							64	N	64	32	3		2010	Lutiac – Small Soft Pro	no inst RAM, instead microcode	no inst mem: small state machine, ~200 inst opt
Lutiac		custom	David Galloway, David	2 reg	16	NA	stratix-4	David Gallow		480	A	4		197		0.67	1.0	275	either						Y	128	N	64	32	3		2010	Lutiac – Small Soft Pro	no inst RAM, instead microcode	no inst mem: large state machine, ~200 inst opt
lwrisc	ClaiRISC	stable	Li Wu	PIC16	8	14	arria-2	James	undefined cor		A				13.1	0.33	1.0	####	verilog	9	risc_core				Y							2008	2009	PIC16 data sheets		
m1_core	M1 Core	beta	Fabrizo Fazzino, Albert	MIPS?	32	32	kintex-7-3	James Brakef		3456	6			233	14.7	1.00	1.0	67	verilog	9	m1_core		yes	N		4G	4G	Y		32		2007	2012		GCC target?	
m65		stable	Naohiko Shimizu	6502	8	8x											1.0			8	m65cpu	yes	yes	N	N	4K	4K	Y				2001	2002	6502 data sheets	source files have unusual suffixes	
m65c02	M65C02	mature	Michael Morris	6502	8	8x	spartan-3	Michael Mor		661	4	0	3	74		0.33	1.0	37	verilog	13	M65C02	yes	yes	N	N	64K	64K	Y				2013	2014	6502 data sheets		
manik		stable	Sandeeo Dytta	RISC	32	32	arria-2	James	vcomponents		A				13.1	0.33	1.0	####	vhdl	45	manik2to	yes	yes	N		4K	4K	Y		16		2002	2006	www.niktech.com/	optional data & inst caches	
marca	McAdam's RISC (	stable	Wolfgang Puffitsch	RISC	16	16	kintex-7-3	James	syntax errors		6				14.7	0.67	1.0	####	vhdl	40	marca	yes		N		8K	16K		75	16	4	2007	2009			
mblite	MB-Lite	beta	Tamar Kranenburg	uBlaze	32	32	virtex-5				6			229			1.0		vhdl	10	core	yes	yes	N		4G	4G	Y	86	32		2009	2012	microBlaze data shee	not all instructions implemented	
mc6809e		beta	Flint Weller	6809	8x	8x	kintex-7-3	James	gate level prin		6				14.7	0.33	1.0	####	vhdl	26	core_680	yes	yes	N	N	64K	64K	Y				1999		6809 data sheets	course work, ASIC orientation	
mc8051		stable	Helmut Mayrhofer	8051	8	8x	kintex-7-3	James Brakef		3022	6	1		83	14.7	0.33	1.0	9	vhdl	49	mc8051co	yes	yes	N	N	256	64K	Y				1999	2013	www.oreganosystem	fast 8051, version available with floating-point by David Lundgren	
mcpu	MCPU A minima	stable	Tim Boscke	accum	8	8	spartan-6-3	James Brakef		41	6			384	14.7	0.17	1.0	1592	vhdl	1	tb02cpu2	yes	asm	N		64	64	Y	4			2007	2014		fits into 32 macrocell CPLD	reduced MIPS/clk due to only 4 inst
mcs-4	4004 CPU & MCS	alpha	Reece Pollack	4004	4	4													verilog	7	i4004			N		4K	4K	N				2012	2012	4004 data sheets	4004 was multi-chip	
mcu8	8-bit microcontr	sim?	Dimo Pepelyashev		8														vhdl	16	processor_E		asm												asm, simulated	
micro8a		beta	John Kent	accum	8	16	kintex-7	Xilinx		531	6			204	14.7	0.33	3.0	42	vhdl	11	Micro8	yes		N	N	2K	2K	Y				2002	2002	members.optushome	derived from Tim Boscke's mcpu, not perfected	
micro16b		beta	John Kent	accum	16	16	kintex-7	Xilinx		205	6			434	14.7	0.33	2.0	349	vhdl	1	u16bcpu	yes	asm	N	N	64K	4K	Y	8			2002	2008	members.optushome	very limited inst set	MIPS/clk adj'd, 2 clks/inst
micro16b		beta	John Kent	accum	16	16	spartan-3E	Xilinx		467	4		3	76	14.7	0.33	2.0	27	vhdl	13	Micro16b	yes	asm	N	N	64K	4K	Y	8			2002	2008	members.optushome	SOC version, very limited inst set	MIPS/clk adj'd, 2 clks/inst
microblaze		proprieta	Xilinx	uBlaze	32	32	kintex-7	Xilinx		1201	6		32	408		1.30	1.0	441	not avail			yes	yes	opt		32	32	Y	86	32	5	2002		www.xilinx.com/tools	performance optimized	70 configuration options, MMU optional
microblaze		proprieta	Xilinx	uBlaze	32	32	kintex-7	Xilinx		546	6		1	264		1.03	1.0	498	not avail			yes	yes	opt		32	32	Y	86	32	3	2002		www.xilinx.com/tools	area optimized	70 configuration options, MMU optional
microcore		beta	Klaus Schleisiek	forth	32	8	spartan-6-3	James Brakef		591	6		1	71	14.7	1.00	1.0	120	vhdl	10	core	yes	asm	N		2M	512K					2004			good documentation	
microriscii	MicroRISC II	alpha	Alikat	RISC	32	32													verilog	7	?			N		64K	64K	Y		16	5	2002	2009		very little code	
minimips	miniMIPS	stable	Poppy etal	MIPS	32	32	kintex-7-3	James Brakef		2939	6	8		118	14.7	1.00	1.0	40	vhdl	12	minimips	yes	yes	N		4G	4G	Y		32	5			MIPS I		
minirisc	Mini-Risc core	stable	Rudolf Usselmann	PIC16	8	14	spartan-3	Rudolf Usselr		460	4			80		0.33	1.0	57	verilog	7	risc_core	yes	yes	N	Y	256	4K	Y				2001	2012	PIC16 data sheets		
minsoc	minsoc	stable	Raul Fajardo etal	OpenRISC	32	32	kintex-7-3	James Brakef		4945	6	4	8	107	14.7	1.00	1.0	22	verilog	88	or1200_t	yes	yes	Y	M	4G	4G	Y		32		2009	2013	www.minsoc.com	minimal OR1200, vendor neutral, has caches	
mips_16	Educational 16-b	stable	Doyya Doyya	RISC	16	16	kintex-7-3	James	collapsed in c		6				14.7	1.00	1.0	####	verilog	12	mips_16	yes		N		64K	64K		13	8	5	2012	2012			
mips_enhanc	MIPS_enhanced	stable	Lazaridis Dimitris, Ioan	SPARC	32	32			difficult to find min design								1.0		vhdl		leon3mp	yes	yes	N		4G	4G	Y		32		2010	2011	tar file does not matc	based on mips789, added cache?? Only source is for Leon3	
mips_fault_t	Mips-FaultTolera	stable	Lazaridis	MIPS	32	32											1.0		vhdl			yes	yes	N		4G	4G	Y		32		2013		MIPS data sheets	arithmetic includes fault detection	
mips32r1	MIPS32 Release	stable	Grant Ayers	MIPS	32	32	kintex-7-3	James Brakef		4822	6	8		90	14.7	1.00	1.0	19	verilog	20	processor	yes	yes	N		4G	4G	Y		32		2012	2014	MIPS data sheets	Harvard arch	
mipsr2000	mipsr2000	stable	Lazaridis Dimitris	MIPS	32	32	kintex-7-3	James Brakef		1971	6	4	6	71	14.7	1.00	1.0	36	vhdl	35	Dm	yes	yes	N		4G	4G	Y		32	5	2012	2013	MIPS data sheets	course project	
mips789	mips789	stable	Li Wei	MIPS	32	32	kintex-7-3	James Brakef		1432	6		1	171	14.7	1.00	1.0	119	verilog	10	mips_cor	yes	yes	N		4G	4G	Y		32		2007	2009	MIPS data sheets		
mproz		stable		RISC	16	16													schematic			yes	asm	N			32K					1999			little documentation, CPLD implementation	
mpx	MPX 32-bit CPU	stable	Ultra Embedded		32	32													verilog					N		4G	4G	Y		32		2012	2013		GCC tools, no Verilog	
msl16		beta	Philip Leong, Tsang, Le	forth	16	4	kintex-7-3	James Brakef		303	6			256	14.7	0.67	1.0	566	vhdl	13	cpu	yes	asm	N		256						2001			CPLD prototype	
myblaze	myBlaze	mature	Jian Luo	uBlaze	32	32											1.0		myhdl			yes	yes	N		4G	4G	Y		32		2010	2010	microBlaze data shee	clone, no VHDL in tar file	
myforthproc	FORTH processo	stable	Gerhard Hohner	forth	32		spartan-3	James	xilinx primitive		4				14.7	1.00	1.0	####	vhdl	51	mycpu	yes	yes	Y								2012	2012		DPANS'94 32-bit Forth, masters thesis, four variants	
myrisc1	myRISC1	stable	Muza Byte	RISC	8	8													no files					N		256	256	Y		4		2011	2011			
natalius_8bit	Natalius 8 bit RIS	beta	Fabio Guzman	RISC	8	16	spartan-3-4	James Brakef		418	4		4	64	14.7	0.33	1.0	50	verilog	12	natalius_	yes	asm	N		32	2K	Y		8		2012	2012		return stack & register file	
natalius_8bit	Natalius 8 bit RIS	beta	Fabio Guzman	RISC	8	16	kintex-7-3	James Brakef		232	6		1	175	14.7	0.33	1.0	249	verilog	12	natalius_	yes	asm	N		32	2K	Y		8		2012	2012		return stack & register file	
navre	Navre AVR clone	stable	Sebastien Bourdeaudu	AVR	8	16	cyclone-4-6	James Brakef		1561	4			113	13.1	0.33	1.0	24	verilog	1	softusb_r	yes	yes	N		64K	64K	Y		32	2	2010	2013	AVR data sheets	AVR clone, part of www.milkymist.org	
navre	Navre AVR clone	stable	Sebastien Bourdeaudu	AVR	8	16	arria-2	James Brakef		1126	A			182	13.1	0.33	1.0	53	verilog	1	softusb_r	yes	yes	N		64K	64K	Y		32	2	2010	2013	AVR data sheets	AVR clone, part of www.milkymist.org	
navre	Navre AVR clone	stable	Sebastien Bourdeaudu	AVR	8	16	cyclone-5	James Brakef		783	A			115	13.1	0.33	1.0	49	verilog	1	softusb_r	yes	yes	N		64K	64K	Y		32	2	2010	2013	AVR data sheets	AVR clone, part of www.milkymist.org	
navre	Navre AVR clone	stable	Sebastien Bourdeaudu	AVR	8	16	spartan-6-3	James Brakef		1038	6			116	14.7	0.33	1.0	37	verilog	1	softusb_r	yes	yes	N		64K	64K	Y		32	2	2010	2013	AVR data sheets	AVR clone, part of www.milkymist.org	
navre	Navre AVR clone	stable	Sebastien Bourdeaudu	AVR	8	16	kintex-7-3	James Brakef		990	6			207	14.7	0.33	1.0	69	verilog	1	softusb_r	yes	yes	N		64K	64K	Y		32	2	2010	2013	AVR data sheets	AVR clone, part of www.milkymist.org	
ncore	nCore	alpha	Stefan Istvan	RISC	8	8													verilog	3	nCore	yes		N					16	16		2006	2009			

_uP_cores_test folder	opencores name	status	author	style / clone	data size	inst size	FPGA	reporter	comment	LUTs ALM	LUT7	mults	blk ram	F max	tool ver	MIPS /clk	clks/ inst	KIPS /LUT	src code	# src files	top file	doc	tool chain	fltg pt	Hardvd	max data	max inst	byte adrs	# inst	# reg	pipe len	start year	last revis	reference	note worthy	comments
neptune-core	The Neptune Co	planning	Llama																no source													2003	2009		single schematic	
next186	Next 80186 proc	stable	Nicolae Dumitrache	8086	8x	8x	arria-2	James Brakef		1966	6	1		83	14.7	0.33	1.0	14	verilog	4	Next186_	yes	yes	N	N	1M	1M	Y				2012	2013	x86 data sheets	boots DOS	
next186	Next 80186 proc	stable	Nicolae Dumitrache	8086	8x	8x	spartan-6-3	James Brakef		2716	6	1		44	14.7	0.33	1.0	5	verilog	4	Next186_	yes	yes	N	N	1M	1M	Y				2012	2013	x86 data sheets	boots DOS	
next186	Next 80186 proc	stable	Nicolae Dumitrache	8086	8x	8x	kintex-7-3	James Brakef		2500	6	1		94	14.7	0.33	1.0	12	verilog	4	Next186_	yes	yes	N	N	1M	1M	Y				2012	2013	x86 data sheets	boots DOS	
nextz80	NextZ80	stable	Nicolae Dumitrache	Z80	8	8x	kintex-7-3	James Brakef		1064	6			106	14.7	0.67	1.0	66	verilog	3	NextZ80C	yes	yes	N	N	64K	64K	Y				2011	2014	z80 data sheets		
nige_machine		stable	Andrew Read	forth	32	8			unable to find files								1.0		vhdl	29	CPU	yes	yes	N		16M	16M		512	512			2014		standalone Forth system	
nios2		proprietar	Altera	Nios II	32	32	cyclone-4-6	Altera		2065	4			160		1.13	1.0	87	no source			yes	yes	opt		4G	4G	Y		32		2004		NIOS2 data sheets	fltg-pt, caches & MMU options	Nios II/f: fastest version
nios2		proprietar	Altera	Nios II	32	32	arria-2	Altera		1355	A			170		1.13	1.0	141	no source			yes	yes	opt		4G	4G	Y		32		2004		NIOS2 data sheets	fltg-pt, caches & MMU options	Nios II/f: fastest version
nios2		proprietar	Altera	Nios II	32	32	cyclone-5	Altera		1050	A			160		1.13	1.0	171	no source			yes	yes	opt		4G	4G	Y		32		2004		NIOS2 data sheets	fltg-pt, caches & MMU options	Nios II/f: fastest version
nios2		proprietar	Altera	Nios II	32	32	arria-5	Altera		1355	A			280		1.13	1.0	232	no source			yes	yes	opt		4G	4G	Y		32		2004		NIOS2 data sheets	fltg-pt, caches & MMU options	Nios II/f: fastest version
nios2		proprietar	Altera	Nios II	32	32	stratix-5	Altera		895	A			310		1.13	1.0	390	no source			yes	yes	opt		4G	4G	Y		32		2004		NIOS2 data sheets	fltg-pt, caches & MMU options	Nios II/f: fastest version
nios2		proprietar	Altera	Nios II	32	32	cyclone-4-6	Altera		1915	4			130		0.64	1.0	43	no source			yes	yes	opt		4G	4G	Y		32		2004		NIOS2 data sheets	fltg-pt, caches & MMU options	Nios II: balanced version
nios2		proprietar	Altera	Nios II	32	32	arria-2	Altera		1045	A			170		0.64	1.0	103	no source			yes	yes	opt		4G	4G	Y		32		2004		NIOS2 data sheets	fltg-pt, caches & MMU options	Nios II: balanced version
nios2		proprietar	Altera	Nios II	32	32	cyclone-5	Altera		785	A			140		0.64	1.0	113	no source			yes	yes	opt		4G	4G	Y		32		2004		NIOS2 data sheets	fltg-pt, caches & MMU options	Nios II: balanced version
nios2		proprietar	Altera	Nios II	32	32	arria-5	Altera		1045	A			250		0.64	1.0	152	no source			yes	yes	opt		4G	4G	Y		32		2004		NIOS2 data sheets	fltg-pt, caches & MMU options	Nios II: balanced version
nios2		proprietar	Altera	Nios II	32	32	stratix-5	Altera		650	A			300		0.64	1.0	293	no source			yes	yes	opt		4G	4G	Y		32		2004		NIOS2 data sheets	fltg-pt, caches & MMU options	Nios II: balanced version
nios2		proprietar	Altera	Nios II	32	32	cyclone-4-6	Altera		1080	4			170		0.15	1.0	24	no source			yes	yes	N		4G	4G	Y		32		2004		NIOS2 data sheets	serial arithmetic	Nios II/e: minimum LUTs version
nios2		proprietar	Altera	Nios II	32	32	arria-2	Altera		730	A			300		0.15	1.0	62	no source			yes	yes	N		4G	4G	Y		32		2004		NIOS2 data sheets	serial arithmetic	Nios II/e: minimum LUTs version
nios2		proprietar	Altera	Nios II	32	32	cyclone-5	Altera		420	A			200		0.15	1.0	71	no source			yes	yes	N		4G	4G	Y		32		2004		NIOS2 data sheets	serial arithmetic	Nios II/e: minimum LUTs version
nios2		proprietar	Altera	Nios II	32	32	arria-5	Altera		730	A			320		0.15	1.0	66	no source			yes	yes	N		4G	4G	Y		32		2004		NIOS2 data sheets	serial arithmetic	Nios II/e: minimum LUTs version
nios2		proprietar	Altera	Nios II	32	32	stratix-5	Altera		445	A			340		0.15	1.0	115	no source			yes	yes	N		4G	4G	Y		32		2004		NIOS2 data sheets	serial arithmetic	Nios II/e: minimum LUTs version
oc54x	OpenCores54x D	beta	Richard Herveille	C54x	16	16													verilog	10	oc54_cpu	yes	yes	N	Y	64K	64K					2002	2009	C54x data sheets	incomplete source code	
octavo		beta	Charles LaForest	reg	16	16	stratix-4	Charles LaFor		500	A	1		550		0.67	1.0	737	verilog	18	Octavo	yes	asm	N					14	16	10		2012	Octavo: an FPGA-Cent	8 core barrel, adjustable data width	~= performance across word sizes, no call/rtn in
oks8	oks8	alpha	Kongzilee	ARM7	32	32											1.0		verilog	8	oks8	yes	yes	N		64K	64K	Y				2006	2009		clone of KS86C4204/C4208/P4208, SAM87RI instruction set	
oops	OoOPs Out-of-O	planning	Joshua Smith	MIPS	32	32													verilog	13		yes	yes	N		4G	4G	Y		32		2012	2012		incomplete source code	
open8_urisc	Open8 uRISC	stable	Kirk Hays, Jshamlet	RISC	8	8	kintex-7-3	James Brakef		691	6	1		263	14.7	0.33	1.0	126	VHDL	9	Open8	yes	yes	N		64K	64K	Y		8		2006	2013		accum & 8 regs, clone of Vautomation uRISC processor, in use	
opencpu32	OpenCPU32	planning	Leonardo Araujo dos Dantos		32	32													vhdl	22	pkgOpenCPU32			N						16		2012	2012		built to test division algorithms	
openfire_cor	OpenFire Proces	alpha	Alex Marschner, Stephe	uBlaze	32	32	kintex-7-3	James	empty project		6				14.7	0.33	1.0	####	verilog	12	openfire_	yes	yes	N	N	4G	4G	Y		32		2007	2009	uBlaze data sheets	"FPGA Proven"	
openmsp430	openMSP430	stable	Oliver Girard	msp430	16	16x	cyclone-4-6	Oliver Girard		1750	A	1		52		0.67	1.0	20	verilog	30	openMSP	yes	yes	N	N	64K	64K	Y		16		2009	2014	msp430 data sheets	implemented on four FPGAs, performance spreadsheet	
openmsp430	openMSP430	stable	Oliver Girard	msp430	16	16x	stratix-3-2	Oliver Girard		1147	A	1		98		0.67	1.0	57	verilog	30	openMSP	yes	yes	N	N	64K	64K	Y		16		2009	2014	msp430 data sheets	implemented on four FPGAs, performance spreadsheet	
openmsp430	openMSP430	stable	Oliver Girard	msp430	16	16x	spartan-6-4	Oliver Girard		1424	6	1		68		0.67	1.0	32	verilog	30	openMSP	yes	yes	N	N	64K	64K	Y		16		2009	2014	msp430 data sheets	implemented on four FPGAs, performance spreadsheet	
openmsp430	openMSP430	stable	Oliver Girard	msp430	16	16x	virtex-6-3	Oliver Girard		1387	6	1		116		0.67	1.0	56	verilog	30	openMSP	yes	yes	N	N	64K	64K	Y		16		2009	2014	msp430 data sheets	implemented on four FPGAs, performance spreadsheet	
or1200_hp	OpenRisc 1200 H	stable	Strauch Tobias	OpenRISC	32	32	kintex-7-3	James	1 slot barrel		6				14.7	1.00	1.0	####	verilog	39	or1200_i	yes	yes	Y		4G	4G	Y		32		2010	2013		original version of OR1200	
or1200_hp	OpenRisc 1200 H	stable	Strauch Tobias	OpenRISC	32	32	kintex-7-3	James	2 slot	went d	6				14.7	1.00	1.0	####	verilog	39	or1200_i	yes	yes	Y		4G	4G	Y		32		2010	2013		2 slot barrel version of OR1200	
or1200_hp	OpenRisc 1200 H	stable	Strauch Tobias	OpenRISC	32	32	kintex-7-3	James	3 slot barrel		6				14.7	1.00	1.0	####	verilog	39	or1200_i	yes	yes	Y		4G	4G	Y		32		2010	2013		3 slot barrel version of OR1200	
or1200_hp	OpenRisc 1200 H	stable	Strauch Tobias	OpenRISC	32	32	kintex-7-3	James	4 slot barrel		6				14.7	1.00	1.0	####	verilog	39	or1200_i	yes	yes	Y		4G	4G	Y		32		2010	2013		4 slot barrel version of OR1200	
or1k-cf	Confluence Ope	alpha	Kenr	OpenRISC	32	32													confluence													2004	2009			
or1k	OpenRISC	stable	Adam Edvardsson etal	OpenRISC	32	32											1.0		verilog			yes	yes	N		4G	4G	Y		32		2001	2014		extensive documentation, source code elusive	
or2k	OpenRISC 2000	planning	Marcus Erlandsson etal		32	32													no source																	
ourisc	16-bit Open uRIS	alpha	Joao Carlos		16	16	stratix-4	Joao Carlos		500	A	1		550		0.67	1.0	737	vhdl										26			2013	2013		very incomplete source code	
p16		alpha	Don Golding	forth	16	5	kintex-7-3	James	bad syntax		6				14.7	0.67	1.0	####	vhdl	1	p16			N		64K	64K					2000				
p16c5x	P16C5x	mature	Michael Morris	PIC16	8	14	spartan-3	Michael Mor		488	4		3	60		0.33	1.0	41	verilog	3	P16C5x	yes	yes	N	Y	256	4K	Y				2013	2014	PIC16 data sheets		
pacoBlaze		mature	Pablo Kocik	picoBlaze	8	18	spartan-3	Pablo Kocik		177	4		1	117		0.33	1.0	218	verilog	18	pacoblaze	yes	asm			8	11	Y	57		2		2006	bleyer.org/pacoblaze	3 versions, behavioral coding	
pavr	pAVR	alpha	Doru Cuturela	AVR	8	16													vhdl	8		yes	yes	N		64K	64K	Y		32	6	2003	2009	AVR data sheets	simulation only, is ASIC project	
pdp11-34verilog		stable	Brad Parker	PDP11	8x	16x	kintex-7-3	James Brakef		3089	6			153	14.7	0.67	1.0	33	verilog	24	pdp11	yes	yes	N	N	64K	64K			8		2009		PDP11 data sheets	boots & runs RT-11, EIS inst & MMU	www.heeltoe.com/download/pdp11/README.t
pdp8	PDP-8 Processor	alpha	Joe Manojlovick, Rob D	PDP8	12	12	spartan-6-3	James Brakef		1332	6	1		81	14.7	0.50	2.0	15	vhdl	55	cpu	yes	yes	N	N	32K	32K			8		2012	2013	PDP8 data sheets	Boots OS/8, runs apps, several variants	
pdp8	PDP-8 Processor	alpha	Joe Manojlovick, Rob D	PDP8	12	12	kintex-7-3	James Brakef		1219	6	1		183	14.7	0.50	2.0	37	vhdl	55	cpu	yes	yes	N	N	32K	32K			8		2012	2013	PDP8 data sheets	Boots OS/8, runs apps, several variants	
pdp8l	Minimal PDP8/L	beta	Ian Schofield	PDP8	12	12	cyclone-3	James Brakef		1088	4			107	14.7	0.50	2.0	24	vhdl	11	top	yes	yes	N	N	4K	4K					2013		PDP8 data sheets		
pdp8verilog		stable	Brad Parker	PDP8	12	12	spartan-6-3	James Brakef		509	6			162	14.7	0.50	2.0	79	verilog	18	pdp8	yes	yes	N	N	32K	32K			8		2005	2010	PDP8 data sheets	boots & runs TSS/8 & Basic	www.heeltoe.com/download/pdp8/README.ht
pdp8verilog		stable	Brad Parker	PDP8	12	12	kintex-7-3	James Brakef		505	6			366	14.7	0.50	2.0	181	verilog	18	pdp8	yes	yes	N	N	32K	32K			8		2005	2010	PDP8 data sheets	boots & runs TSS/8 & Basic	www.heeltoe.com/download/pdp8/README.ht
pdp8verilog		stable	Brad Parker	PDP8	12	12	kintex-7-3	James Brakef		1117	6			251	14.7	0.50	2.0	56	verilog	18	top	yes	yes	N	N	32K	32K			8		2005	2010	PDP8 data sheets	boots & runs TSS/8 & Basic	www.heeltoe.com/download/pdp8/README.ht
pepelatz_mis	Pepelatz MISC	planning	Myname IsTeapot	MISC															verilog	1															insignificant source	
pic_coonan		alpha	Tom Coonan	PIC16	8	14													vhdl			yes	yes	N	Y	256	4K	Y				1999		PIC16 data sheets		
picoblaze	picoblaze	stable	Ken Chapman	picoBlaze	8	18	spartan-3-4	James Brakef		178	4			182	14.7	0.33	1.0	338	vhdl	1	kcspm3	yes	asm	N		256	2K	Y				2003		picoblaze data sheets	2 clocks per inst	this is the original picoBlaze author
plasma	Plasma most MI	stable	Steve Rhoads	MIPS	32	32	kintex-7-3	James Brakef		2462	6		3	97	14.7	1.00	1.0	40	vhdl	22	plasma	yes	yes	N		4G	4G	Y		32		2001	2013	MIPS data sheets	wide outside use, opencores page has list of related publications	
popcorn		stable	Jeung Joon Lee	accum	8	8x	spartan-6-3	James Brakef		268	6			171	14.7	0.33	1.0	211	verilog	4	pc	yes		N		64K	64K	Y	43			2000			small 8 bit uP	
ppx16	PPX16 mcu	stable	Daniel Wallner	PIC16	8	14	spartan-6-3	James	missing ROM BB						14.7		1.0		vhdl	10	P16C55, F	yes	yes	N	Y	256	4K	Y				2002	2009	PIC16 data sheets	both 16C55 & 16F84	
qrisc32	qrisc32 wishbon	alpha	Viacheslav	RISC	32	32			system verilog source										system v	8	qrisc32	yes	yes	Y		4G	4G	Y		32	4	2010	2011		for PhD thesis	
r2000	r2000 Soc	alpha	Abdallah Ellbrahimi	RISC	32	32													verilog																empty tar file	
raptor64	Raptor64	planning	Robert Finch	RISC	64	32	kintex-7-3	James	missing port n		6				14.7	1.50	1.0	####	verilog	48	Raptor64	yes	yes	Y		2<<64	2<<64	Y		32		2012	2013		8-16-32-64 bit data, cache, MMU, hyper-threaded version also	
recore54		beta	ht-lab.com	PIC16	8	14	kintex-7-3	James	Cannot find <c		6				14.7	0.33	1.0	####	vhdl	20	rcore54_s	yes	yes	N	Y	256	4K	Y				1999		PIC16 data sheets	PIC16 clone	www.ht-lab.com
rtf8088	rtf8088	planning	Robert Finch	8086	8x	8x	kintex-7-3	James Brakef		4514	6	4		174	14.7	0.67	1.0	26	verilog	57	rtf8088	yes	yes	N	N	1M	1M	Y				2012	2013	x86 data sheets		
risc_core_i	RISC_Core_I	planning	Manuel Imhof	RISC	16	16	kintex-7-3	James Brakef		349	6	1		717	14.7	0.67	1.0	1377	vhdl	13	CPU	yes	asm	N		1K	1K			8	4	2001	2009		Havard arch	dubious Fmax
risc0		beta	Niklaus Wirth	RISC	32	32	kintex-7-3	James Brakef		1186	6	4	6	110	14.7	0.67	1.0	62	verilog	8	RISC0	yes	yes	N		4G	4G					2011			minimalist Wirth, education tool	
risc16f84	risc16f84	stable	John Clayton	PIC16	8	14	kintex-7-3	James Brakef		331	6			333	14.7	1.00	1.0	1007	verilog	1	risc16f84	yes	yes	N	Y	256	4K	Y				2002	2013	PIC16 data sheets	derived from CQPIC by Sumio Morioka	
risc5		beta	Niklaus Wirth	RISC	32	32	kintex-7-3	James	missing prom		6	4	6		14.7	1.00	1.0	####	verilog	17	RISC5Top	yes	yes	Y		4G	4G					2013			minimalist Wirth, part of Project Oberon 2013	
risc5x	RISC5x	stable	MikeJ	PIC16	8	14	kintex-7-3	James	errors in using		6				14.7	0.33	1.0	####	vhdl	15	cpu	yes	yes	N	Y	256	4K	Y				2002	2011	PIC16 data sheets	makes extensive use of xilinx primitives	
riscmcu	RISC Microcontr	stable	Yapzihe	AVR	8	16	arria-2	James	LPM paramete		6				14.7	0.33	1.0	####	vhdl	15	v_riscmcu	yes	yes	N		128	512	Y	92	16		2002	2009	AVR data sheets		
rise	RISE Microproce	beta	Jlechner etal	RISC	16	16	kintex-7-3	James	missing blox b		6	1			14.7	0.67	1.0	####	vhdl	26	rise	yes	asm	N		64K	64K			16	5	2006	2010	en.wikiversity.org/wil	ARM style register usage	
rtf65002	RTF65002	planning	Robert Finch	accum	32	8x													verilog	47	rtf65002_	yes		N		4G	4G	Y		16		2013	2013		32-bit 6502 + 6502 emulation	
s1_core	S1 Core	stable	Fabrizio Fazzino etal	SPARC	64	32	kintex-7-3	James Brakef		54434	6	8	57	50	14.7	1.00	1.0	1	verilog	136	s1_top	yes	yes	N	M	4G	4G	Y		32		2007	2012	SPARC data sheets	reduced version of OpenSPARC T1	
sayeh_proce	SAYEH education	stable	Alireza Haghdoost, Arm	RISC	16	16	kintex-7-3	James Brakef		479	6	1		164	14.7	0.67	1.0	230	verilog	13	Sayeh	yes		N		64K	64K			32		2008	2009	haghdoost.persiangig	simple RISC	
scarts	Scarts Processor	beta	Jlechner, Martin Walte	RISC	16	16	kintex-7-3	James	missing signal		6				14.7	0.67	1.0	####	vhdl	18	scarts		yes	N		64K	64K		122	16	4	2011	2012		GCC compiler	
secretblaze		beta	Lyonel Barthe	uBlaze	32	32	spartan-3-4	Lyonel Barthe		1563	4			91	12.1	1.00	1.0	58	vhdl	26	sb_core		yes			4G	4G	Y	86	32	5	2010	2012	www.lirmm.fr/ADAC/		
sparcv8coprc	Coprocessor-rea	planning	Nicholas Voorsanger	SPARC	32	32													no files													2012		SPARC data sheets		
ssbcc	Smal Stack Based	stable	Rodney Sinclair	forth	8	9			syntax errors								1.0		verilog	3	core	yes	asm	N				Y				2012	2014		Python program generates the Verilog	
storm_core	Storm Core (ARM	beta	Stephan Nolting	ARM7	32	32	kintex-7-3	James Brakef		2312	6	3		179	14.7	1.00	1.0	77	vhdl	16	CORE	yes	yes	N	N	4G	4G	Y		32	8	2011	2013		I & D caches not compiled	
storm_core	Storm Core (ARM	beta	Stephan Nolting	ARM7	32	32	kintex-7-3	James Brakef		3514	6	3	4	157	14.7	1.00	1.0	45	vhdl	16	STORM_T	yes	yes	N	M	4G	4G	Y		32	8	2011	2013		I & D caches	
sub86	Small x86 subset	alpha	Jose Rissetto	8086	8x	8x													verilog	1	sub86	yes	yes	N	N	64K	64K	Y		7		2012	2013		no segment registers, limited op-codes	
sxp	SXP (Simple eXte	beta	Sam Gladstone etal	RISC	32	32			too many los										verilog		sxp			N		4G	4G			32		2001	2009		basic RISC	too many los
system05	SOC:system05	beta	John Kent	6805	8	8x	kintex-7-3	James Brakef		834	6			204	14.7	0.33	1.0	81	vhdl	10	System05	yes	yes	N	N	64K	64K	Y				2003	2009	6805 data sheets		
system09	SOC:system09	stable	John Kent	6809	8x	8x	spartan-6-3	James Brakef		2127	6			64	14.7	0.33	1.0	10	vhdl	40	cpu09l	yes	yes	N	N	64K	64K	Y				2003	2012	6809 data sheets	from John Kent web page	
system09	SOC:system09	stable	John Kent	6809	8x	8x	kintex-7-3	James Brakef		1945	6			154	14.7	0.33	1.0	26	vhdl	40	cpu09l	yes	yes	N	N	64K	64K	Y				2003	2012	6809 data sheets	from John Kent web page	
system11		alpha	John Kent, David Burne	6811	8	8x	kintex-7-3	James Brakef		1218	6			153	14.7	0.33	1.0	41	vhdl	17	cpu11	yes	yes	N	N	64K	64K	Y				2003	2009	6811 data sheets	known bugs & untested instructions	
system68	System68	stable	John Kent, David Burne	6801	8	8x	spartan-3-5	James Brakef		2235	4		4	46	14.7	0.33	1.0	7	vhdl	21	cpu68	yes	yes	N	N	64K	64K	Y				2003	2009	6801 data sheets		
t400	T400 uController	stable	Arnim Laeuger	COP400	4	8x	cyclone-1	Arnim Laeuge		583	4		2	59		0.17	1.0	17	vhdl	53	t400_core	yes	asm	N		256	1K					2006	2009	COP400 data sheets	several variants	
t400	T400 uController	stable	Arnim Laeuger	COP400	4	8x	spartan-2	Arnim Laeuge		643	4		2	60		0.17	1.0	16	vhdl	53	t400_core	yes	asm	N		256	1K					2006	2009	COP400 data sheets	several variants	
t48	T48 uController	stable	Arnim Laeuger	MCS-48	8	8x	cyclone-1	Arnim Laeuge		738	4		1	59		0.33	1.0	26	vhdl	70	t48_core	yes	asm	N		256	1K					2004	2009	MCS-48 data sheets	used in several projects	
t48	T48 uController	stable	Arnim Laeuger	MCS-48	8	8x	spartan-2	Arnim Laeuge		771	4		1	30		0.33	1.0	13	vhdl	70	t48_core	yes	asm	N		256	1K					2004	2009	MCS-48 data sheets	used in several projects	
t51	T51 mcu	alpha	Andreas Voggeneder	8051	8	8x	kintex-7-3	James Brakefield			6				14.7	0.33	1.0		vhdl	17	T8052	yes	yes	N	N	64K	64K	Y				2002	2010	8052 data sheets	8052 & 8032	
t65	T65 CPU	stable	Daniel Wallner	6502	8	8x	spartan-6-3	James Brakef		725	6			128	14.7	0.33	1.0	58	vhdl	7	T65	yes	yes	N	N	64K	64K	Y				2002	2010	6502 data sheets	6502, 65C02 & 65C816; wide use	

_uP_cores_test folder	opencores name	status	author	style / clone	data size	inst size	FPGA	reporter	comment	LUTs ALM	LUT?	mults	blk ram	F max	tool ver	MIPS /clk	clks/ inst	KIPS /LUT	src code	# src files	top file	doc	tool chain	fltg pt	Ha vd	max data	max inst	byte adrs	# inst	# reg	pipe len	start year	last revis	reference	note worthy	comments
t65	T65 CPU	stable	Daniel Wallner	6502	8	8x	kintex-7-3	James Brakef		575	6			291	14.7	0.33	1.0	167	vhdl	7	T65	yes	yes	N	N	64K	64K	Y				2002	2010	6502 data sheets	6502, 65C02 & 65C816; wide use	
t6507lp	T6507LP	beta	Gabriel Oshiro, Samuel	6502	8	8x	spartan-6-3	James	errors						14.7		1.0		verilog	22	t6507lp	yes	yes	N	N	64K	64K	Y				2009	2010	6502 data sheets	for use in ATARI 2600	
t80	T80 cpu	stable	Daniel Wallner	8080	8	8x	spartan-6-3	James	8080 I	958	6			95	14.7	0.33	1.0	33	vhdl	16	T8080se	yes	yes	N	N	64K	64K	Y				2002	2011	z80 data sheets	Z80 & 8080 inst sets, several usage	
t80	T80 cpu	stable	Daniel Wallner	Z80	8	8x	spartan-6-3	James	Z80 m	1462	6			83	14.7	0.33	1.0	19	vhdl	16	T80a	yes	yes	N	N	64K	64K	Y				2002	2011	z80 data sheets	Z80 & 8080 inst sets, several usage	
t80	T80 cpu	stable	Daniel Wallner	Z80	8	8x	kintex-7-3	James Brakef		1389	6			163	14.7	0.67	1.0	79	vhdl	16	T80a	yes	yes	N	N	64K	64K	Y				2002	2011	z80 data sheets	Z80 & 8080 inst sets, several usage	
tg68	TG68 execute 68	stable	Tobias Gubener	68000	8x	16x	kintex-7-3	James Brakef		2331	6			44	14.7	0.67	1.0	13	vhdl	2	TG68_fas	yes	yes	N	N	4G	4G	Y		16		2007	2012	68000 data sheets	for use with Minimig	
theia_gpu	Theia: ray graph	beta	Diego Valverde	GPU													1.0		verilog	32	Theia	yes	asm	N						12		2011	2012		multi-core, 3D rendering & shader	
tiny64	Tiny64	stable	Ulrich Riedel	RISC	64		kintex-7-3	James	bit length mis		6				14.7	1.00	1.0	####	vhdl	7	TinyX		asm	N		64K	64K		16	8		2004	2009		word size configurable from 32 to 64	
tiny8	tiny8	mature	Ulrich Riedel	CISC	8x	8x											1.0		AHDL				asm	N		64K	64K	Y				2002	2009		registers in RAM like TMS9900, uses Altera AHDL, megafunctions & schematic entry	
tinycpu	TinyCPU	alpha	Jordan Earls	RISC	8	16													vhdl	10	top		asm	N		64K	64K			16		2012	2012			
tisc	Tiny Instruction	beta	Vincent Crabtree	accum	8	8x	spartan-6-3	James Brakef		198	6			60	14.7	0.33	1.0	100	vhdl	1	TISC			N		256	1K	Y		2		2009	2009		minimal accumulator machine	
totalcpu	TotalCPU	alpha		RISC	12+	12													verilog											16		2007	2009		data width 12 bits and up, no data memory	
turbo8051	turbo 8051	beta	Dinesh Annayya	8051	8	8x	cyclone-2	Dinesh Anna		5072	4			39	14.7	0.33	1.0	3	verilog	74	oc8051_t	yes	yes	N	N	64K	64K	Y				2011	2013	8051 data sheets	includes perpherials	
turbo8051	turbo 8051	beta	Dinesh Annayya	8051	8	8x	kintex-7-3	James Brakef		1985	6	1		127	14.7	0.33	1.0	21	verilog	74	oc8051_t	yes	yes	N	N	64K	64K	Y				2011	2013	8051 data sheets	includes perpherials	
tv80	TV80	mature	Guy Hutchison, Howar	Z80	8	8x	kintex-7-3	James Brakef		1207	6			182	14.7	0.67	1.0	101	verilog	6	tv80n	yes	yes	N	N	64K	64K	Y				2004	2012	z80 data sheets	derived from Daniel Wallner's T80, ASIC implementations	
ucore	Ucore	stable	Whitewill	MIPS	32	32	kintex-7-3	James Brakef		2469	6		1	231	14.7	1.00	1.0	93	verilog	25	ucore	yes	yes	N		4G	4G	Y		32	6	2005	2010	MIPS data sheets	MMU & caches	
usimplez	MicroSimplez	stable	Pablo Salvadeo etal	accum	12	12	stratix-2	Pablo Salvad		48	4			134	9.1	0.17	1.0	476	vhdl	3	usimplez_cpu			N		512	512		8			2011			von Neuman arch, Simplez processor	MIPS/Mhz reduced due to few inst
v1_coldfire		stable	IPextreme	68000	8x	16x	cyclone-3	freescale		5000	4			80		0.89	1.0	14				yes	yes	N	N	4G	4G	Y		16		2008		68000 data sheets	free for Cyclone III	
vtach	VTACH Bell Labs	mature	Al Williams		13	12	spartan-3-4	James Brakef		557	4			71	14.7	0.50	1.0	64	verilog	16	vtach			N		256	256	Y				2913	2013		ISE project only, BCD arithmetic	
vtach	VTACH Bell Labs	mature	Al Williams		13	12	kintex-7-3	James	xilinx core pro		6				14.7	0.50	1.0	####	verilog	16	vtach			N		256	256	Y				2913	2013		ISE project only, BCD arithmetic	
w11	PDP-11/70 CPU	alpha	Walter Mueller	PDP11	8x	16x	spartan-6	Walter Muell		3418	6			80		0.67	1.0	16	vhdl	26	pdp11	yes	yes	N	N	4M	4M	Y		8		2010	2013	PDP11 data sheets	Boots UNIX, has MMU & cache, retro project	
wb_z80	Wishbone High	stable	Brewster Porcella	Z80	8	8x	kintex-7-3	James Brakef		2025	6			144	14.7	0.67	1.0	48	verilog	4	z80_core	yes	yes	N	N	64K	64K	Y				2004	2012	z80 data sheets	derived from Guy Hutchison TV80	
wb4pb	Software Aided	stable	Stefan Fischer	picoBlaze	13	13													vhdl & v	10					Y							2010	2013	picoblaze data sheets	software addon for picoBlaze	
x32		stable	Sijmen Woutersen	forth	32	8	kintex-7-3	James	missing define		6				14.7	1.00	1.0	####	vhdl	32	core	yes	yes	N		4G	4G	Y				2006	2007		MS thesis, byte code, needs caches	
xproz		stable	Herbert Kleebauer	CISC	16	16x											1.0		schematic			yes	asm	N		64K	64K					1995			documentation in German	
xr16		stable	Jan Gray	RISC	16	16	kintex-7-3	James Brakef		371	6			7	14.7	0.67	1.0	13	verilog	12	xsoc	yes		N		64K	64K			16		1999	2001		handcrafted FPGA layout & instruction set	
y80e	Y80e Z80/Z180 c	stable	Sergey Belyashov	Z80	8	8x	kintex-7-3	James	empty project		6				14.7	1.00	1.0	####	verilog	15	y80_top	yes	yes	N	N	64K	64K	Y				2013	2013	z80 data sheets	based on Y80 from "Microprocessor Design Using Verilog HDL" by Monte Dalryple	
yacc	YACC Yet Anothe	stable	Tak Sugawara	MIPS	32	32	kintex-7-3	James	xilinx IP proble		6				14.7	1.00	1.0	####	verilog	10	yacc2	yes	yes	N		4G	4G	Y		32	5	2005	2009	MIPS data sheets	derived from, but independent of plasma, xilinx & altera implemntations	
yasep		alpha	Yann Guidon	RISC	16	32	kintex-7-3	James	syntax errors		6				14.7	1.00	1.0	####	vhdl		microYAE	yes	asm	N			2K			16		2008	2014	www.yaesp.org	Java generated VHDL, revisions ongoir	funky web site
yellowstar	Yellow Star	stable	Charles Brej	MIPS	32	32			missing declarations										verilog	1	processor	yes	yes	N		4G	4G	Y		32		2001	2013	MIPS data sheets	MIPS R3000 clone, gate level dsgn	brej.org/yellow_star/
zet86	Zet The x86 (IA-3	alpha	Zeus Marmolejo	8086	8x	8x	kintex-7-3	James Brakef		3642	6	1		68	14.7	0.67	1.0	12	verilog	32	fpga_zet	yes	yes	N	N	1M	1M	Y				2008	2014	x86 data sheets	equivalent to 80186, boots MS-DOS	zet.aluzina.org/index.php/Zet_processor
zpu	ZPU the worlds s	stable	Oyvind Harboe	forth	32	8	spartan-6	Oyvind Harbo		1259	6			135		0.10	1.0	11	vhdl	23	zpu_core	yes	yes	N		4G	4G	Y	37			2008	2009	www.zylin.com	zpu4: 16 & 32 bit versions, code size 80% of ARM (thumb), low MIPs/MHz	
zpu	ZPU the worlds s	stable	Oyvind Harboe	forth	32	8	spartan-3	Oyvind Harbo		440	4			85		0.05	1.0	10	vhdl	23	zpu_core	yes	yes	N		4G	4G	Y	37			2008	2009	www.zylin.com	zpu4: 16 & 32 bit versions, code size 80% of ARM (thumb), low MIPs/MHz	

58 # usable(beta, stable or mature): "A"(clones) & "W"(originals) 70 # adr locations

38 "B" or "X" of limited interest

Web page DMIPS per clock cycle per core en.wikipedia.org/wiki/Instructions_ community.freescale, www.eembc.org/coremark/index.php

MIPS/MHz Pro-rating for data size:

1-bit	0.04
8-bit	0.33
16-bit	0.67
32-bit	1.00

Under the assumption that the core is capable of one instuction per clock

Silicon Area equivalents

LUTS/DSP48	16:1
LUTS/Block RAM	32:1

Following has DMIPS per clock for many microprocessors
http://en.wikipedia.org/wiki/Instructions_per_second

uP	MIPS			CoreMarks /MHz	MHz	
4004	0.10					
6502	0.50		0.02	0.06		
8051			0.08	0.24		
8080	0.17			0.25		
68K	0.10			0.15		
ARM Cortex A9	2.50	DMIPS		5.93	1000	
ARM Cortex M0	0.90	DMIPS		1.50	70	
ARM Cortex M3	1.25	DMIPS		2.92	25	
ARM7	0.90		0.74	2.04	600	
AVR	1.00		0.21	0.53	8	
AVR32				1.62	60	
BA21				2.44	400	
Coldfire				2.80	400	
Coldfire				0.77	150	Virtex-5
HCS08			0.04	0.12		
LEON3/Spartan-6				1.96	100	
MC6809	1.24		0.07	1.86		
MicroBlaze 3-stage	1.03			1.50		
MicroBlaze 5-stage	1.38			1.90	125	
MIPS32	1.51			2.28		
MSP430			0.40	1.20		
MSP430				1.10	25	
Nios II	0.64	DMIPS		0.93	200	
Nios II -e	0.15	DMIPS		0.25		
Nios II -f	1.13	DMIPS		1.60	200	
PIC16	0.25					
PIC18				0.04	40	
PIC24			0.72	1.86	40	
PIC32				3.45	80	
Super H-2				1.44	180	
VAX780	1.00	DMIPS		1.50		
Z80	1.60		0.01	0.03		
	2X		1X	3X		

Column Titles	Details
"A"	A: 1st choice clone, B: 2nd choice clone, W: 1st choice original, X: 2nd choice original
"B"	currently unused and hidden
_uP_cores_test folder	if opencores design is their folder name, otherwise my folder name
opencores name	
status	ASIC, planning, alpha, beta, stable, mature, proprietary
author	First Name, Last Name
style / clone	part number or "forth", RISC, accumulator, etc
data size	data memory word size
inst size	instruction size
FPGA	FPGA family for compile, place, route & timing
reporter	First Name, Last Name
comments	compile, place, route & timing problems
LUTs ALM	4-LUT, 6-LUT, Altera ALM, Actel Tile
LUT?	total number of LUTs or ALMs used including route-thrus & otherwise unavailable
mults	total number of multipliers/DSPs used
blk RAM	total number of block RAMs used, does not include small and extra large Altera block RAMs, Xilinx half block RAM rounded up
Fmax	maximum primary clock speed from compile, place, route & timing run
tool ver	Altera, Xilinx, Lattice Semiconductor or MicroSemi tool version number
MIPS /clk	prorated DMIPS per clock, reduced for data word sizes under 32-bits, greater than one for multiple issue processors
clks/ inst	number of clocks per instruction, typically 1.0 for modern pipelined processors
KIPS /LUT	figure of merit, does not include effects of memory capacity, floating point or instruction set quality
src code	VHDL or Verilog or other
# src files	number of source files for compile, place, route & timing
top file	top file for compile, place, route & timing run
doc	is documentation provided
tool chain	is there a compiler or assembler provided or available
fltg pt	does the compile, place, route & timing run include floating point
Ha vd	separate instruction and data memory(s), there can be more than one data memory, M for MMU & caches
max data	maximum data address
max inst	maximum instruction address
byte adrs	is byte addressing provided
# inst	number of unique instructions, somewhat subjective
# reg	number of registers in register file
pipe len	number of pipeline stages
start year	year of first design activity
last revis	last year for revisions
reference	web address or generic information (for clones)
note worthy	anything special about the design
comments	catchall