Small soft core uP Inventory **©2014 James Brakefield**

Opencore and other soft core processors

_uP_cores_test folder	opencores name	status	author	style / clone	data	inst size	FPGA	reporter	comment	LUTs ALM	LUT?	mults	blk ram	F max	tool ver	MIPS /clk	clks/ inst	KIPS /LUT	src code	# src files	top file	doc	tool chai	fltg pt	Hav	max data	max inst	byte adrs	# inst	# reg	pipe len	start year	last revis	reference	note worthy	comments
copyblaze	copyBlaze	stable	Abdallah Ellbrahim	picoBlaze	8	18	spartan-6-3	James Brakefiel		619	6			86		0.33	1.0	46	vhdl	16	cp_co	yes	asm	N		256	2K	Y				2011	2013	microBlaze data sheet	wishbone extras	LUT count high, Fmax low: see picobla
r2000	r2000 Soc	alpha	Abdallah Ellbrahim	RISC	32	32													verilog																empty tar file	
or1k	OpenRISC	stable	Adam Edvardsson e	OpenRISC	32	32											1.0		verilog			yes	yes	N		4G	4G	Y		32		2001	2014		extensive documentation, source code elusive	
blue	16-bit CPU Blue	stable	Al Williams	accum	16	16	spartan-6-3	James Br	missing file		6					0.67	1.0	#####	verilog	16	top	web		N		4K	4K	N	16	2		2009	2010		Caxton Foster's Blue derivative	http://www.youtube.com/watch?v=dt
vtach	VTACH Bell Labs	mature	Al Williams		13	12	spartan-3-4	James Brakefiel		557	4			71	14.7	0.50	1.0	64	verilog	16	vtach			N		256	256	Y				2913	2013		ISE project only, BCD arithmetic	
6809_6309	6809_6309_com	beta	Alejandro Paz Schm	6809	8x	8x	kintex-7-3	James Brakefiel		2207	6			212	14.7	0.33	1.0	32	verilog	5	MC6809_c	yes	N	N	64K	64K	Y				2012	2013	6809 data sheets	includes 6309 op-codes, xilinx & lattice projects	
ao68000	ao68000	beta	Aleksander Osman	68000	8x	16x	arria-2	James Brakefiel		3479	A		6	169	13.1	1.00	1.0	49	verilog	1	ao680	som	yes	N		4G	4G	Y				2010	2011	68000 data sheets	uses microcode, 4750 LUTs	
openfire_cor	OpenFire Proces	alpha	Alex Marschner, Ste	uBlaze	32	32	kintex-7-3	James Br	empty projec		6				14.7	0.33	1.0	#####	verilog	12	openf	yes	yes	N	N	4G	4G	Y		32		2007	2009	uBlaze data sheets	"FPGA Proven"	
gl85		stable	Alex Miczo	8085	8	8x	kintex-7-3	James Br	gate level de		6				14.7	0.33	1.0	#####	vhdl	1	i8085	yes	yes	N	N	64K	64K	Y				1993		8085 data sheets	also a TTL implementation in VHDL	
microriscii	MicroRISC II	alpha	Alikat	RISC	32	32													verilog	7	?			N		64K	64K	Y		16	5	2002	2009		very little code	
hmta	HyperMTA	planning	Alikat etal																no files					Y						64		2002	2009		up to 256 threads	
sayeh_proce	SAYEH educatior	stable	Alireza Haghdoost,	RISC	16	16	kintex-7-3	James Brakefiel		479	6	1		164	14.7	0.67	1.0	230	verilog	13	Sayeh	yes		N		64K	64K			32		2008	2009	haghdoost.persiangig.	simple RISC	
encore	Encore	planning	Aloy Ambergen																no files													2010	2011			
nios2		proprietar	Altera	Nios II	32	32	stratix-5	Altera		895	A			310		1.13	1.0	390	no source			yes	yes	opt		4G	4G	Y		32		2004		NIOS2 data sheets	fltg-pt, caches & MMU options	Nios II/f: fastest version
crisc_cpu	CRISC CPU	planning	Andre Adrian	68000 like	8x	16x													no files					N		4G	4G	Y	20	15		2011			see opencores web page: both 16-bit & 32-bit registers, 11 addressing mod	
af65k		alpha	Andre Fachat	6502	16	8x													vhdl			yes		N	N							2011			extended 6502 with 16, 32 or 64 bit data	
alwcpu	Alwcpu	alpha	Andreas Hilvarsson	RISC	16	16	kintex-7-3	James Brakefiel		298	6			237	14.7	0.67	1.0	533	vhdl	7	top	some		N		64K	64K	Y		16		2009	2009		400 LUTs	
avrtinyx61co	avrtinyx61core	beta	Andreas Hilvarsson	AVR	8	16	kintex-7-3	James Brakefiel		1243	6			194	14.7	0.33	1.0	51	vhdl	1	mcu_core	yes		N		64K	128K	Y		32		2008	2009	AVR data sheets		
t51	T51 mcu	alpha	Andreas Voggenede	8051	8	8x	kintex-7-3	James Brakefiel			6				14.7	0.33	1.0		vhdl	17	T8052	yes	yes	N	N	64K	64K	Y				2002	2010	8052 data sheets	8052 & 8032	
nige_machine		stable	Andrew Read	forth	32	8			unable to find files								1.0		vhdl	29	CPU	yes	yes	N		16M	16M		512	512			2014		standalone Forth system	
ARM_Cortex_A9		ASIC	ARM	ARM a9	32	16	arria V	altera		4500	A			1050		2.50	1.0	583	asic			yes	yes	Y		4G	4G	Y	80	16	10		2012	altera data sheets	uses pro-rated LC area	dual issue, includes fltg-pt & MMU & c
t400	T400 uController	stable	Arnim Laeuger	COP400	4	8x	cyclone-1	Arnim Laeuger		583	4		2	59		0.17	1.0	17	vhdl	53	t400_	yes	asm	N		256	1K					2006	2009	COP400 data sheets	several variants	
t48	T48 uController	stable	Arnim Laeuger	MCS-48	8	8x	cyclone-1	Arnim Laeuger		738	4		1	59		0.33	1.0	26	vhdl	70	t48_c	yes	asm	N		256	1K					2004	2009	MCS-48 data sheets	used in several projects	
edu_3bus_ar	Educational 3 Bu	spec	Ayman Mohamed	RISC	32	32													no files										33	32		2012	2013			
b16		stable	Bernd Paysan	forth	16	5	spartan-6-3	James Brakefiel		554	6			134		0.67	1.0	162	verilog	1	b16	yes	yes	N								2002	2011	bernd-paysan.de/b16.	two versions: one/15 source files, derived from c18	
lpu	LocationPU	planning	Bkorsedal																no files													2002	2009		very early: minimal doc	
pdp11-34verilog		stable	Brad Parker	PDP11	8x	16x	kintex-7-3	James Brakefiel		3089	6			153	14.7	0.67	1.0	33	verilog	24	pdp11	yes	yes	N	N	64K	64K			8		2009		PDP11 data sheets	boots & runs RT-11, EIS inst & MMU	www.heeltoe.com/download/pdp11/
pdp8verilog		stable	Brad Parker	PDP8	12	12	kintex-7-3	James Brakefiel		505	6			366	14.7	0.50	2.0	181	verilog	18	pdp8	yes	yes	N	N	32K	32K			8		2005	2010	PDP8 data sheets	boots & runs TSS/8 & Basic	www.heeltoe.com/download/pdp8/R
wb_z80	Wishbone High	stable	Brewster Porcella	Z80	8	8x	kintex-7-3	James Brakefiel		2025	6			144	14.7	0.67	1.0	48	verilog	4	z80_c	yes	yes	N	N	64K	64K	Y				2004	2012	z80 data sheets	derived from Guy Hutchison TV80	
cpu16		beta	C. H. Ting	forth	16	5	kintex-7-3	James Br	case c	367	6			355	14.7	0.67	1.0	648	vhdl	1	cpu16	yes	asm	N		64K	64K					2000			part of eForth?	
ba22		proprieta	CAST Inc	RISC	32	16x	spartan-6	CAST Inc		1800	6		32	72		1.00	1.0	40	not avail							4G	4G			32				www.cast-inc.com		
yellowstar	Yellow Star	stable	Charles Brej	MIPS	32	32			missing declarations										verilog	1	proce	yes	yes	N		4G	4G	Y		32		2001	2013	MIPS data sheets	MIPS R3000 clone, gate level dsgn	brej.org/yellow_star/
gullwing		simulatior	Charles LaForest	forth	32	5													no code			yes	asm	N		4K	4K					2007		BS thesis	virtual stack machines vs RISC	MuP21 clone
octavo		beta	Charles LaForest	reg	16	16	stratix-4	Charles LaFores		500	A	1		550		0.67	1.0	737	verilog	18	Octav	yes	asm	N					14	16	10		2012	Octavo: an FPGA-Cent	8 core barrel, adjustable data width	~= performance across word sizes, no
iDEA		proprietar	Cheah etal	RISC	16	32	virtex-6	Cheah		190	6	1	1	534		0.67	1.0	1883	not avail										20	32	9		2011	A Lean FPGA Soft Proc	by Xilinx, no source	
cray1		alpha	Christopher Fenton	cray1	64	16													verilog	42	cray_t	yes	yes	Y	N	4M	4M	N				2010		CRAY data sheets	homebrew Cray1	www.chrisfenton.com/homebrew-cra
amber	Amber ARM-cor	stable	Conor Santifort	ARM7	32	32	kintex-7-3	James Br	slow,	####	6		4	98	14.7	0.90	1.0	7	verilog	25	a25_c	yes	yes	N		4G	4G	Y				2010	2013	ARM7 data sheets	no MMU	4096 single port RAM LUTs
ax8	AX8 MCU	stable	Daniel Wallner	AVR	8	16	spartan-6-3	James Br	missing ROM		6				14.7		1.0		vhdl	14	A90S1200			N		64K	128K	Y		32		2002	2009	AVR data sheets	both A90S1200 & A90S2313	
ppx16	PPX16 mcu	stable	Daniel Wallner	PIC16	8	14	spartan-6-3	James Br	missing ROM BB						14.7		1.0		vhdl	10	P16C5	yes	yes	N	Y	256	4K	Y				2002	2009	PIC16 data sheets	both 16C55 & 16F84	
t65	T65 CPU	stable	Daniel Wallner	6502	8	8x	kintex-7-3	James Brakefiel		575	6			291	14.7	0.33	1.0	167	vhdl	7	T65	yes	yes	N	N	64K	64K	Y				2002	2010	6502 data sheets	6502, 65C02 & 65C816; wide use	
t80	T80 cpu	stable	Daniel Wallner	Z80	8	8x	kintex-7-3	James Brakefiel		1389	6			163	14.7	0.67	1.0	79	vhdl	16	T80a	yes	yes	N	N	64K	64K	Y				2002	2011	z80 data sheets	Z80 & 8080 inst sets, several usage	
agcnorm	Apollo Guidance	beta	Dave Roberts	?	16	16											1.0		vhdl	5	AGC	some		N		32M	32M					2010	2012		Apollo Guidance Computer via NOR gate emulation	
Lutiac		custom	David Galloway, Da	2 reg	16	NA	stratix-4	David Galloway		140	A	4		198		0.67	1.0	948	either								64	N	64	32	3		2010	Lutiac – Small Soft Pro	no inst RAM, instead microcode	no inst mem: small state machine, ~20
free6502		stable	David Kessner	6502	8	8x	spartan-6-3	James Brakefiel		663	6			89	14.7	0.33	1.0	44	vhdl	5	free65	yes	yes	N	N	64K	64K	Y				1999	2000	6502 data sheets	microcoded	
elm	ELM Embedded	alpha	David Sheffield, Curt Harting																no files													2010	2010			
1664	1664 microproce	sim?	Denis Godinho																C										26			2010	2010		C based simulation only	
theia_gpu	Theia: ray graph	beta	Diego Valverde	GPU													1.0		verilog	32	Theia	yes	asm	N						12		2011	2012		multi-core, 3D rendering & shader	
mcu8	8-bit microcontr	sim?	Dimo Pepelyashev		8														vhdl	16	processor_	asm													asm, simulated	
turbo8051	turbo 8051	beta	Dinesh Annayya	8051	8	8x	kintex-7-3	James Brakefiel		1985	6	1		127	14.7	0.33	1.0	21	verilog	74	oc805	yes	yes	N	N	64K	64K	Y				2011	2013	8051 data sheets	includes perpherials	
p16		alpha	Don Golding	forth	16	5	kintex-7-3	James Br	bad syntax		6				14.7	0.67	1.0	#####	vhdl	1	p16			N		64K	64K					2000				
pavr	pAVR	alpha	Doru Cuturela	AVR	8	16													vhdl	8		yes	yes	N		64K	64K	Y		32	6	2003	2009	AVR data sheets	simulation only, is ASIC project	
mips_16	Educational 16-b	stable	Doyya Doyya	RISC	16	16	kintex-7-3	James Br	collapsed in		6				14.7	1.00	1.0	#####	verilog	12	mips_	yes		N		64K	64K		13	8	5	2012	2012			
c0or1k	Codezero OpenR	planning	Drasko Draskovic	RISC															no code													2010			C code for simulation	
ensilica		proprieta	ensilica.com	eSi-3200	32		stratix-4	ensilica		1800	A			200		1.00	1.0	111	not avail			yes	yes			4G	4G			16	5			www.ensilica.com	verilog source included with license	10 addressing modes
eric5		proprieta	enter-electronics.co	forth	9	8	cyclone-4-6	enter-electroni		110	4	opt		60		0.42	1.0	229	not avail							512	1K			3-4		2007			25 MIPS: ERIC5xs, ERIC5Q	
hive	hive	stable	Eric Wallin	4-8 stack	32	16	cyclone-5	Eric Wallin		1877	4	4	3	226		1.00	1.0	120	verilog			yes		N				N	40	10	8	2013	2014		4-8 symetrical stacks, eight threads via pipeline barrel	
natalius_8bit	Natalius 8 bit RIS	beta	Fabio Guzman	RISC	8	16	kintex-7-3	James Brakefiel		232	6		1	175	14.7	0.33	1.0	249	verilog	12	natali	yes	asm	N		32	2K	Y		8		2012	2012		return stack & register file	
s1_core	S1 Core	stable	Fabrizio Fazzino eta	SPARC	64	32	kintex-7-3	James Brakefiel		####	6	8	57	50	14.7	1.00	1.0	1	verilog	136	s1_top	yes	yes	N	M	4G	4G	Y		32		2007	2012	SPARC data sheets	reduced version of OpenSPARC T1	
m1_core	M1 Core	beta	Fabrizo Fazzino, Alb	MIPS?	32	32	kintex-7-3	James Brakefiel		3456	6			233	14.7	1.00	1.0	67	verilog	9	m1_core	yes	yes	N		4G	4G	Y		32		2007	2012		GCC target?	
diogenes	diogenes	beta	Fekknhifer	RISC	16	16	kintex-7-3	James Br	missing file "		6				14.7	0.67	1.0	#####	vhdl	11	cpu						1K					2008	2009			
mc6809e		beta	Flint Weller	6809	8x	8x	kintex-7-3	James Br	gate level pr		6				14.7	0.33	1.0	#####	vhdl	26	core_	yes	yes	N	N	64K	64K	Y				1999		6809 data sheets	course work, ASIC orientation	
t6507lp	T6507LP	beta	Gabriel Oshiro, San	6502	8	8x	spartan-6-3	James Br	errors						14.7		1.0		verilog	22	t6507	yes	yes	N	N	64K	64K	Y				2009	2010	6502 data sheets	for use in ATARI 2600	
ignite_ptsc		proprietar	George Shaw	forth	32	8											1.0		not avail					N		4G	4G					1995	2002		ShBoom clone, fast ASIC with high coding density	
myforthproc	FORTH processo	stable	Gerhard Hohner	forth	32		spartan-3	James Br	xilinx primitiv		4				14.7	1.00	1.0	#####	vhdl	51	mycpu	yes	yes	Y								2012	2012		DPANS'94 32-bit Forth, masters thesis, four variants	
cpugen	Cpu Generator	stable	Giovanni Ferrante																													2003	2009		x86 executable that generates VHDL uP	
mips32r1	MIPS32 Release	stable	Grant Ayers	MIPS	32	32	kintex-7-3	James Brakefiel		4822	6	8		90	14.7	1.00	1.0	19	verilog	20	proce	yes	yes	N		4G	4G	Y		32		2012	2014	MIPS data sheets	Harvard arch	
hc11core		stable	Green Mountain Co	68HC11	8x	8x	kintex-7-3	James Brakefiel		2014	6			125	14.7	0.33	1.0	21	vhdl	1	hc11r	yes	yes	N	N	64K	64K	N	53	8	2	2000		6811 data sheets	restricted use license, no divide inst	
tv80	TV80	mature	Guy Hutchison, Hov	Z80	8	8x	kintex-7-3	James Brakefiel		1207	6			182	14.7	0.67	1.0	101	verilog	6	tv80n	yes	yes	N	N	64K	64K	Y				2004	2012	z80 data sheets	derived from Daniel Wallner's T80, ASIC implementations	
hivek		alpha	Hadley Magno	VLIW	32												1.0		vhdl	18	hivek											2013			two inst per clock	incomplete source code
hicovec	HiCoVec a config	beta	Harald Manske, Gu	RISC	32	32	kintex-7-3	James Br	compiler erro		6				14.7	1.00	1.0	#####	vhdl	28	cpu	yes	asm	N				Y				2008	2010		hybrid scalar & vector processor	
eco32	SOC:ECO32	alpha	Hellwing Geisse	RISC	32	32	kintex-7-3	James Brakefiel		2210	6		1	160	14.7	1.00	1.0	72	verilog	23	cpu	yes	yes	N		512M	256M	Y	61	32		2003	2014		MIPS like, MMU	
mc8051		stable	Helmut Mayrhofer	8051	8	8x	kintex-7-3	James Brakefiel		3022	6	1		83	14.7	0.33	1.0	9	vhdl	49	mc805	yes	yes	N	N	256	64K	Y				1999	2013	www.oreganosystems	fast 8051, version available with floating-point by David Lundgren	
xproz		stable	Herbert Kleebauer	CISC	16	16x											1.0		schematic			yes	asm	N		64K	64K					1995			documentation in German	
df6805		proprietar	Hitech Global	6805	8	8x	stratix-1	Hitech Global		1690	4			83		0.33	1.0	16	not avail			yes	yes	N	N	64K	64K	Y						6805 data sheets		www.hitechglobal.com/IPCores/DF680
cpu86		beta	ht-lab.com	8086	8	8x	kintex-7-3	James Brakefiel		3421	6	1		127	14.7	0.17	1.0	6	vhdl	23	cpu86	yes	yes	N	N	1M	1M	Y				2002	2010	x86 data sheets	8088 clone	www.ht-lab.com
recore54		beta	ht-lab.com	PIC16	8	14	kintex-7-3	James Br	Cannot find		6				14.7	0.33	1.0	#####	vhdl	20	rcore5	yes	yes	N	Y	256	4K	Y				1999		PIC16 data sheets	PIC16 clone	www.ht-lab.com
6502vhdl	6502vhdl	planning	Huyvo	6502	8	8x													C				yes	N	N	64K	64K	Y				2003	2009	6502 data sheets	to have a C program generate VHDL	
6502_verilog	6502_verilog_de	sim?	Hyungok Tak	6502	8	8x													verilog				yes	N	N	64K	64K	Y				2010	2010	6502 data sheets	no files, simulated	
lattice6502	Lattice 6502	beta	Ian Chapman	6502	8	8x	kintex-7-3	James Brakefiel		4942	6			214	14.7	0.33	1.0	14	vhdl	3	ghdl_	yes	yes	N	N	64K	64K	Y				2010	2010	6502 data sheets	targeted to LCMXO2280	huge LUT count
pdp8l	Minimal PDP8/L	beta	Ian Schofield	PDP8	12	12	cyclone-3	James Brakefiel		1088	4			107	14.7	0.50	2.0	24	vhdl	11	top	yes	yes	N	N	4K	4K					2013		PDP8 data sheets		
v1_coldfire		stable	IPextreme	68000	8x	16x	cyclone-3	freescale		5000	4			80		0.89	1.0	14				yes	yes	N	N	4G	4G	Y		16		2008		68000 data sheets	free for Cyclone III	
J1		stable	James Bowman	forth	16	16	spartan-6	James Brakefiel		333	6		1	117	14.7	0.80	1.0	280	vhdl	1	j1	yes	forth	N		64K	64K		16		2	2006	2010	excamera.com/sphinx	uCode inst, dual port block RAM	32 deep data & return stacks
lem1_9	lem1_9	stable	James Brakefield	accum	1	9	kintex-7	James Brakefiel		40	6		1	357	14.5	0.04	1.0	357	vhdl	3	lem1_	yes	asm	N	Y	6	11	N	8	64	1	2003	2009		very small, 2 pipe stage is twice as fa	"logic emulation machine"

xr16		stable	Jan Gray	RISC	16	16	kintex-7-3	James Brakefiel	371	6			7	14.7	0.67	1.0	13	verilog	12	xsoc	yes		N		64K	64K			16		1999	2001		handcrafted FPGA layout & instruction set	
cpu6502_tru	cpu6502_tc	stable	Jens Gutschmidt	6502	8	8x	kintex-7-3	James Brakefiel	1678	6			159	14.7	0.33	1.0	31	vhdl	7	r6502_tc	yes	N	N	64K	64K	Y				2008	2010	6502 data sheets		
cpu65c02_tru	cpu65c02_tc	stable	Jens Gutschmidt	6502	8	8x	spartan-6-3	James Br	latch	4794	6			47	14.7	0.33	1.0	3	vhdl	8	core		yes	N	N	64K	64K	Y				2008	2013	6502 data sheets		
popcorn		stable	Jeung Joon Lee	accum	8	8x	spartan-6-3	James Brakefiel	268	6			171	14.7	0.33	1.0	211	verilog	4	pc	yes		N		64K	64K	Y	43			2000			small 8 bit uP	
myblaze	myBlaze	mature	Jian Luo	uBlaze	32	32										1.0		myhdl			yes	yes	N		4G	4G	Y		32		2010	2010	microBlaze data sheet	clone, no VHDL in tar file	
leon		stable	Jiri Gaisler, Jan And	SPARC	32	32			hard to find min configuration							1.0		vhdl	100s	leon3	yes	yes	Y		4G	4G			64		2003	2013	SPARC data sheets	customized for ~20 FPGA boards, configurable	
rise	RISE Microproce	beta	Jlechner etal	RISC	16	16	kintex-7-3	James Br	missing blox	6	1			14.7	0.67	1.0	#####	vhdl	26	rise	yes	asm	N		64K	64K			16	5	2006	2010	en.wikiversity.org/wik	ARM style register usage	
scarts	Scarts Processor	beta	Jlechner, Martin W	RISC	16	16	kintex-7-3	James Br	missing signa	6				14.7	0.67	1.0	#####	vhdl	18	scarts		yes	N		64K	64K		122	16	4	2011	2012		GCC compiler	
ourisc	16-bit Open uRI	alpha	Joao Carlos		16	16	stratix-4	Joao Carlos	500	A	1		550		0.67	1.0	737	vhdl										26			2013	2013		very incomplete source code	
pdp8	PDP-8 Processor	alpha	Joe Manojlovick, Ro	PDP8	12	12	kintex-7-3	James Brakefiel	1219	6	1		183	14.7	0.50	2.0	37	vhdl	55	cpu	yes	yes	N	N	32K	32K			8		2012	2013	PDP8 data sheets	Boots OS/8, runs apps, several variants	
jam		stable	Johan Thelin etal	RISC	64	32	kintex-7-3	James Brakefiel	1369	6			143	14.7	1.00	1.0	104	vhdl	17	cpu	yes		N		128K	128K			32	5	2002				
risc16f84	risc16f84	stable	John Clayton	PIC16	8	14	kintex-7-3	James Brakefiel	331	6			333	14.7	1.00	1.0	1007	verilog	1	risc16	yes	yes	N	Y	256	4K	Y				2002	2013	PIC16 data sheets	derived from CQPIC by Sumio Morioka	
micro16b		beta	John Kent	accum	16	16	kintex-7	Xilinx	205	6			434	14.7	0.33	2.0	349	vhdl	1	u16bc	yes	asm	N	N	64K	4K	Y	8			2002	2008	members.optushome.	very limited inst set	MIPS/clk adj'd, 2 clks/inst
micro8a		beta	John Kent	accum	8	16	kintex-7	Xilinx	531	6			204	14.7	0.33	3.0	42	vhdl	11	Micro	yes		N	N	2K	2K	Y				2002	2002	members.optushome.	derived from Tim Boscke's mcpu, not perfected	
system05	SOC:system05	beta	John Kent	6805	8	8x	kintex-7-3	James Brakefiel	834	6			204	14.7	0.33	1.0	81	vhdl	10	Syster	yes	yes	N	N	64K	64K	Y				2003	2009	6805 data sheets		
system09	SOC:system09	stable	John Kent	6809	8x	8x	kintex-7-3	James Brakefiel	1945	6			154	14.7	0.33	1.0	26	vhdl	40	cpu09	yes	yes	N	N	64K	64K	Y				2003	2012	6809 data sheets	from John Kent web page	
system11		alpha	John Kent, David Bu	6811	8	8x	kintex-7-3	James Brakefiel	1218	6			153	14.7	0.33	1.0	41	vhdl	17	cpu11	yes	yes	N	N	64K	64K	Y				2003	2009	6811 data sheets	known bugs & untested instructions	
system68	System68	stable	John Kent, David Bu	6801	8	8x	spartan-3-5	James Brakefiel	2235	4		4	46	14.7	0.33	1.0	7	vhdl	21	cpu68	yes	yes	N	N	64K	64K	Y				2003	2009	6801 data sheets		
jpu16		stable	Joksan Alvarado	RISC	16	26	kintex-7-3	James Br	missing defir	6				14.7	0.67	1.0	#####	vhdl	9	JPU16	yes	asm	N		64K	64K			16		2012			32 deep call stack, 8 addressing modes	
leros32	Leros-32	alpha	Jon Pry	forth	32													no files					N		4G	4G					2013			see Leros entry	
tinycpu	TinyCPU	alpha	Jordan Earls	RISC	8	16												vhdl	10	top		asm	N		64K	64K			16		2012	2012			
sub86	Small x86 subset	alpha	Jose Rissetto	8086	8x	8x												verilog	1	sub86	yes	yes	N	N	64K	64K	Y		7		2012	2013		no segment registers, limited op-codes	
ion	Ion MIPS compa	mature	Jose Ruiz	MIPS	32	32	kintex-7-3	James Brakefiel	1533	6			163	14.7	1.00	1.0	106	vhdl	12	mips_	yes	yes	N		4G	4G	Y		32		2011	2014		MIPS R3000 clone	
ion	Ion MIPS compa	mature	Jose Ruiz	MIPS	32	32	virtex-5	Jose Ruiz	2017	6			104		1.00	1.0	52	vhdl	12	mips_	yes	yes	N		4G	4G	Y		32		2011	2014		MIPS R3000 clone	
light52	Lightweight 805	beta	Jose Ruiz	8051	8	8x	kintex-7-3	James Brakefiel	1027	6	1	1	148	14.7	0.17	1.0	24	vhdl	8	light5	yes	yes	N	N	64K	64K	Y				2012	2013	8051 data sheets	targeted to area	
light8080	Lightweight 808	stable	Jose Ruiz, Moti Lito	8080	8	8x	kintex-7-3	James Brakefiel	154	6		1	247	14.7	0.17	1.0	265	verilog	5	i80soc	yes	yes	N	N	64K	64K	Y				2007	2012	8080 data sheets	targeted to area, includes UART, interrupt ctlr & RAM	
oops	OoOPs Out-of-O	planning	Joshua Smith	MIPS	32	32												verilog	13		yes	yes	N		4G	4G	Y		32		2012	2012		incomplete source code	
c16	16 Bit Microcont	stable	Jsauermann	C	16	8x	spartan-3-5	James Brakefiel	1850	4		16	57	14.7	0.33	1.0	10	vhdl	22	Board	min	C,asm	N		64K	64K	Y		5		2003	2012		8080 derivative, optional UART, 8-bit memory port	
jmr16f84	JMP16F84 PIC M	stable	Julio Rodriguez	PIC16	8	14										1.0		no files						Y							2013		PIC16 data sheets		
picoblaze	picoblaze	stable	Ken Chapman	picoBlaze	8	18	spartan-3-4	James Brakefiel	178	4			182	14.7	0.33	1.0	338	vhdl	1	kcspm	yes	asm	N		256	2K	Y				2003		picoblaze data sheets	2 clocks per inst	this is the original picoBlaze author
or1k-cf	Confluence Ope	alpha	Kenr	OpenRISC	32	32												confluence													2004	2009			
gup	HC11 Compatibl	stable	Kevin Phillipson	68C11	8x	8x	kintex-7-3	James Br	missing uP fil	6				14.7	0.67	1.0	#####	vhdl	25	?	yes	yes	N	N	64K	64K	N				2008	2009	6811 data sheets	68HC11 compatible	
open8_urisc	Open8 uRISC	stable	Kirk Hays, Jshamlet	RISC	8	8	kintex-7-3	James Brakefiel	691	6	1		263	14.7	0.33	1.0	126	VHDL	9	Open8	yes	yes	N		64K	64K	Y		8		2006	2013		accum & 8 regs, clone of Vautomation uRISC processor, in use	
microcore		beta	Klaus Schleisiek	forth	32	8	spartan-6-3	James Brakefiel	591	6		1	71	14.7	1.00	1.0	120	vhdl	10	core	yes	asm	N		2M	512K					2004			good documentation	
oks8	oks8	alpha	Kongzilee	ARM7	32	32										1.0		verilog	8	oks8	yes	yes	N		64K	64K	Y				2006	2009		clone of KS86C4204/C4208/P4208, SAM87RI instruction set	
latticemicro8		stable	Lattice Semiconduc	RISC	8	18	LFE2	Lattice Semicor	265	4			104			1.0		vhdl	10	isp8_c	yes	yes	N		256	4K	Y		32		2005	2010	en.wikipedia.org/wiki/	16 deep call stack, four configurations	
mips_fault_t	Mips-FaultTolera	stable	Lazaridis	MIPS	32	32										1.0		vhdl			yes	yes	N		4G	4G	Y		32		2013		MIPS data sheets	arithmetic includes fault detection	
mipsr2000	mipsr2000	stable	Lazaridis Dimitris	MIPS	32	32	kintex-7-3	James Brakefiel	1971	6	4	6	71	14.7	1.00	1.0	36	vhdl	35	Dm	yes	yes	N		4G	4G	Y		32	5	2012	2013	MIPS data sheets	course project	
mips_enhanc	MIPS_enhanced	stable	Lazaridis Dimitris, I	SPARC	32	32			difficult to find min design							1.0		vhdl		leon3	yes	yes	N		4G	4G	Y		32		2010	2011	tar file does not match	based on mips789, added cache?? Only source is for Leon3	
distributed_i	Distributed limit	planning	Leo Ger		16	16												vhdl	11	mini_uP_x16			N		64K	64K					2009	2009		single stack and 4 data registers	
opencpu32	OpenCPU32	planning	Leonardo Araujo dos Dantos		32	32												vhdl	22	pkgOpenCPU32			N						16		2012	2012		built to test division algorithms	
dragonfly		beta	LEOX team	MISC	16	16	kintex-7-3	James Brakefiel	788	6			164	14.7	0.67	1.0	139	vhdl	6	dgf_c	yes		N		256	2K					2001		www.leox.org	unusual, uses FIFOs	
mips789	mips789	stable	Li Wei	MIPS	32	32	kintex-7-3	James Brakefiel	1432	6		1	171	14.7	1.00	1.0	119	verilog	10	mips_	yes	yes	N		4G	4G	Y		32		2007	2009	MIPS data sheets		
lwrisc	ClaiRISC	stable	Li Wu	PIC16	8	14	arria-2	James Br	undefined co	A				13.1	0.33	1.0	#####	verilog	9	risc_core				Y							2008	2009	PIC16 data sheets		
neptune-core	The Neptune Co	planning	Llama															no source													2003	2009		single schematic	
secretblaze		beta	Lyonel Barthe	uBlaze	32	32	spartan-3-4	Lyonel Barthe	1563	4			91	12.1	1.00	1.0	58	vhdl	26	sb_core	yes				4G	4G	Y	86	32	5	2010	2012	www.lirmm.fr/ADAC/		
risc_core_i	RISC_Core_I	planning	Manuel Imhof	RISC	16	16	kintex-7-3	James Brakefiel	349	6	1		717	14.7	0.67	1.0	1377	vhdl	13	CPU	yes	asm	N		1K	1K			8	4	2001	2009		Havard arch	dubious Fmax
or2k	OpenRISC 2000	planning	Marcus Erlandsson etal		32	32												no source																	
leros	Leros	stable	Martin Schoeberl	accum	16	16	kintex-7-3	James Br	adjust	115	6		1	277	14.7	0.67	1.0	1614	vhdl	6	leros	yes	yes	N		64K	64K			2	2	2008	2012	Leros: A Tiny Microcor	short LUT inst ROM	256 word data RAM, PIC like
jop	JOP a Java Optin	stable	Martin Schoeberl e	forth	16	16	cyclone-1	Martin Schoebe	2000	4			100	10	0.67	1.0	34	vhdl	11	core	yes	yes	N		256K	256K					2004	2014		opencores download is empty	https://github.com/jop-devel/jop
m65c02	M65C02	mature	Michael Morris	6502	8	8x	spartan-3	Michael Morris	661	4	0	3	74		0.33	1.0	37	verilog	13	M65C	yes	yes	N	N	64K	64K	Y				2013	2014	6502 data sheets		
p16c5x	P16C5x	mature	Michael Morris	PIC16	8	14	spartan-3	Michael Morris	488	4		3	60		0.33	1.0	41	verilog	3	P16C5	yes	yes	N	Y	256	4K	Y				2013	2014	PIC16 data sheets		
risc5x	RISC5x	stable	MikeJ	PIC16	8	14	kintex-7-3	James Br	errors in usir	6				14.7	0.33	1.0	#####	vhdl	15	cpu	yes	yes	N	Y	256	4K	Y				2002	2011	PIC16 data sheets	makes extensive use of xilinx primitives	
myrisc1	myRISC1	stable	Muza Byte	RISC	8	8												no files					N		256	256	Y		4		2011	2011			
pepelatz_mis	Pepelatz MISC	planning	Myname IsTeapot	MISC														verilog	1															insignificant source	
m65		stable	Naohiko Shimizu	6502	8	8x										1.0			8	m65c	yes	yes	N	N	4K	4K	Y				2001	2002	6502 data sheets	source files have unusual suffixes	
sparcv8copro	Coprocessor-rea	planning	Nicholas Voorsange	SPARC	32	32												no files													2012		SPARC data sheets		
avr8	Reduced AVR Co	beta	Nick Kovach	AVR	8	16	kintex-7-3	James Brakefiel	174	6			418	14.7	0.33	1.0	792	verilog	1	rAVR	yes	yes	N		64K	64K	Y	17	4		2010	2010	AVR data sheets	not a full clone, doc is opencores page	
next186	Next 80186 proc	stable	Nicolae Dumitrache	8086	8x	8x	arria-2	James Brakefiel	1966	6	1		83	14.7	0.33	1.0	14	verilog	4	Next1	yes	yes	N	N	1M	1M	Y				2012	2013	x86 data sheets	boots DOS	
nextz80	NextZ80	stable	Nicolae Dumitrache	Z80	8	8x	kintex-7-3	James Brakefiel	1064	6			106	14.7	0.67	1.0	66	verilog	3	NextZ	yes	yes	N	N	64K	64K	Y				2011	2014	z80 data sheets		
risc0		beta	Niklaus Wirth	RISC	32	32	kintex-7-3	James Brakefiel	1186	6	4	6	110	14.7	0.67	1.0	62	verilog	8	RISC0	yes	yes	N		4G	4G					2011			minimalist Wirth, education tool	
risc5		beta	Niklaus Wirth	RISC	32	32	kintex-7-3	James Br	missing prom	6	4	6		14.7	1.00	1.0	#####	verilog	17	RISC5	yes	yes	Y		4G	4G					2013			minimalist Wirth, part of Project Oberon 2013	
ag_6502	ag_6502 soft co	beta	Oleg Odintsov	6502	8	8x	spartan-6-3	James Brakefiel	807	6	0	0	80	14.7	0.33	1.0	33	verilog	2	ag_6502	yes	yes	N	N	64K	64K	Y				2012	2012	6502 data sheets	verilog code generation, "phase level accurate", 978 LUTs	
openmsp430	openMSP430	stable	Oliver Girard	msp430	16	16x	stratix-3-2	Oliver Girard	1147	A	1		98		0.67	1.0	57	verilog	30	openM	yes	yes	N	N	64K	64K	Y		16		2009	2014	msp430 data sheets	implemented on four FPGAs, performance spreadsheet	
zpu	ZPU the worlds	stable	Oyvind Harboe	forth	32	8	spartan-6	Oyvind Harboe	1259	6			135		0.10	1.0	11	vhdl	23	zpu_c	yes	yes	N		4G	4G	Y	37			2008	2009	www.zylin.com	zpu4: 16 & 32 bit versions, code size 80% of ARM (thumb), low MIPs/MHz	
zpu	ZPU the worlds	stable	Oyvind Harboe	forth	32	8	spartan-3	Oyvind Harboe	440	4			85		0.05	1.0	10	vhdl	23	zpu_c	yes	yes	N		4G	4G	Y	37			2008	2009	www.zylin.com	zpu4: 16 & 32 bit versions, code size 80% of ARM (thumb), low MIPs/MHz	
pacoBlaze		mature	Pablo Kocik	picoBlaze	8	18	spartan-3	Pablo Kocik	177	4		1	117		0.33	1.0	218	verilog	18	pacob	yes	asm			8	11	Y	57		2		2006	bleyer.org/pacoblaze	3 versions, behavioral coding	
usimplez	MicroSimplez	stable	Pablo Salvadeo etal	accum	12	12	stratix-2	Pablo Salvadeo	48	4			134	9.1	0.17	1.0	476	vhdl	3	usimplez_cpu			N		512	512		8			2011			von Neuman arch, Simplez processo	MIPS/Mhz reduced due to few inst
gumnut		stable	Peter Ashenden	RISC	8	18	kintex-7-3	James Br	missing file	6				14.7	0.33	1.0	#####	vhdl	20	gumn	yes		N		256	4K	Y		8		2007			see Digital Design: An Embedded Systems Approach Using VHDL	
msl16		beta	Philip Leong, Tsang,	forth	16	4	kintex-7-3	James Brakefiel	303	6			256	14.7	0.67	1.0	566	vhdl	13	cpu	yes	asm	N		256						2001			CPLD prototype	
minimips	miniMIPS	stable	Poppy etal	MIPS	32	32	kintex-7-3	James Brakefiel	2939	6	8		118	14.7	1.00	1.0	40	vhdl	12	minim	yes	yes	N		4G	4G	Y		32	5			MIPS I		
minsoc	minsoc	stable	Raul Fajardo etal	OpenRISC	32	32	kintex-7-3	James Brakefiel	4945	6	4	8	107	14.7	1.00	1.0	22	verilog	88	or120	yes	yes	Y	M	4G	4G	Y		32		2009	2013	www.minsoc.com	minimal OR1200, vendor neutral, has caches	
mcs-4	4004 CPU & MC	alpha	Reece Pollack	4004	4	4												verilog	7	i4004			N		4K	4K	N				2012	2012	4004 data sheets	4004 was multi-chip	
oc54x	OpenCores54x D	beta	Richard Herveille	C54x	16	16												verilog	10	oc54_	yes	yes	N	Y	64K	64K					2002	2009	C54x data sheets	incomplete source code	
8bit_chapman		beta	Rob Chapman, Stev	forth	8	8	kintex-7-3	James Br	syntax errors	6				14.7	0.33	1.0	#####	vhdl	10	top	yes		N		256	256					1998			course work	
dataflow_chapman		alpha	Rob Chapman, Stev	forth			kintex-7-3	James Br	file WebCase	6				14.7	0.33	1.0	#####	vhdl	27	DataF	yes		N		256	256					2003			course work	
klc32	KLC32	planning	Robert Finch	RISC	32	32												verilog	25	KLC32	yes		N		4G	4G	Y		32		2011	2012			
raptor64	Raptor64	planning	Robert Finch	RISC	64	32	kintex-7-3	James Br	missing port	6				14.7	1.50	1.0	#####	verilog	48	Rapto	yes	yes	Y		2<<64	2<<64	Y		32		2012	2013		8-16-32-64 bit data, cache, MMU, hyper-threaded version also	
rtf65002	RTF65002	planning	Robert Finch	accum	32	8x												verilog	47	rtf650	yes		N		4G	4G	Y		16		2013	2013		32-bit 6502 + 6502 emulation	
rtf8088	rtf8088	planning	Robert Finch	8086	8x	8x	kintex-7-3	James Brakefiel	4514	6	4		174	14.7	0.67	1.0	26	verilog	57	rtf808	yes	yes	N	N	1M	1M	Y				2012	2013	x86 data sheets		
ssbcc	Smal Stack Base	stable	Rodney Sinclair	forth	8	9			syntax errors							1.0		verilog	3	core	yes	asm	N				Y				2012	2014		Python program generates the Verilog	
dfp	dfp	stable	Ron Chapman	forth	X	Y	spartan-6-3	James Brakefiel	334	6			112	14.7	0.33	1.0	111	vhdl	25	top	yes										2003	2009		8-bitter, generates a custom VHDL stack machine, compiler is in Forth	
minirisc	Mini-Risc core	stable	Rudolf Usselmann	PIC16	8	14	spartan-3	Rudolf Usselma	460	4			80		0.33	1.0	57	verilog	7	risc_c	yes	yes	N	Y	256	4K	Y				2001	2012	PIC16 data sheets		
avr_core	avr_core	stable	Rusian Lepetenok	AVR	8	16	kintex-7-3	James Br	errors	2135	6			127	14.7	0.33	1.0	20	verilog		avr_core		yes	N		64K	128K	Y		32		2002	2012	AVR data sheets	VHDL core included	
ecpu	ecpu	planning	Sahrfili Matturi															verilog													2009	2009			
sxp	SXP (Simple eXte	beta	Sam Gladstone etal	RISC	32	32			too many Ios									verilog		sxp			N		4G	4G			32		2001	2009		basic RISC	too many Ios
manik		stable	Sandeeo Dytta	RISC	32	32	arria-2	James Br	vcomponent	A				13.1	0.33	1.0	#####	vhdl	45	manik	yes	yes	N		4K	4K	Y		16		2002	2006	www.niktech.com/	optional data & inst caches	
cpu8080	8080 Compativle	stable	Scott Moore	8080	8	8x	spartan-6-3	James Brakefiel	1269	6			129	14.7	0.33	1.0	34	verilog	1	m808	yes	yes	N	N	64K	64K	Y				2006	2009	8080 data sheets	includes VGA display generator, three variants	
navre	Navre AVR clone	stable	Sebastien Bourdeau	AVR	8	16	kintex-7-3	James Brakefiel	990	6			207	14.7	0.33	1.0	69	verilog	1	softus	yes	yes	N		64K	64K	Y		32	2	2010	2013	AVR data sheets	AVR clone, part of www.milkymist.org	
y80e	Y80e Z80/Z180 c	stable	Sergey Belyashov	Z80	8	8x	kintex-7-3	James Br	empty projec	6				14.7	1.00	1.0	#####	verilog	15	y80_t	yes	yes	N	N	64K	64K	Y				2013	2013	z80 data sheets	based on Y80 from "Microprocessor Design Using Verilog HDL" by Monte D	

erp	Educational RISC	stable	Shahzadjk	RISC	8	16	kintex-7-3	James Br	syntax errors	6				14.7	0.33	1.0	#####	verilog	1	ERPve	yes							15	6		2004	2009		two report PDFs & one Verilog file	
ae18	ae18	beta	Shawn Tan	PIC18	16	24	arria-2	James Brakefiel	1084	A	1		207	13.1	0.67	1.0	128	verilog	1	ae18_core	yes	N	Y	4K	1M					2003	2009	PIC18 data sheets	not 100% compatable	negative edge reset "clock"
aeMB	aeMB	beta	Shawn Tan	uBlaze	32	32	kintex-7-3	James Brakefiel	1018	6	3		131	14.7	1.30	1.0	167	verilog	29	aeMB	yes	N		4G	4G	Y				2004	2009	xilinx documentation	not 100% compatable	
k68	K68	alpha	Shawn Tan	68000	8x	16x												verilog	15	k68_c	yes	yes	N	4K	4G	Y		16		2003	2009	68000 data sheets	68K binary compatible	
x32		stable	Sijmen Woutersen	forth	32	8	kintex-7-3	James Br	missing defin	6				14.7	1.00	1.0	#####	vhdl	32	core	yes	yes	N		4G	4G	Y				2006	2007		MS thesis, byte code, needs caches	
8051	8051	alpha	Simon Teran, Jakas	8051	8	8												verilog	32	oc805	yes	yes	N		64K	64K	Y				2001	2009	8051 data sheets	not fully tested	
aspida	ASPIDA DLX core	stable	Sotiriou	DLX	32	32	kintex-7-3	James Brakefiel	3586	6			257	14.7	1.00	1.0	72	verilog	10	DLX_t	yes	yes		4G	4G					2002	2009	Knuth DLX		compiled sync version
bobcat		beta	Stan Drey		16	24	kintex-7-3	James Brakefiel	1622	6	1		107	14.7	0.67	1.0	44	vhdl						64K	64K					1998			appears to be a DSP	
wb4pb	Software Aided	stable	Stefan Fischer	picoBlaze	13	13												vhdl & ve	10				Y							2010	2013	picoblaze data sheets	software addon for picoBlaze	
ncore	nCore	alpha	Stefan Istvan	RISC	8	8												verilog	3	nCore	yes	N						16	16		2006	2009			
atlas_core	Atlas Processor	beta	Stephan Nolting	RISC	16	16	kintex-7-3	James Brakefiel	655	6	1	1	192	14.7	0.80	1.0	235	vhdl	13	ATLAS	yes	asm	N	4G	4G	N	80	8		2013	2013		ARM thumb like inst set, also X2 vers	both MMU and non-MMU versions
atlas_x2	Atlas Processor	beta	Stephan Nolting	RISC	16	16	kintex-7-3	James Br	missing defin	6	1	1		14.7	0.80	1.0	#####	vhdl	13	ATLAS	yes	asm	N	4G	4G	N	80	8		2013	2013		ARM thumb like inst set	has MMU & full SOC features
storm_core	Storm Core (ARM	beta	Stephan Nolting	ARM7	32	32	kintex-7-3	James Brakefiel	2312	6	3		179	14.7	1.00	1.0	77	vhdl	16	CORE	yes	yes	N	N	4G	4G	Y		32	8	2011	2013		I & D caches not compiled	
plasma	Plasma most MI	stable	Steve Rhoads	MIPS	32	32	kintex-7-3	James Brakefiel	2462	6		3	97	14.7	1.00	1.0	40	vhdl	22	plasm	yes	yes	N		4G	4G	Y		32		2001	2013	MIPS data sheets	wide outside use, opencores page has list of related publications	
avr_hp	avr_hp	stable	Strauch Tobias	AVR	8	16	kintex-7-3	James Br	2 slot	1554	6		223	14.7	0.33	1.0	47	vhdl	10	avr_c	som	yes	N		64K	128K	Y		32		2010	2010	AVR data sheets	hyper pipelined (eg barrel) AVR	
cortex_m3	cortex_m3	?	Strauch Tobias	ARM c3	32	16												no files													2013		cortex M3 data sheets	claims to be mature	
or1200_hp	OpenRisc 1200 H	stable	Strauch Tobias	OpenRISC	32	32	kintex-7-3	James Br	1 slot barrel		6			14.7	1.00	1.0	#####	verilog	39	or120	yes	yes	Y		4G	4G	Y		32		2010	2013		original version of OR1200	
jane_nn		stable	Suresh Devanathan	RISC	4	8	kintex-7-3	James Brakefiel	723	6			178	14.7	0.33	1.0	81	vhdl	3	Proce	yes							27	16		2002			neural network microprocessor, specialized registers	
ARC		proprieta	Synopsys		32	16										1.0		not avail							4G	4G								range of reduced SPARC? uP	
eight_bit_uc		stable	Synplicity	RISC	8	12	kintex-7-3	James Br	signal/variab	6				14.7	0.67	1.0	#####	vhdl	10	eight_bit_uc					2K	Y		32						part of Amplify documentation	
yacc	YACC Yet Anothe	stable	Tak Sugawara	MIPS	32	32	kintex-7-3	James Br	xilinx IP prob	6				14.7	1.00	1.0	#####	verilog	10	yacc2	yes	yes	N		4G	4G	Y		32	5	2005	2009	MIPS data sheets	derived from, but independent of plasma, xilinx & altera implemntations	
mblite	MB-Lite	beta	Tamar Kranenburg	uBlaze	32	32	virtex-5			6			229			1.0		vhdl	10	core	yes	yes	N		4G	4G	Y	86	32		2009	2012	microBlaze data sheet	not all instructions implemented	
cowgirl	Cowgirl	beta	Thebeekeeper		16	16	kintex-7-3	James Br	empty design	6				14.7	0.67	1.0	#####	vhdl	14	cowgirl					64K						2006	2009			
free_risc8		stable	Thomas Coonan	PIC16	8	14	kintex-7-3	James Brakefiel	355	6			142	14.7	0.33	1.0	132	verilog	8	cpu	yes	yes	N		256	4K	Y				2002	2011	PIC16 data sheets		
aquarius	aquarius	stable	Thorn Aitch	SuperH-2	32	16	kintex-7-3	James Brakefiel	3958	6	2		86	14.7	1.00	1.0	22	verilog	21	top	yes	yes	N		4G	4G	Y				2003	2009	SuperH data sheets		
mcpu	MCPU A minima	stable	Tim Boscke	accum	8	8	spartan-6-3	James Brakefiel	41	6			384	14.7	0.17	1.0	1592	vhdl	1	tb02c	yes	asm	N		64	64	Y	4			2007	2014		fits into 32 macrocell CPLD	reduced MIPS/clk due to only 4 inst
tg68	TG68 execute 68	stable	Tobias Gubener	68000	8x	16x	kintex-7-3	James Brakefiel	2331	6			44	14.7	0.67	1.0	13	vhdl	2	TG68_	yes	yes	N	N	4G	4G	Y		16		2007	2012	68000 data sheets	for use with Minimig	
pic_coonan		alpha	Tom Coonan	PIC16	8	14												vhdl			yes	yes	N	Y	256	4K	Y				1999		PIC16 data sheets		
cf_ssp	CF State Space P	stable	Tom Hawkins	?														vhdl													2003	2009		confluence to VHDL	
fpgammix		stable	Tommy Thorn	RISC	64	32			system verilog							1.0		system ve	12	core	yes							256	256		2006	2008		clone of Knuth's MMIX	
dalton_8051		stable	Tony Givargis	8051	8	8x	kintex-7-3	James Brakefiel	2725	6	1	1	105	14.7	0.33	1.0	13	vhdl	7	i8051	yes	yes	N	N	64K	64K	Y				1999	2003	8051 data sheets	ASIC	www.cs.ucr.edu/~dalton/
hd63701	HD63701 compa	planning	Tsuyoshi Hasegawa	6801	8	8x	spartan-6-3	James Brakefiel	1412	6	1	3	31	14.7	0.33	1.0	7	verilog	6	HD63701_CORE		N	N	64K	64K	Y				2014			Used in Atari game console, 6801 clone?	
ic6821	vhdl core of IC68	beta	Ttsenis		8											1.0		vhdl	1	VHDL	yes										2005	2009	6800 data sheets	VHDL for M6821	
68hc05	68hc05	stable	Ulrich Riedel	6805	8	8x	kintex-7-3	James Brakefiel	1225	6			300	14.7	0.33	1.0	81	vhdl	1	6805		yes	N	N	64K	64K	Y				2007	2009	6805 data sheets		
68hc08	68hc08	stable	Ulrich Riedel	6808	8	8x	kintex-7-3	James Brakefiel	2290	6			101	14.7	0.33	1.0	15	vhdl	1	x68ur08		yes	N	N	64K	64K	Y				2007	2009	6808 data sheets		
tiny64	Tiny64	stable	Ulrich Riedel	RISC	64		kintex-7-3	James Br	bit length mi	6				14.7	1.00	1.0	#####	vhdl	7	TinyX		asm	N		64K	64K		16	8		2004	2009		word size configurable from 32 to 64	
tiny8	tiny8	mature	Ulrich Riedel	CISC	8x	8x										1.0		AHDL				asm	N		64K	64K	Y				2002	2009		registers in RAM like TMS9900, uses Altera AHDL, megafunctions & schema	
altor32	AltOr32	stable	Ultra Embedded	OpenRISC	32	32										1.0		verilog	19	altor32		yes	N		4G	4G	Y				2012	2014	OpenRISC 1000	simplified OpenRISC 1000	
mpx	MPX 32-bit CPU	stable	Ultra Embedded		32	32												verilog					N		4G	4G	Y		32		2012	2013		GCC tools, no Verilog	
hpc-16	HPC-16	beta	Umair Siddiqui	RISC	16	16	kintex-7-3	James Brakefiel	875	6			136	14.7	0.67	1.0	104	vhdl	20	cpu	yes	asm	N		64K	64K			16		2005	2009			
qrisc32	qrisc32 wishbon	alpha	Viacheslav	RISC	32	32			system verilog source									system ve	8	qrisc3	yes	yes	Y		4G	4G	Y		32	4	2010	2011		for PhD thesis	
tisc	Tiny Instruction	beta	Vincent Crabtree	accum	8	8x	spartan-6-3	James Brakefiel	198	6			60	14.7	0.33	1.0	100	vhdl	1	TISC			N		256	1K	Y		2		2009	2009		minimal accumulator machine	
w11	PDP-11/70 CPU	alpha	Walter Mueller	PDP11	8x	16x	spartan-6	Walter Mueller	3418	6			80		0.67	1.0	16	vhdl	26	pdp11	yes	yes	N	N	4M	4M	Y		8		2010	2013	PDP11 data sheets	Boots UNIX, has MMU & cache, retro project	
ucore	Ucore	stable	Whitewill	MIPS	32	32	kintex-7-3	James Brakefiel	2469	6		1	231	14.7	1.00	1.0	93	verilog	25	ucore	yes	yes	N		4G	4G	Y		32	6	2005	2010	MIPS data sheets	MMU & caches	
lemberg		stable	Wolfgang Puffitsch	VLIW	32	32	cyclone-4-6	James Br	fitter failed		4			13.1	1.00	1.0	#####	vhdl	32	core	yes	yes	Y		4G	2M	Y		32	4	2011		www2.imm.dtu.dk/~w	upto 4 inst/clock	
marca	McAdam's RISC	stable	Wolfgang Puffitsch	RISC	16	16	kintex-7-3	James Br	syntax errors	6				14.7	0.67	1.0	#####	vhdl	40	marca	yes		N		8K	16K		75	16	4	2007	2009			
microblaze		proprieta	Xilinx	uBlaze	32	32	kintex-7	Xilinx	546	6		1	264		1.03	1.0	498	not avail			yes	yes	opt		32	32	Y	86	32	3	2002		www.xilinx.com/tools/	area optimized	70 configuration options, MMU optior
yasep		alpha	Yann Guidon	RISC	16	32	kintex-7-3	James Br	syntax errors	6				14.7	1.00	1.0	#####	vhdl		micro	yes	asm	N			2K			16		2008	2014	www.yaesp.org	Java generated VHDL, revisions ongo	funky web site
latticemicro32		stable	Yann Siommeau, M	RISC	32	32	kintex-7-3	James Brakefiel	2292	6	3	8	155	14.7	0.80	1.0	54	verilog	24	lm32_	yes	yes	N		4G	4G	Y		32		2006	2012	en.wikipedia.org/wiki/	optional data & inst caches	
riscmcu	RISC Microcontr	stable	Yapzihe	AVR	8	16	arria-2	James Br	LPM parame		6			14.7	0.33	1.0	#####	vhdl	15	v_risc	yes	yes	N		128	512	Y	92	16		2002	2009	AVR data sheets		
zet86	Zet The x86 (IA-3	alpha	Zeus Marmolejo	8086	8x	8x	kintex-7-3	James Brakefiel	3642	6	1		68	14.7	0.67	1.0	12	verilog	32	fpga_	yes	yes	N	N	1M	1M	Y				2008	2014	x86 data sheets	equivalent to 80186, boots MS-DOS	zet.aluzina.org/index.php/Zet_process
mproz		stable		RISC	16	16												schematic			yes	asm	N			32K					1999			little documentation, CPLD implementation	
totalcpu	TotalCPU	alpha		RISC	12+	12												verilog											16		2007	2009		data width 12 bits and up, no data memory	

41 # usable(beta, stable or mature): "A"(clones) & "W"(originals) 69 # adr locations

30 "B" or "X" of limited interest

Web page DMIPS per clock cycle per co en.wikipedia.org/wiki/Instructions_pe community.freescale.c www.eembc.org/coremark/index.php

MIPS/MHz Pro-rating for data size:

1-bit	0.04
8-bit	0.33
16-bit	0.67
32-bit	1.00

Under the assumption that the core is capable of one instuction per clock

Following has DMIPS per clock for many microprocessors
http://en.wikipedia.org/wiki/Instructions_per_second

Silicon Area equivalents

LUTS/DSP48	16:1
LUTS/Block RAM	32:1

uP	MIPS			CoreMarks /MHz	MHz	
4004	0.10					
6502	0.50		0.02	0.06		
8051			0.08	0.24		
8080	0.17			0.25		
68K	0.10			0.15		
ARM Cortex A9	2.50	DMIPS		5.93	1000	
ARM Cortex M0	0.90	DMIPS		1.50	70	
ARM Cortex M3	1.25	DMIPS		2.92	25	
ARM7	0.90		0.74	2.04	600	
AVR	1.00		0.21	0.53	8	
AVR32				1.62	60	
BA21				2.44	400	
Coldfire				2.80	400	
Coldfire				0.77	150	Virtex-5
HCS08			0.04	0.12		
LEON3/Spartan-6				1.96	100	
MC6809	1.24		0.07	1.86		
MicroBlaze 3-stage	1.03			1.50		
MicroBlaze 5-stage	1.38			1.90	125	
MIPS32	1.51			2.28		
MSP430			0.40	1.20		
MSP430				1.10	25	
Nios II	0.64	DMIPS		0.93	200	
Nios II -e	0.15	DMIPS		0.25		
Nios II -f	1.13	DMIPS		1.60	200	
PIC16	0.25					
PIC18				0.04	40	
PIC24			0.72	1.86	40	
PIC32				3.45	80	
Super H-2				1.44	180	

Column Titles	Details
"A"	A: 1st choice clone, B: 2nd choice clone, W: 1st choice original, X: 2nd choice original
"B"	currently unused and hidden
_uP_cores_test folder	if opencores design is their folder name, otherwise my folder name
opencores name	
status	ASIC, planning, alpha, beta, stable, mature, proprietary
author	First Name, Last Name
style / clone	part number or "forth", RISC, accumulator, etc
data size	data memory word size
inst size	instruction size
FPGA	FPGA family for compile, place, route & timing
reporter	First Name, Last Name
comments	compile, place, route & timing problems
LUTs ALM	4-LUT, 6-LUT, Altera ALM, Actel Tile
LUT?	total number of LUTs or ALMs used including route-thrus & otherwise unavailable
mults	total number of multipliers/DSPs used
blk RAM	total number of block RAMs used, does not include small and extra large Altera block RAMs, Xilinx half block RAM rounded up
Fmax	maximum primary clock speed from compile, place, route & timing run
tool ver	Altera, Xilinx, Lattice Semiconductor or MicroSemi tool version number
MIPS /clk	prorated DMIPS per clock, reduced for data word sizes under 32-bits, greater than one for multiple issue processors
clks/ inst	number of clocks per instruction, typically 1.0 for modern pipelined processors
KIPS /LUT	figure of merit, does not include effects of memory capacity, floating point or instruction set quality
src code	VHDL or Verilog or other
# src files	number of source files for compile, place, route & timing
top file	top file for compile, place, route & timing run

doc	is documentation provided
tool chain	is there a compiler or assembler provided or available
fltg pt	does the compile, place, route & timing run include floating point
Ha vd	separate instruction and data memory(s), there can be more than one data memory, M for MMU & caches
max data	maximum data address
max inst	maximum instruction address
byte adrs	is byte addressing provided
# inst	number of unique instructions, somewhat subjective
# reg	number of registers in register file
pipe len	number of pipeline stages
start year	year of first design activity
last revis	last year for revisions
reference	web address or generic information (for clones)
note worthy	anything special about the design
comments	catchall

VAX780	1.00	DMIPS		1.50
Z80	1.60		0.01	0.03
	2X		1X	3X