Small soft core uP Inventory
under 500 LUTs with source code

_uP_cores_test folder	opencores name	status	author	style / clone	data size	inst size	FPGA	reporter	comments	LUTs ALM	LUT?	mul ts	blk ram	F max	tool ver	MIPS /clk	clks/ inst	KIPS /LUT	src code	# src	top file	doc	tool chain	fltg pt	Ha vd	max data	ma x	byte adrs	# inst	# reg	pipe len	start year	last revis	reference	note worthy	comments
ag_6502	ag_6502 soft cor	beta	Oleg Odintsov	6502	8	8x	spartan-6-3	James Brakefiel		807	6	0	0	80	14.7	0.33	1.0	33	verilog	2	ag_6502		yes	N	N	64K	64K	Y				2012	2012	6502 data sheets	verilog code generation, "phase level accurate", 978 LUTs	
cpu6502_tru	cpu6502_tc	stable	Jens Gutschmidt	6502	8	8x	kintex-7-3	James Brakefiel		1678	6			159	14.7	0.33	1.0	31	vhdl	7	r6502_tc		yes	N	N	64K	64K	Y				2008	2010	6502 data sheets		
cpu65c02_tru	cpu65c02_tc	stable	Jens Gutschmidt	6502	8	8x	spartan-6-3	James Br	latch	4794	6			47	14.7	0.33	1.0	3	vhdl	8	core		yes	N	N	64K	64K	Y				2008	2013	6502 data sheets		
free6502		stable	David Kessner	6502	8	8x	spartan-6-3	James Brakefiel		663	6			89	14.7	0.33	1.0	44	vhdl	5	free6502	yes	yes	N	N	64K	64K	Y				1999	2000	6502 data sheets	microcoded	
lattice6502	Lattice 6502	beta	Ian Chapman	6502	8	8x	kintex-7-3	James Brakefiel		4942	6			214	14.7	0.33	1.0	14	vhdl	3	ghdl_proce	yes	yes	N	N	64K	64K	Y				2010	2010	6502 data sheets	targeted to LCMXO2280	huge LUT count
m65c02	M65C02	mature	Michael Morris	6502	8	8x	spartan-3	Michael Morris		661	4	0	3	74		0.33	1.0	37	verilog	13	M65C02	yes	yes	N	N	64K	64K	Y				2013	2014	6502 data sheets		
t65	T65 CPU	stable	Daniel Wallner	6502	8	8x	spartan-6-3	James Brakefiel		725	6			128	14.7	0.33	1.0	58	vhdl	7	T65	yes	yes	N	N	64K	64K	Y				2002	2010	6502 data sheets	6502, 65C02 & 65C816; wide use	
t65	T65 CPU	stable	Daniel Wallner	6502	8	8x	kintex-7-3	James Brakefiel		575	6			291	14.7	0.33	1.0	167	vhdl	7	T65	yes	yes	N	N	64K	64K	Y				2002	2010	6502 data sheets	6502, 65C02 & 65C816; wide use	
t6507lp	T6507LP	beta	Gabriel Oshiro, Samue	6502	8	8x	spartan-6-3	James Br	errors						14.7		1.0		verilog	22	t6507lp	yes	yes	N	N	64K	64K	Y				2009	2010	6502 data sheets	for use in ATARI 2600	
m65		stable	Naohiko Shimizu	6502	8	8x											1.0			8	m65cpu	yes	yes	N	N	4K	4K	Y				2001	2002	6502 data sheets	source files have unusual suffixes	
hd63701	HD63701 compa	planning	Tsuyoshi Hasegawa	6801	8	8x	spartan-3-5	James Brakefiel		1937	4	1	3	20	14.7	0.33	1.0	3	verilog	6	HD63701_CORE			N	N	64K	64K	Y				2014			Used in Atari game console, 6801 clone?	
hd63701	HD63701 compa	planning	Tsuyoshi Hasegawa	6801	8	8x	spartan-6-3	James Brakefiel		1412	6	1	3	31	14.7	0.33	1.0	7	verilog	6	HD63701_CORE			N	N	64K	64K	Y				2014			Used in Atari game console, 6801 clone?	
system68	System68	stable	John Kent, David Burne	6801	8	8x	spartan-3-5	James Brakefiel		2235	4		4	46	14.7	0.33	1.0	7	vhdl	21	cpu68	yes	yes	N	N	64K	64K	Y				2003	2009	6801 data sheets		
system05	SOC:system05	beta	John Kent	6805	8	8x	kintex-7-3	James Brakefiel		834	6			204	14.7	0.33	1.0	81	vhdl	10	System05	yes	yes	N	N	64K	64K	Y				2003	2009	6805 data sheets		
68hc05	68hc05	stable	Ulrich Riedel	6805	8	8x	kintex-7-3	James Brakefiel		1225	6			300	14.7	0.33	1.0	81	vhdl	1	6805		yes	N	N	64K	64K	Y				2007	2009	6805 data sheets		
68hc08	68hc08	stable	Ulrich Riedel	6808	8	8x	kintex-7-3	James Brakefiel		2290	6			101	14.7	0.33	1.0	15	vhdl	1	x68ur08		yes	N	N	64K	64K	Y				2007	2009	6808 data sheets		
6809_6309	6809_6309_com	beta	Alejandro Paz Schmidt	6809	8x	8x	spartan-6-3	James Brakefiel		2061	6			109	14.7	0.33	1.0	17	verilog	5	MC6809_cpu		yes	N	N	64K	64K	Y				2012	2013	6809 data sheets	includes 6309 op-codes, xilinx & lattice projects	
6809_6309	6809_6309_com	beta	Alejandro Paz Schmidt	6809	8x	8x	kintex-7-3	James Brakefiel		2207	6			212	14.7	0.33	1.0	32	verilog	5	MC6809_cpu		yes	N	N	64K	64K	Y				2012	2013	6809 data sheets	includes 6309 op-codes, xilinx & lattice projects	
system09	SOC:system09	stable	John Kent	6809	8x	8x	spartan-6-3	James Brakefiel		2127	6			64	14.7	0.33	1.0	10	vhdl	40	cpu09l	yes	yes	N	N	64K	64K	Y				2003	2012	6809 data sheets	from John Kent web page	
system09	SOC:system09	stable	John Kent	6809	8x	8x	kintex-7-3	James Brakefiel		1945	6			154	14.7	0.33	1.0	26	vhdl	40	cpu09l	yes	yes	N	N	64K	64K	Y				2003	2012	6809 data sheets	from John Kent web page	
mc6809e		beta	Flint Weller	6809	8x	8x	kintex-7-3	James Br	gate level pri		6				14.7	0.33	1.0	####	vhdl	26	core_6809	yes	yes	N	N	64K	64K	Y				1999		6809 data sheets	course work, ASIC orientation	
system11		alpha	John Kent, David Burne	6811	8	8x	kintex-7-3	James Brakefiel		1218	6			153	14.7	0.33	1.0	41	vhdl	17	cpu11	yes	yes	N	N	64K	64K	Y				2003	2009	6811 data sheets	known bugs & untested instructions	
dalton_8051		stable	Tony Givargis	8051	8	8x	kintex-7-3	James Brakefiel		2725	6	1	1	105	14.7	0.33	1.0	13	vhdl	7	i8051_all	yes	yes	N	N	64K	64K	Y				1999	2003	8051 data sheets	ASIC	www.cs.ucr.edu/~dalton/
light52	Lightweight 805	beta	Jose Ruiz	8051	8	8x	kintex-7-3	James Brakefiel		1027	6	1	1	148	14.7	0.17	1.0	24	vhdl	8	light52_cp	yes	yes	N	N	64K	64K	Y				2012	2013	8051 data sheets	targeted to area	
mc8051		stable	Helmut Mayrhofer	8051	8	8x	kintex-7-3	James Brakefiel		3022	6	1		83	14.7	0.33	1.0	9	vhdl	49	mc8051cor	yes	yes	N	N	256	64K	Y				1999	2013	www.oreganosystems.	fast 8051, version available with floating-point by David Lundgren	
t51	T51 mcu	alpha	Andreas Voggeneder	8051	8	8x	kintex-7-3	James Brakefield			6				14.7	0.33	1.0		vhdl	17	T8052	yes	yes	N	N	64K	64K	Y				2002	2010	8052 data sheets	8052 & 8032	
turbo8051	turbo 8051	beta	Dinesh Annayya	8051	8	8x	cyclone-2	Dinesh Annayya		5072	4			39	14.7	0.33	1.0	3	verilog	74	oc8051_to	yes	yes	N	N	64K	64K	Y				2011	2013	8051 data sheets	includes perpherials	
turbo8051	turbo 8051	beta	Dinesh Annayya	8051	8	8x	kintex-7-3	James Brakefiel		1985	6	1		127	14.7	0.33	1.0	21	verilog	74	oc8051_to	yes	yes	N	N	64K	64K	Y				2011	2013	8051 data sheets	includes perpherials	
cpu8080	8080 Compatible	stable	Scott Moore	8080	8	8x	spartan-6-3	James Brakefiel		1269	6			129	14.7	0.33	1.0	34	verilog	1	m8080	yes	yes	N	N	64K	64K	Y				2006	2009	8080 data sheets	includes VGA display generator, three variants	
light8080	Lightweight 808	stable	Jose Ruiz, Moti Litoche	8080	8	8x	kintex-7-3	James Brakefiel		154	6		1	247	14.7	0.17	1.0	265	verilog	5	i80soc	yes	yes	N	N	64K	64K	Y				2007	2012	8080 data sheets	targeted to area, includes UART, interrupt ctlr & RAM	
light8080	Lightweight 808	stable	Jose Ruiz, Moti Litoche	8080	8	8x	spartan-6	James Brakefiel		148	6		3	172	14.7	0.17	1.0	192	verilog	5	light8080	yes	yes	N	N	64K	64K	Y				2007	2012	8080 data sheets	targeted to area, bare core	
light8080	Lightweight 808	stable	Jose Ruiz, Moti Litoche	8080	8	8x	kintex-7-3	James Brakefiel		154	6		1	247	14.7	0.17	1.0	265	verilog	5	light8080	yes	yes	N	N	64K	64K	Y				2007	2012	8080 data sheets	targeted to area, bare core	
light8080	Lightweight 808	stable	Jose Ruiz, Moti Litoche	8080	8	8x	spartan-6	James Brakefiel		150	6		3	142	14.7	0.17	1.0	156	vhdl	5	light8080	yes	yes	N	N	64K	64K	Y				2007	2012	8080 data sheets	targeted to area, bare core	
t80	T80 cpu	stable	Daniel Wallner	8080	8	8x	spartan-6-3	James Br	8080	958	6			95	14.7	0.33	1.0	33	vhdl	16	T8080se	yes	yes	N	N	64K	64K	Y				2002	2011	z80 data sheets	Z80 & 8080 inst sets, several usage	
gl85		stable	Alex Miczo	8085	8	8x	kintex-7-3	James Br	gate level des		6				14.7	0.33	1.0	####	vhdl	1	i8085	yes	yes	N	N	64K	64K	Y				1993		8085 data sheets	also a TTL implementation in VHDL	
cpu86		beta	ht-lab.com	8086	8	8x	kintex-7-3	James Brakefiel		3421	6	1		127	14.7	0.17	1.0	6	vhdl	23	cpu86_top	yes	yes	N	N	1M	1M	Y				2002	2010	x86 data sheets	8088 clone	www.ht-lab.com
next186	Next 80186 proc	stable	Nicolae Dumitrache	8086	8x	8x	arria-2	James Brakefiel		1966	6	1		83	14.7	0.33	1.0	14	verilog	4	Next186_C	yes	yes	N	N	1M	1M	Y				2012	2013	x86 data sheets	boots DOS	
next186	Next 80186 proc	stable	Nicolae Dumitrache	8086	8x	8x	spartan-6-3	James Brakefiel		2716	6	1		44	14.7	0.33	1.0	5	verilog	4	Next186_C	yes	yes	N	N	1M	1M	Y				2012	2013	x86 data sheets	boots DOS	
next186	Next 80186 proc	stable	Nicolae Dumitrache	8086	8x	8x	kintex-7-3	James Brakefiel		2500	6	1		94	14.7	0.33	1.0	12	verilog	4	Next186_C	yes	yes	N	N	1M	1M	Y				2012	2013	x86 data sheets	boots DOS	
rtf8088	rtf8088	planning	Robert Finch	8086	8x	8x	kintex-7-3	James Brakefiel		4514	6	4		174	14.7	0.67	1.0	26	verilog	57	rtf8088	yes	yes	N	N	1M	1M	Y				2012	2013	x86 data sheets		
zet86	Zet The x86 (IA-	alpha	Zeus Marmolejo	8086	8x	8x	kintex-7-3	James Brakefiel		3642	6	1		68	14.7	0.67	1.0	12	verilog	32	fpga_zet_t	yes	yes	N	N	1M	1M	Y				2008	2014	x86 data sheets	equivalent to 80186, boots MS-DOS	zet.aluzina.org/index.php/Zet_pro
ao68000	ao68000	beta	Aleksander Osman	68000	8x	16x	arria-2	James Brakefiel		3479	A		6	169	13.1	1.00	1.0	49	verilog	1	ao68000	som	yes	N		4G	4G	Y				2010	2011	68000 data sheets	uses microcode, 4750 LUTs	
tg68	TG68 execute 68	stable	Tobias Gubener	68000	8x	16x	kintex-7-3	James Brakefiel		2331	6			44	14.7	0.67	1.0	13	vhdl	2	TG68_fast	yes	yes	N	N	4G	4G	Y		16		2007	2012	68000 data sheets	for use with Minimig	
v1_coldfire		stable	IPextreme	68000	8x	16x	cyclone-3	freescale		5000	4			80		0.89	1.0	14					yes	N	N	4G	4G	Y		16		2008		68000 data sheets	free for Cyclone III	
agcnorm	Apollo Guidance	beta	Dave Roberts	?	16	16											1.0		vhdl	5	AGC	some		N		32M	32M					2010	2012		Apollo Guidance Computer via NOR gate emulation	
gup	HC11 Compatibl	stable	Kevin Phillipson	68C11	8x	8x	kintex-7-3	James Br	missing uP fil		6				14.7	0.67	1.0	####	vhdl	25	?	yes	yes	N	N	64K	64K	N				2008	2009	6811 data sheets	68HC11 compatible	
hc11core		stable	Green Mountain Comp	68HC11	8x	8x	kintex-7-3	James Brakefiel		2014	6			125	14.7	0.33	1.0	21	vhdl	1	hc11rtl	yes	yes	N	N	64K	64K	N	53	8	2	2000		6811 data sheets	restricted use license, no divide inst	
ARM_Cortex_A9		ASIC	ARM	ARM a9	32	16	zynq	xilinx		4500	6			1000		2.50	1.0	556	asic				yes	yes	Y		4G	4G	Y	80	16	10		2012	xilinx plan ahead: an A	uses pro-rated LC area	dual issue, includes fltg-pt & MMU
ARM_Cortex_A9		ASIC	ARM	ARM a9	32	16	arria V	altera		4500	A			1050		2.50	1.0	583	asic				yes	yes	Y		4G	4G	Y	80	16	10		2012	altera data sheets	uses pro-rated LC area	dual issue, includes fltg-pt & MMU
ARM_Cortex_A9		ASIC	ARM	ARM a9	32	16	cyclone V	altera		4500	A			925		2.50	1.0	514	asic				yes	yes	Y		4G	4G	Y	80	16	10		2012	altera data sheets	uses pro-rated LC area	dual issue, includes fltg-pt & MMU
amber	Amber ARM-cor	stable	Conor Santifort	ARM7	32	32	kintex-7-3	James Br	slow,	12450	6		4	98	14.7	0.90	1.0	7	verilog	25	a25_core	yes	yes	N		4G	4G	Y				2010	2013	ARM7 data sheets	no MMU	4096 single port RAM LUTs
storm_core	Storm Core (ARM	beta	Stephan Nolting	ARM7	32	32	kintex-7-3	James Brakefiel		2312	6	3		179	14.7	1.00	1.0	77	vhdl	16	CORE	yes	yes	N	N	4G	4G	Y		32	8	2011	2013		I & D caches not compiled	
storm_core	Storm Core (ARM	beta	Stephan Nolting	ARM7	32	32	kintex-7-3	James Brakefiel		3514	6	3	4	157	14.7	1.00	1.0	45	vhdl	16	STORM_TC	yes	yes	N	M	4G	4G	Y		32	8	2011	2013		I & D caches	
oks8	oks8	alpha	Kongzilee	ARM7	32	32											1.0		verilog	8	oks8	yes	yes	N		64K	64K	Y				2006	2009		clone of KS86C4204/C4208/P4208, SAM87RI instruction set	
avr_core	avr_core	stable	Rusian Lepetenok	AVR	8	16	kintex-7-3	James Br	errors	2135	6			127	14.7	0.33	1.0	20	verilog		avr_core		yes	N		64K	128K	Y		32		2002	2012	AVR data sheets	VHDL core included	
avr_hp	avr_hp	stable	Strauch Tobias	AVR	8	16	kintex-7-3	James Br	1 slot	1199	6			127	14.7	0.33	1.0	35	vhdl	9	avr_core	som	yes	N		64K	128K	Y		32		2010	2010	AVR data sheets	hyper pipelined (eg barrel) AVR	
avr_hp	avr_hp	stable	Strauch Tobias	AVR	8	16	kintex-7-3	James Br	2 slot	1554	6			223	14.7	0.33	1.0	47	vhdl	10	avr_core_c	som	yes	N		64K	128K	Y		32		2010	2010	AVR data sheets	hyper pipelined (eg barrel) AVR	
avr_hp	avr_hp	stable	Strauch Tobias	AVR	8	16	kintex-7-3	James Br	3 slot	1812	6			243	14.7	0.33	1.0	44	vhdl	10	avr_core_c	som	yes	N		64K	128K	Y		32		2010	2010	AVR data sheets	hyper pipelined (eg barrel) AVR	
avr_hp	avr_hp	stable	Strauch Tobias	AVR	8	16	kintex-7-3	James Br	4 slot	2054	6			278	14.7	0.33	1.0	45	vhdl	10	avr_core_c	som	yes	N		64K	128K	Y		32		2010	2010	AVR data sheets	hyper pipelined (eg barrel) AVR	
avr8	Reduced AVR Co	beta	Nick Kovach	AVR	8	16	kintex-7-3	James Brakefiel		174	6			418	14.7	0.33	1.0	792	verilog	1	rAVR	yes	yes	N		64K	64K	Y	17	4		2010	2010	AVR data sheets	not a full clone, doc is opencores page	
avrtinyx61co	avrtinyx61core	beta	Andreas Hilvarsson	AVR	8	16	kintex-7-3	James Brakefiel		1243	6			194	14.7	0.33	1.0	51	vhdl	1	mcu_core		yes	N		64K	128K	Y		32		2008	2009	AVR data sheets		
ax8	AX8 MCU	stable	Daniel Wallner	AVR	8	16	spartan-6-3	James Br	missing ROM		6				14.7		1.0		vhdl	14	A90S1200			N		64K	128K	Y		32		2002	2009	AVR data sheets	both A90S1200 & A90S2313	
navre	Navre AVR clone	stable	Sebastien Bourdeaudu	AVR	8	16	cyclone-4-6	James Brakefiel		1561	4			113	13.1	0.33	1.0	24	verilog	1	softusb_na	yes	yes	N		64K	64K	Y		32	2	2010	2013	AVR data sheets	AVR clone, part of www.milkymist.org	
navre	Navre AVR clone	stable	Sebastien Bourdeaudu	AVR	8	16	arria-2	James Brakefiel		1126	A			182	13.1	0.33	1.0	53	verilog	1	softusb_na	yes	yes	N		64K	64K	Y		32	2	2010	2013	AVR data sheets	AVR clone, part of www.milkymist.org	
navre	Navre AVR clone	stable	Sebastien Bourdeaudu	AVR	8	16	cyclone-5	James Brakefiel		783	A			115	13.1	0.33	1.0	49	verilog	1	softusb_na	yes	yes	N		64K	64K	Y		32	2	2010	2013	AVR data sheets	AVR clone, part of www.milkymist.org	
navre	Navre AVR clone	stable	Sebastien Bourdeaudu	AVR	8	16	spartan-6-3	James Brakefiel		1038	6			116	14.7	0.33	1.0	37	verilog	1	softusb_na	yes	yes	N		64K	64K	Y		32	2	2010	2013	AVR data sheets	AVR clone, part of www.milkymist.org	
navre	Navre AVR clone	stable	Sebastien Bourdeaudu	AVR	8	16	kintex-7-3	James Brakefiel		990	6			207	14.7	0.33	1.0	69	verilog	1	softusb_na	yes	yes	N		64K	64K	Y		32	2	2010	2013	AVR data sheets	AVR clone, part of www.milkymist.org	
riscmcu	RISC Microcontr	stable	Yapzihe	AVR	8	16	arria-2	James Br	LPM paramet		6				14.7	0.33	1.0	####	vhdl	15	v_riscmcu	yes	yes	N		128	512	Y	92	16		2002	2009	AVR data sheets		
t400	T400 uControlle	stable	Arnim Laeuger	COP400	4	8x	cyclone-1	Arnim Laeuger		583	4		2	59		0.17	1.0	17	vhdl	53	t400_core	yes	asm	N		256	1K					2006	2009	COP400 data sheets	several variants	
t400	T400 uControlle	stable	Arnim Laeuger	COP400	4	8x	spartan-2	Arnim Laeuger		643	4		2	60		0.17	1.0	16	vhdl	53	t400_core	yes	asm	N		256	1K					2006	2009	COP400 data sheets	several variants	
aspida	ASPIDA DLX core	stable	Sotiriou	DLX	32	32	kintex-7-3	James Brakefiel		3586	6			257	14.7	1.00	1.0	72	verilog	10	DLX_top	yes	yes			4G	4G					2002	2009	Knuth DLX		compiled sync version
t48	T48 uController	stable	Arnim Laeuger	MCS-48	8	8x	cyclone-1	Arnim Laeuger		738	4		1	59		0.33	1.0	26	vhdl	70	t48_core	yes	asm	N		256	1K					2004	2009	MCS-48 data sheets	used in several projects	
t48	T48 uController	stable	Arnim Laeuger	MCS-48	8	8x	spartan-2	Arnim Laeuger		771	4		1	30		0.33	1.0	13	vhdl	70	t48_core	yes	asm	N		256	1K					2004	2009	MCS-48 data sheets	used in several projects	
Ion	Ion MIPS compa	mature	Jose Ruiz	MIPS	32	32	virtex-5	Jose Ruiz		2017	6			104		1.00	1.0	52	vhdl	12	mips_soc	yes	yes	N		4G	4G	Y		32		2011	2014		MIPS R3000 clone	
Ion	Ion MIPS compa	mature	Jose Ruiz	MIPS	32	32	kintex-7-3	James Brakefiel		1533	6			163	14.7	1.00	1.0	106	vhdl	12	mips_soc	yes	yes	N		4G	4G	Y		32		2011	2014		MIPS R3000 clone	
minimips	miniMIPS	stable	Poppy etal	MIPS	32	32	kintex-7-3	James Brakefiel		2939	6	8		118	14.7	1.00	1.0	40	vhdl	12	minimips	yes	yes	N		4G	4G	Y		32	5			MIPS I		
mips_fault_t	Mips-FaultToler	stable	Lazaridis	MIPS	32	32											1.0		vhdl			yes	yes	N		4G	4G	Y		32		2013		MIPS data sheets	arithmetic includes fault detection	
mips32r1	MIPS32 Release	stable	Grant Ayers	MIPS	32	32	kintex-7-3	James Brakefiel		4822	6	8		90	14.7	1.00	1.0	19	verilog	20	processor	yes	yes	N		4G	4G	Y		32		2012	2014	MIPS data sheets	Harvard arch	
mips789	mips789	stable	Li Wei	MIPS	32	32	kintex-7-3	James Brakefiel		1432	6		1	171	14.7	1.00	1.0	119	verilog	10	mips_core	yes	yes	N		4G	4G	Y		32		2007	2009	MIPS data sheets		
mipsr2000	mipsr2000	stable	Lazaridis Dimitris	MIPS	32	32	kintex-7-3	James Brakefiel		1971	6	4	6	71	14.7	1.00	1.0	36	vhdl	35	Dm	yes	yes	N		4G	4G	Y		32	5	2012	2013	MIPS data sheets	course project	
plasma	Plasma most MI	stable	Steve Rhoads	MIPS	32	32	kintex-7-3	James Brakefiel		2462	6		3	97	14.7	1.00	1.0	40	vhdl	22	plasma	yes	yes	N		4G	4G	Y		32		2001	2013	MIPS data sheets	wide outside use, opencores page has list of related publications	
ucore	Ucore	stable	Whitewill	MIPS	32	32	kintex-7-3	James Brakefiel		2469	6		1	231	14.7	1.00	1.0	93	verilog	25	ucore	yes	yes	N		4G	4G	Y		32	6	2005	2010	MIPS data sheets	MMU & caches	
yacc	YACC Yet Anothe	stable	Tak Sugawara	MIPS	32	32	kintex-7-3	James Br	xilinx IP prob		6				14.7	1.00	1.0	####	verilog	10	yacc2	yes	yes	N		4G	4G	Y		32	5	2005	2009	MIPS data sheets	derived from, but independent of plasma, xilinx & altera implemntatio	

m1_core	M1 Core	beta	Fabrizo Fazzino, Albert	MIPS?	32	32	kintex-7-3	James Brakefiel		3456	6			233	14.7	1.00	1.0	67	verilog	9	m1_core		yes	N		4G	4G	Y		32		2007	2012		GCC target?	
openmsp430	openMSP430	stable	Oliver Girard	msp430	16	16x	cyclone-4-6	Oliver Girard		1750	A	1		52		0.67	1.0	20	verilog	30	openMSP4	yes	yes	N	N	64K	64K	Y		16		2009	2014	msp430 data sheets	implemented on four FPGAs, performance spreadsheet	
openmsp430	openMSP430	stable	Oliver Girard	msp430	16	16x	stratix-3-2	Oliver Girard		1147	A	1		98		0.67	1.0	57	verilog	30	openMSP4	yes	yes	N	N	64K	64K	Y		16		2009	2014	msp430 data sheets	implemented on four FPGAs, performance spreadsheet	
openmsp430	openMSP430	stable	Oliver Girard	msp430	16	16x	spartan-6-4	Oliver Girard		1424	6	1		68		0.67	1.0	32	verilog	30	openMSP4	yes	yes	N	N	64K	64K	Y		16		2009	2014	msp430 data sheets	implemented on four FPGAs, performance spreadsheet	
openmsp430	openMSP430	stable	Oliver Girard	msp430	16	16x	virtex-6-3	Oliver Girard		1387	6	1		116		0.67	1.0	56	verilog	30	openMSP4	yes	yes	N	N	64K	64K	Y		16		2009	2014	msp430 data sheets	implemented on four FPGAs, performance spreadsheet	
nios2		proprietar	Altera	Nios II	32	32	cyclone-4-6	Altera		2065	4			160		1.13	1.0	87	no source			yes	yes	opt		4G	4G	Y		32		2004		NIOS2 data sheets	fltg-pt, caches & MMU options	Nios II/f: fastest version
nios2		proprietar	Altera	Nios II	32	32	arria-2	Altera		1355	A			170		1.13	1.0	141	no source			yes	yes	opt		4G	4G	Y		32		2004		NIOS2 data sheets	fltg-pt, caches & MMU options	Nios II/f: fastest version
nios2		proprietar	Altera	Nios II	32	32	cyclone-5	Altera		1050	A			160		1.13	1.0	171	no source			yes	yes	opt		4G	4G	Y		32		2004		NIOS2 data sheets	fltg-pt, caches & MMU options	Nios II/f: fastest version
nios2		proprietar	Altera	Nios II	32	32	arria-5	Altera		1355	A			280		1.13	1.0	232	no source			yes	yes	opt		4G	4G	Y		32		2004		NIOS2 data sheets	fltg-pt, caches & MMU options	Nios II/f: fastest version
nios2		proprietar	Altera	Nios II	32	32	stratix-5	Altera		895	A			310		1.13	1.0	390	no source			yes	yes	opt		4G	4G	Y		32		2004		NIOS2 data sheets	fltg-pt, caches & MMU options	Nios II/f: fastest version
nios2		proprietar	Altera	Nios II	32	32	cyclone-4-6	Altera		1915	4			130		0.64	1.0	43	no source			yes	yes	opt		4G	4G	Y		32		2004		NIOS2 data sheets	fltg-pt, caches & MMU options	Nios II: balanced version
nios2		proprietar	Altera	Nios II	32	32	arria-2	Altera		1045	A			170		0.64	1.0	103	no source			yes	yes	opt		4G	4G	Y		32		2004		NIOS2 data sheets	fltg-pt, caches & MMU options	Nios II: balanced version
nios2		proprietar	Altera	Nios II	32	32	cyclone-5	Altera		785	A			140		0.64	1.0	113	no source			yes	yes	opt		4G	4G	Y		32		2004		NIOS2 data sheets	fltg-pt, caches & MMU options	Nios II: balanced version
nios2		proprietar	Altera	Nios II	32	32	arria-5	Altera		1045	A			250		0.64	1.0	152	no source			yes	yes	opt		4G	4G	Y		32		2004		NIOS2 data sheets	fltg-pt, caches & MMU options	Nios II: balanced version
nios2		proprietar	Altera	Nios II	32	32	stratix-5	Altera		650	A			300		0.64	1.0	293	no source			yes	yes	opt		4G	4G	Y		32		2004		NIOS2 data sheets	fltg-pt, caches & MMU options	Nios II: balanced version
nios2		proprietar	Altera	Nios II	32	32	cyclone-4-6	Altera		1080	4			170		0.15	1.0	24	no source			yes	yes	N		4G	4G	Y		32		2004		NIOS2 data sheets	serial arithmetic	Nios II/e: minimum LUTs version
nios2		proprietar	Altera	Nios II	32	32	arria-2	Altera		730	A			300		0.15	1.0	62	no source			yes	yes	N		4G	4G	Y		32		2004		NIOS2 data sheets	serial arithmetic	Nios II/e: minimum LUTs version
nios2		proprietar	Altera	Nios II	32	32	cyclone-5	Altera		420	A			200		0.15	1.0	71	no source			yes	yes	N		4G	4G	Y		32		2004		NIOS2 data sheets	serial arithmetic	Nios II/e: minimum LUTs version
nios2		proprietar	Altera	Nios II	32	32	arria-5	Altera		730	A			320		0.15	1.0	66	no source			yes	yes	N		4G	4G	Y		32		2004		NIOS2 data sheets	serial arithmetic	Nios II/e: minimum LUTs version
nios2		proprietar	Altera	Nios II	32	32	stratix-5	Altera		445	A			340		0.15	1.0	115	no source			yes	yes	N		4G	4G	Y		32		2004		NIOS2 data sheets	serial arithmetic	Nios II/e: minimum LUTs version
pdp11-34verilog		stable	Brad Parker	PDP11	8x	16x	kintex-7-3	James Brakefiel		3089	6			153	14.7	0.67	1.0	33	verilog	24	pdp11	yes	yes	N	N	64K	64K			8		2009		PDP11 data sheets	boots & runs RT-11, EIS inst & MMU	www.heeltoe.com/download/pdp
w11	PDP-11/70 CPU	alpha	Walter Mueller	PDP11	8x	16x	spartan-6	Walter Mueller		3418	6			80		0.67	1.0	16	vhdl	26	pdp11	yes	yes	N	N	4M	4M	Y		8		2010	2013	PDP11 data sheets	Boots UNIX, has MMU & cache, retro project	
pdp8	PDP-8 Processor	alpha	Joe Manojlovick, Rob D	PDP8	12	12	spartan-6-3	James Brakefiel		1332	6	1		81	14.7	0.50	2.0	15	vhdl	55	cpu	yes	yes	N	N	32K	32K			8		2012	2013	PDP8 data sheets	Boots OS/8, runs apps, several variants	
pdp8	PDP-8 Processor	alpha	Joe Manojlovick, Rob D	PDP8	12	12	kintex-7-3	James Brakefiel		1219	6	1		183	14.7	0.50	2.0	37	vhdl	55	cpu	yes	yes	N	N	32K	32K			8		2012	2013	PDP8 data sheets	Boots OS/8, runs apps, several variants	
pdp8l	Minimal PDP8/L	beta	Ian Schofield	PDP8	12	12	cyclone-3	James Brakefiel		1088	4			107	14.7	0.50	2.0	24	vhdl	11	top	yes	yes	N	N	4K	4K					2013		PDP8 data sheets		
pdp8verilog		stable	Brad Parker	PDP8	12	12	spartan-6-3	James Brakefiel		509	6			162	14.7	0.50	2.0	79	verilog	18	pdp8	yes	yes	N	N	32K	32K			8		2005	2010	PDP8 data sheets	boots & runs TSS/8 & Basic	www.heeltoe.com/download/pdp
pdp8verilog		stable	Brad Parker	PDP8	12	12	kintex-7-3	James Brakefiel		505	6			366	14.7	0.50	2.0	181	verilog	18	pdp8	yes	yes	N	N	32K	32K			8		2005	2010	PDP8 data sheets	boots & runs TSS/8 & Basic	www.heeltoe.com/download/pdp
pdp8verilog		stable	Brad Parker	PDP8	12	12	kintex-7-3	James Brakefiel		1117	6			251	14.7	0.50	2.0	56	verilog	18	top	yes	yes	N	N	32K	32K			8		2005	2010	PDP8 data sheets	boots & runs TSS/8 & Basic	www.heeltoe.com/download/pdp
free_risc8		stable	Thomas Coonan	PIC16	8	14	kintex-7-3	James Brakefiel		355	6			142	14.7	0.33	1.0	132	verilog	8	cpu	yes	yes	N		256	4K	Y				2002	2011	PIC16 data sheets		
lwrisc	ClaiRISC	stable	Li Wu	PIC16	8	14	arria-2	James Br	undefined co		A				13.1	0.33	1.0	####	verilog	9	risc_core				Y							2008	2009	PIC16 data sheets		
minirisc	Mini-Risc core	stable	Rudolf Usselmann	PIC16	8	14	spartan-3	Rudolf Usselma		460	4			80		0.33	1.0	57	verilog	7	risc_core_	yes	yes	N	Y	256	4K	Y				2001	2012	PIC16 data sheets		
p16c5x	P16C5x	mature	Michael Morris	PIC16	8	14	spartan-3	Michael Morris		488	4		3	60		0.33	1.0	41	verilog	3	P16C5x	yes	yes	N	Y	256	4K	Y				2013	2014	PIC16 data sheets		
ppx16	PPX16 mcu	stable	Daniel Wallner	PIC16	8	14	spartan-6-3	James Br	missing ROM BB						14.7		1.0		vhdl	10	P16C55, P1	yes	yes	N	Y	256	4K	Y				2002	2009	PIC16 data sheets	both 16C55 & 16F84	
recore54		beta	ht-lab.com	PIC16	8	14	kintex-7-3	James Br	Cannot find <		6				14.7	0.33	1.0	####	vhdl	20	rcore54_sy	yes	yes	N	Y	256	4K	Y				1999		PIC16 data sheets	PIC16 clone	www.ht-lab.com
risc16f84	risc16f84	stable	John Clayton	PIC16	8	14	kintex-7-3	James Brakefiel		331	6			333	14.7	1.00	1.0	1007	verilog	1	risc16f84_	yes	yes	N	Y	256	4K	Y				2002	2013	PIC16 data sheets	derived from CQPIC by Sumio Morioka	
risc5x	RISC5x	stable	MikeJ	PIC16	8	14	kintex-7-3	James Br	errors in usin		6				14.7	0.33	1.0	####	vhdl	15	cpu	yes	yes	N	Y	256	4K	Y				2002	2011	PIC16 data sheets	makes extensive use of xilinx primitives	
ae18	ae18	beta	Shawn Tan	PIC18	16	24	arria-2	James Brakefiel		1084	A	1		207	13.1	0.67	1.0	128	verilog	1	ae18_core		yes	N	Y	4K	1M					2003	2009	PIC18 data sheets	not 100% compatable	negative edge reset "clock"
ae18	ae18	beta	Shawn Tan	PIC18	16	24	spartan-6-3	James Brakefiel		1176	6	1		81	14.7	0.67	1.0	46	verilog	1	ae18_core		yes	N	Y	4K	1M					2003	2009	PIC18 data sheets	not 100% compatable	negative edge reset "clock"
ae18	ae18	beta	Shawn Tan	PIC18	16	24	virtex-6-3	James Brakefiel		1133	6	1		117	14.7	0.67	1.0	69	verilog	1	ae18_core		yes	N	Y	4K	1M					2003	2009	PIC18 data sheets	not 100% compatable	negative edge reset "clock"
ae18	ae18	beta	Shawn Tan	PIC18	16	24	kintex-7-3	James Brakefiel		1131	6	1		68	14.7	0.67	1.0	41	verilog	1	ae18_core		yes	N	Y	4K	1M					2003	2009	PIC18 data sheets	not 100% compatable	negative edge reset "clock"
copyblaze	copyBlaze	stable	Abdallah ElIbrahimi	picoBlaze	8	18	spartan-6-3	James Brakefiel		619	6			86		0.33	1.0	46	vhdl	16	cp_copybla	yes	asm	N		256	2K	Y				2011	2013	microBlaze data sheets	wishbone extras	LUT count high, Fmax low: see pic
pacoBlaze		mature	Pablo Kocik	picoBlaze	8	18	spartan-3	Pablo Kocik		177	4		1	117		0.33	1.0	218	verilog	18	pacoblaze	yes	asm			8	11	Y	57		2		2006	bleyer.org/pacoblaze	3 versions, behavioral coding	
picoblaze	picoblaze	stable	Ken Chapman	picoBlaze	8	18	spartan-3-4	James Brakefiel		178	4			182	14.7	0.33	1.0	338	vhdl	1	kcspm3	yes	asm	N		256	2K	Y				2003		picoblaze data sheets	2 clocks per inst	this is the original picoBlaze autho
mips_16	Educational 16-b	stable	Doyya Doyya	RISC	16	16	kintex-7-3	James Br	collapsed in c		6				14.7	1.00	1.0	####	verilog	12	mips_16_c	yes		N		64K	64K		13	8	5	2012	2012			
leon		stable	Jiri Gaisler, Jan Anders	SPARC	32	32			hard to find min configuration								1.0		vhdl	100s	leon3x	yes	yes	Y		4G	4G			64		2003	2013	SPARC data sheets	customized for ~20 FPGA boards, configurable	
s1_core	S1 Core	stable	Fabrizio Fazzino etal	SPARC	64	32	kintex-7-3	James Brakefiel		54434	6	8	57	50	14.7	1.00	1.0	1	verilog	136	s1_top	yes	yes	N	M	4G	4G	Y		32		2007	2012	SPARC data sheets	reduced version of OpenSPARC T1	
aquarius	aquarius	stable	Thorn Aitch	SuperH-2	32	16	kintex-7-3	James Brakefiel		3958	6	2		86	14.7	1.00	1.0	22	verilog	21	top	yes	yes	N		4G	4G	Y				2003	2009	SuperH data sheets		
aeMB	aeMB	beta	Shawn Tan	uBlaze	32	32	kintex-7-3	James Brakefiel		1018	6	3		131	14.7	1.30	1.0	167	verilog	29	aeMB_core	yes	yes	N		4G	4G	Y				2004	2009	xilinx documentation	not 100% compatable	
mblite	MB-Lite	beta	Tamar Kranenburg	uBlaze	32	32	virtex-5				6			229			1.0		vhdl	10	core	yes	yes	N		4G	4G	Y	86	32		2009	2012	microBlaze data sheets	not all instructions implemented	
microblaze		proprieta	Xilinx	uBlaze	32	32	kintex-7	Xilinx		1201	6		32	408		1.30	1.0	441	not avail			yes	yes	opt		32	32	Y	86	32	5	2002		www.xilinx.com/tools/	performance optimized	70 configuration options, MMU op
microblaze		proprieta	Xilinx	uBlaze	32	32	kintex-7	Xilinx		546	6		1	264		1.03	1.0	498	not avail			yes	yes	opt		32	32	Y	86	32	3	2002		www.xilinx.com/tools/	area optimized	70 configuration options, MMU op
myblaze	myBlaze	mature	Jian Luo	uBlaze	32	32											1.0		myhdl			yes	yes	N		4G	4G	Y		32		2010	2010	microBlaze data sheets	clone, no VHDL in tar file	
openfire_cor	OpenFire Proces	alpha	Alex Marschner, Steph	uBlaze	32	32	kintex-7-3	James Br	empty projec		6				14.7	0.33	1.0	####	verilog	12	openfire_c	yes	yes	N	N	4G	4G	Y		32		2007	2009	uBlaze data sheets	"FPGA Proven"	
secretblaze		beta	Lyonel Barthe	uBlaze	32	32	spartan-3-4	Lyonel Barthe		1563	4			91	12.1	1.00	1.0	58	vhdl	26	sb_core		yes			4G	4G	Y	86	32	5	2010	2012	www.lirmm.fr/ADAC/		
nextz80	NextZ80	stable	Nicolae Dumitrache	Z80	8	8x	kintex-7-3	James Brakefiel		1064	6			106	14.7	0.67	1.0	66	verilog	3	NextZ80CP	yes	yes	N	N	64K	64K	Y				2011	2014	z80 data sheets		
t80	T80 cpu	stable	Daniel Wallner	Z80	8	8x	spartan-6-3	James Br	Z80 m	1462	6			83	14.7	0.33	1.0	19	vhdl	16	T80a	yes	yes	N	N	64K	64K	Y				2002	2011	z80 data sheets	Z80 & 8080 inst sets, several usage	
t80	T80 cpu	stable	Daniel Wallner	Z80	8	8x	kintex-7-3	James Brakefiel		1389	6			163	14.7	0.67	1.0	79	vhdl	16	T80a	yes	yes	N	N	64K	64K	Y				2002	2011	z80 data sheets	Z80 & 8080 inst sets, several usage	
tv80	TV80	mature	Guy Hutchison, Howar	Z80	8	8x	kintex-7-3	James Brakefiel		1207	6			182	14.7	0.67	1.0	101	verilog	6	tv80n	yes	yes	N	N	64K	64K	Y				2004	2012	z80 data sheets	derived from Daniel Wallner's T80, ASIC implementations	
wb_z80	Wishbone High I	stable	Brewster Porcella	Z80	8	8x	kintex-7-3	James Brakefiel		2025	6			144	14.7	0.67	1.0	48	verilog	4	z80_core_	yes	yes	N	N	64K	64K	Y				2004	2012	z80 data sheets	derived from Guy Hutchison TV80	
y80e	Y80e Z80/Z180 c	stable	Sergey Belyashov	Z80	8	8x	kintex-7-3	James Br	empty projec		6				14.7	1.00	1.0	####	verilog	15	y80_top	yes	yes	N	N	64K	64K	Y				2013	2013	z80 data sheets	based on Y80 from "Microprocessor Design Using Verilog HDL" by Mon	

0 # usable(beta, stable or mature): "A"(clones) & "W"(origina # reg bits

0 "B" or "X" of limited interest

adr locations

Web page DMIPS per clock cycle per core en.wikipec community.freescale.com/thread/60391

MIPS/MHz Pro-rating for data size:

1-bit	0.04
8-bit	0.33
16-bit	0.67
32-bit	1.00

Silicon Area equivalents

LUTS/DSP48	16:1
LUTS/Block RAM	32:1

Under the assumption that the core is capable of one instuction per clock

Following has DMIPS per clock for many microprocessors
http://en.wikipedia.org/wiki/Instructions_per_second

Column Titles	Details
"A"	A: 1st choice clone, B: 2nd choice clone, W: 1st choice original, X: 2nd choice original
"B"	currently unused and hidden
_uP_cores_test folder	if opencores design is their folder name, otherwise my folder name
opencores name	
status	ASIC, planning, alpha, beta, stable, mature, proprietary
author	First Name, Last Name
style / clone	part number or "forth", RISC, accumulator, etc
data size	data memory word size
inst size	instruction size
FPGA	FPGA family for compile, place, route & timing
reporter	First Name, Last Name
comments	compile, place, route & timing problems
LUTs ALM	4-LUT, 6-LUT, Altera ALM, Actel Tile
LUT?	total number of LUTs or ALMs used including route-thrus & otherwise unavailable

uP	MIPS			CoreMarks /MHz	MHz	
4004	0.10					
6502	0.50		0.02	0.06		
8051			0.08	0.24		
8080	0.17			0.25		
68K	0.10			0.15		
ARM Cortex A9	2.50	DMIPS		5.93	1000	
ARM Cortex M0	0.90	DMIPS		1.50	70	
ARM Cortex M3	1.25	DMIPS		2.92	25	
ARM7	0.90		0.74	2.04	600	
AVR	1.00		0.21	0.53	8	
AVR32				1.62	60	
BA21				2.44	400	
Coldfire				2.80	400	
Coldfire				0.77	150	Virtex-5
HCS08			0.04	0.12		
LEON3/Spartan-6				1.96	100	
MC6809	1.24		0.07	1.86		
MicroBlaze 3-stage	1.03			1.50		
MicroBlaze 5-stage	1.38			1.90	125	
MIPS32	1.51			2.28		

mults	total number of multipliers/DSPs used
blk RAM	total number of block RAMs used, does not include small and extra large Altera block RAMs, Xilinx half block RAM rounded up
Fmax	maximum primary clock speed from compile, place, route & timing run
tool ver	Altera, Xilinx, Lattice Semiconductor or MicroSemi tool version number
MIPS /clk	prorated DMIPS per clock, reduced for data word sizes under 32-bits, greater than one for multiple issue processors
clks/ inst	number of clocks per instruction, typically 1.0 for modern pipelined processors
KIPS /LUT	figure of merit, does not include effects of memory capacity, floating point or instruction set quality
src code	VHDL or Verilog or other
# src files	number of source files for compile, place, route & timing
top file	top file for compile, place, route & timing run
doc	is documentation provided
tool chain	is there a compiler or assembler provided or available
fltg pt	does the compile, place, route & timing run include floating point
Ha vd	separate instruction and data memory(s), there can be more than one data memory, M for MMU & caches
max data	maximum data address
max inst	maximum instruction address
byte adrs	is byte addressing provided
# inst	number of unique instructions, somewhat subjective
# reg	number of registers in register file
pipe len	number of pipeline stages
start year	year of first design activity
last revis	last year for revisions
reference	web address or generic information (for clones)
note worthy	anything special about the design
comments	catchall

MSP430			0.40	1.20	
MSP430				1.10	25
Nios II	0.64	DMIPS		0.93	200
Nios II -e	0.15	DMIPS		0.25	
Nios II -f	1.13	DMIPS		1.60	200
PIC16	0.25				
PIC18				0.04	40
PIC24			0.72	1.86	40
PIC32				3.45	80
Super H-2				1.44	180
VAX780	1.00	DMIPS		1.50	
Z80	1.60		0.01	0.03	
	2X		1X	3X	