Small soft core uP Inventory ©2014 James Brakefield

under 500 LUTs with source code

_uP_cores_test folder	opencores name	status	author	style / clone	data size	inst size	FPGA	reporter	comments	LUTs ALM	LUT?	mults	blk ram	F max	tool ver	MIPS /clk	clks/ inst	KIPS /LUT	src code	# src files	top file	doc	tool chain	fltg pt	Hazd	max data	max inst	byte adrs	# inst	# reg	pipe len	start year	last revis	reference	note worthy	comments
Lutiac		custom	David Galloway, David	2 reg	16	NA	stratix-4	David Galloway		140	A	4		198		0.67	1.0	948	either								64	N	64	32	3		2010	Lutiac – Small Soft Proce	no inst RAM, instead microcode	no inst mem: small state machine, ~200 in
hive	hive	stable	Eric Wallin	4-8 stack	32	16	cyclone-3	Eric Wallin		1800	4	4	3	200		1.00	1.0	111	verilog			yes		N			N	40	10	8	2013	2014		4-8 symetrical stacks, eight threads via pipeline barrel	
hive	hive	stable	Eric Wallin	4-8 stack	32	16	cyclone-5	Eric Wallin		1877	4	4	3	226		1.00	1.0	120	verilog			yes		N			N	40	10	8	2013	2014		4-8 symetrical stacks, eight threads via pipeline barrel	
blue	16-bit CPU Blue	stable	Al Williams	accum	16	16	spartan-6-3	James Bra	missing file		6					0.67	1.0	####	verilog	16	top	web		N		4K	4K	N	16	2		2009	2010		Caxton Foster's Blue derivative	http://www.youtube.com/watch?v=dt4ze
lem1_9	lem1_9	stable	James Brakefield	accum	1	9	kintex-7	James Brakefield		40	6		1	357	14.5	0.04	1.0	357	vhdl	3	lem1_9n	yes	asm	N	Y	6	11	N	8	64	1	2003	2009		very small, 2 pipe stage is twice as fast	"logic emulation machine"
leros	Leros	stable	Martin Schoeberl	accum	16	16	cyclone-4-6	Martin Schoeberl		189	4		1	160		0.67	1.0	567	vhdl	6	leros "to	yes	yes	N		64K	64K			2	2	2008	2012	Leros: A Tiny Microcontr	short LUT inst ROM	256 word data RAM, PIC like
leros	Leros	stable	Martin Schoeberl	accum	16	16	spartan-3	Martin Schoeberl		188	4		1	129		0.67	1.0	460	vhdl	6	leros "to	yes	yes	N		64K	64K			2	2	2008	2012	Leros: A Tiny Microcontr	short LUT inst ROM	256 word data RAM, PIC like
leros	Leros	stable	Martin Schoeberl	accum	16	16	spartan-6	Martin Schoeberl		112	6		1	182	14.7	0.67	1.0	1089	vhdl	6	leros "to	yes	yes	N		64K	64K			2	2	2008	2012	Leros: A Tiny Microcontr	short LUT inst ROM	256 word data RAM, PIC like
leros	Leros	stable	Martin Schoeberl	accum	16	16	cyclone-4-6	James Brakefield		132	4		1	199	13.1	0.67	1.0	1010	vhdl	6	leros "to	yes	yes	N		64K	64K			2	2	2008	2012	Leros: A Tiny Microcontr	short LUT inst ROM	256 word data RAM, PIC like
leros	Leros	stable	Martin Schoeberl	accum	16	16	spartan-3-5	James Bra	probably s	116	4		1	155	14.7	0.67	1.0	898	vhdl	6	leros "to	yes	yes	N		64K	64K			2	2	2008	2012	Leros: A Tiny Microcontr	short LUT inst ROM	256 word data RAM, PIC like
leros	Leros	stable	Martin Schoeberl	accum	16	16	spartan-6	James Bra	probably s	66	6		1	222	14.7	0.67	1.0	2257	vhdl	6	leros "to	yes	yes	N		64K	64K			2	2	2008	2012	Leros: A Tiny Microcontr	short LUT inst ROM	256 word data RAM, PIC like
leros	Leros	stable	Martin Schoeberl	accum	16	16	kintex-7-3	James Bra	adjusted to	115	6		1	277	14.7	0.67	1.0	1614	vhdl	6	leros "to	yes	yes	N		64K	64K			2	2	2008	2012	Leros: A Tiny Microcontr	short LUT inst ROM	256 word data RAM, PIC like
mcpu	MCPU A minima	stable	Tim Boscke	accum	8	8	spartan-6-3	James Brakefield		41	6			384	14.7	0.17	1.0	1592	vhdl	1	tb02cpu	yes	asm	N		64	64	Y	4			2007	2014		fits into 32 macrocell CPLD	reduced MIPS/clk due to only 4 inst
micro16b		beta	John Kent	accum	16	16	kintex-7	Xilinx		205	6			434	14.7	0.33	2.0	349	vhdl	1	u16bcpu	yes	asm	N	N	64K	4K	Y	8			2002	2008	members.optushome.co	very limited inst set	MIPS/clk adj'd, 2 clks/inst
popcorn		stable	Jeung Joon Lee	accum	8	8x	spartan-6-3	James Brakefield		268	6			171	14.7	0.33	1.0	211	verilog	4	pc	yes		N		64K	64K	Y	43			2000			small 8 bit uP	
tisc	Tiny Instruction	beta	Vincent Crabtree	accum	8	8x	spartan-6-3	James Brakefield		198	6			60	14.7	0.33	1.0	100	vhdl	1	TISC			N		256	1K	Y		2		2009	2009		minimal accumulator machine	
usimplez	MicroSimplez	stable	Pablo Salvadeo etal	accum	12	12	stratix-2	Pablo Salvadeo		48	4			134	9.1	0.17	1.0	476	vhdl	3	usimplez_cpu			N		512	512		8			2011			von Neuman arch, Simplez processor	MIPS/Mhz reduced due to few inst
c16	16 Bit Microcont	stable	Jsauermann	C	16	8x	spartan-3-5	James Brakefield		1850	4		16	57	14.7	0.33	1.0	10	vhdl	22	Board_c	min	C,asm	N		64K	64K	Y		5		2003	2012		8080 derivative, optional UART, 8-bit memory port	
tiny8	tiny8	mature	Ulrich Riedel	CISC	8x	8x											1.0		AHDL					asm	N	64K	64K	Y				2002	2009		registers in RAM like TMS9900, uses Altera AHDL, megafunctions & schematic entry	
xproz		stable	Herbert Kleebauer	CISC	16	16x											1.0		schematic			yes	asm	N		64K	64K					1995			documentation in German	
ensilica		proprieta	ensilica.com	eSi-1600	16		virtex-5	ensilica		1100	6			160		0.67	1.0	97	not avail			yes	yes	N		64K	64K			16				www.ensilica.com	verilog source included with license	10 addressing modes
ensilica		proprieta	ensilica.com	eSi-3200	32		stratix-4	ensilica		1800	A			200		1.00	1.0	111	not avail			yes	yes			4G	4G			16	5			www.ensilica.com	verilog source included with license	10 addressing modes
b16		stable	Bernd Paysan	forth	16	5	spartan-6-3	James Brakefield		554	6			134		0.67	1.0	162	verilog	1	b16	yes	yes	N								2002	2011	bernd-paysan.de/b16.ht	two versions: one/15 source files, derived from c18	
dfp	dfp	stable	Ron Chapman	forth	X	Y	spartan-6-3	James Brakefield		334	6			112	14.7	0.33	1.0	111	vhdl	25	top	yes										2003	2009		8-bitter, generates a custom VHDL stack machine, compiler is in Forth	
J1		stable	James Bowman	forth	16	16	spartan-6	James Brakefield		333	6		1	117	14.7	0.80	1.0	280	vhdl	1	j1	yes	forth	N		64K	64K		16		2	2006	2010	excamera.com/sphinx/fp	uCode inst, dual port block RAM	32 deep data & return stacks
J1		stable	James Bowman	forth	16	16	kintex-7-3	James Brakefield		387	6		4	133	14.7	0.80	1.0	275	verilog	1	j1	yes	forth	N		64K	64K		16		2	2006	2010	excamera.com/sphinx/fp	uCode inst, dual port block RAM	32 deep data & return stacks
J1		stable	James Bowman	forth	16	16	kintex-7-3	James Bra	syntax errors		6				14.7	0.80	1.0	####	vhdl	1	j1	yes	forth	N		64K	64K		16		2	2006	2010	excamera.com/sphinx/fp	uCode inst, dual port block RAM	32 deep data & return stacks
jop	JOP a Java Optim	stable	Martin Schoeberl etal	forth	16	16	cyclone-1	Martin Schoeberl		2000	4			100	10	0.67	1.0	34	vhdl	11	core	yes	yes	N		256K	256K					2004	2014		opencores download is empty	https://github.com/jop-devel/jop
microcore		beta	Klaus Schleisiek	forth	32	8	spartan-6-3	James Brakefield		591	6		1	71	14.7	1.00	1.0	120	vhdl	10	core	yes	asm	N		2M	512K					2004			good documentation	
myforthproce	FORTH processo	stable	Gerhard Hohner	forth	32		spartan-3	James Bra	xilinx primitives n		4				14.7	1.00	1.0	####	vhdl	51	mycpu	yes	yes	Y								2012	2012		DPANS'94 32-bit Forth, masters thesis, four variants	
nige_machine		stable	Andrew Read	forth	32	8			unable to find files								1.0		vhdl	29	CPU	yes	yes	N		16M	16M		512	512			2014		standalone Forth system	
ssbcc	Smal Stack Base	stable	Rodney Sinclair	forth	8	9			syntax errors								1.0		verilog	3	core	yes	asm	N				Y				2012	2014		Python program generates the Verilog	
zpu	ZPU the worlds s	stable	Oyvind Harboe	forth	32	8	spartan-6	Oyvind Harboe		1259	6			135		0.10	1.0	11	vhdl	23	zpu_core	yes	yes	N		4G	4G	Y	37			2008	2009	www.zylin.com	zpu4: 16 & 32 bit versions, code size 80% of ARM (thumb), low MIPs/MHz	
zpu	ZPU the worlds s	stable	Oyvind Harboe	forth	32	8	spartan-3	Oyvind Harboe		440	4			85		0.05	1.0	10	vhdl	23	zpu_core	yes	yes	N		4G	4G	Y	37			2008	2009	www.zylin.com	zpu4: 16 & 32 bit versions, code size 80% of ARM (thumb), low MIPs/MHz	
8bit_chapman		beta	Rob Chapman, Steven	forth	8	8	kintex-7-3	James Bra	syntax errors		6				14.7	0.33	1.0	####	vhdl	10	top	yes		N		256	256					1998			course work	
cpu16		beta	C. H. Ting	forth	16	5	kintex-7-3	James Bra	case const	367	6			355	14.7	0.67	1.0	648	vhdl	1	cpu16	yes	asm	N		64K	64K					2000			part of eForth?	
dataflow_chapman		alpha	Rob Chapman, Steven	forth			kintex-7-3	James Bra	file WebCase repo		6				14.7	0.33	1.0	####	vhdl	27	DataFlov	yes		N		256	256					2003			course work	
msl16		beta	Philip Leong, Tsang, Le	forth	16	4	kintex-7-3	James Brakefield		303	6			256	14.7	0.67	1.0	566	vhdl	13	cpu	yes	asm	N		256						2001			CPLD prototype	
p16		alpha	Don Golding	forth	16	5	kintex-7-3	James Bra	bad syntax		6				14.7	0.67	1.0	####	vhdl	1	p16			N		64K	64K					2000				
x32		stable	Sijmen Woutersen	forth	32	8	kintex-7-3	James Bra	missing defines		6				14.7	1.00	1.0	####	vhdl	32	core	yes	yes	N		4G	4G	Y				2006	2007		MS thesis, byte code, needs caches	
theia_gpu	Theia: ray graph	beta	Diego Valverde	GPU													1.0		verilog	32	Theia	yes	asm	N						12		2011	2012		multi-core, 3D rendering & shader	
dragonfly		beta	LEOX team	MISC	16	16	kintex-7-3	James Brakefield		788	6			164	14.7	0.67	1.0	139	vhdl	6	dgf_core	yes		N		256	2K					2001		www.leox.org	unusual, uses FIFOs	
altor32	AltOr32	stable	Ultra Embedded	OpenRISC	32	32											1.0		verilog	19	altor32		yes	N		4G	4G	Y				2012	2014	OpenRISC 1000	simplified OpenRISC 1000	
minsoc	minsoc	stable	Raul Fajardo etal	OpenRISC	32	32	kintex-7-3	James Brakefield		4945	6	4	8	107	14.7	1.00	1.0	22	verilog	88	or1200_	yes	yes	Y	M	4G	4G	Y		32		2009	2013	www.minsoc.com	minimal OR1200, vendor neutral, has caches	
or1200_hp	OpenRisc 1200 H	stable	Strauch Tobias	OpenRISC	32	32	kintex-7-3	James Bra	1 slot barrel		6				14.7	1.00	1.0	####	verilog	39	or1200_	yes	yes	Y		4G	4G	Y		32		2010	2013		original version of OR1200	
or1200_hp	OpenRisc 1200 H	stable	Strauch Tobias	OpenRISC	32	32	kintex-7-3	James Bra	2 slot barrel	went	6				14.7	1.00	1.0	####	verilog	39	or1200_	yes	yes	Y		4G	4G	Y		32		2010	2013		2 slot barrel version of OR1200	
or1200_hp	OpenRisc 1200 H	stable	Strauch Tobias	OpenRISC	32	32	kintex-7-3	James Bra	3 slot barrel		6				14.7	1.00	1.0	####	verilog	39	or1200_	yes	yes	Y		4G	4G	Y		32		2010	2013		3 slot barrel version of OR1200	
or1200_hp	OpenRisc 1200 H	stable	Strauch Tobias	OpenRISC	32	32	kintex-7-3	James Bra	4 slot barrel		6				14.7	1.00	1.0	####	verilog	39	or1200_	yes	yes	Y		4G	4G	Y		32		2010	2013		4 slot barrel version of OR1200	
or1k	OpenRISC	stable	Adam Edvardsson etal	OpenRISC	32	32											1.0		verilog				yes	yes	N		4G	4G	Y		32		2001	2014		extensive documentation, source code elusive	
octavo		beta	Charles LaForest	reg	16	16	stratix-4	Charles LaForest		500	A	1		550		0.67	1.0	737	verilog	18	Octavo	yes	asm	N						14	16	10		2012	Octavo: an FPGA-Centric	8 core barrel, adjustable data width	~= performance across word sizes, no call/
alwcpu	Alwcpu	alpha	Andreas Hilvarsson	RISC	16	16	kintex-7-3	James Brakefield		298	6			237	14.7	0.67	1.0	533	vhdl	7	top	some		N		64K	64K	Y		16		2009	2009		400 LUTs	
atlas_core	Atlas Processor (	beta	Stephan Nolting	RISC	16	16	arria-2	James Brakefield		906	A	2	2	138	14.7	0.80	1.0	122	vhdl	13	ATLAS_C	yes	asm	N		4G	4G	N	80	8		2013	2013		ARM thumb like inst set, also X2 version	both MMU and non-MMU versions
atlas_core	Atlas Processor (	beta	Stephan Nolting	RISC	16	16	spartan-6	James Brakefield		677	6	1	1	103	14.7	0.80	1.0	122	vhdl	13	ATLAS_C	yes	asm	N		4G	4G	N	80	8		2013	2013		ARM thumb like inst set, also X2 version	both MMU and non-MMU versions
atlas_core	Atlas Processor (	beta	Stephan Nolting	RISC	16	16	kintex-7-3	James Brakefield		655	6	1	1	192	14.7	0.80	1.0	235	vhdl	13	ATLAS_C	yes	asm	N		4G	4G	N	80	8		2013	2013		ARM thumb like inst set, also X2 version	both MMU and non-MMU versions
atlas_x2	Atlas Processor (	beta	Stephan Nolting	RISC	16	16	kintex-7-3	James Bra	missing defines		6	1	1		14.7	0.80	1.0	####	vhdl	13	ATLAS_X	yes	asm	N		4G	4G	N	80	8		2013	2013		ARM thumb like inst set	has MMU & full SOC features
ba22		proprieta	CAST Inc	RISC	32	16x	spartan-6	CAST Inc		1800	6		32	72		1.00	1.0	40	not avail							4G	4G			32				www.cast-inc.com		
erp	Educational RISC	stable	Shahzadjk	RISC	8	16	kintex-7-3	James Bra	syntax errors		6				14.7	0.33	1.0	####	verilog	1	ERPveril	yes							15	6		2004	2009		two report PDFs & one Verilog file	
gumnut		stable	Peter Ashenden	RISC	8	18	kintex-7-3	James Bra	missing file		6				14.7	0.33	1.0	####	vhdl	20	gumnut	yes		N		256	4K	Y		8		2007			see Digital Design: An Embedded Systems Approach Using VHDL	
jane_nn		stable	Suresh Devanathan	RISC	4	8	kintex-7-3	James Brakefield		723	6			178	14.7	0.33	1.0	81	vhdl	3	Processc	yes							27	16		2002			neural network microprocessor, specialized registers	
jpu16		stable	Joksan Alvarado	RISC	16	26	kintex-7-3	James Bra	missing defines		6				14.7	0.67	1.0	####	vhdl	9	JPU16	yes	asm	N		64K	64K			16		2012			32 deep call stack, 8 addressing modes	
latticemicro32		stable	Yann Siommeau, Micha	RISC	32	32	spartan-6	James Brakefield		2093	6	3	15	85	14.7	0.80	1.0	32	verilog	24	lm32_cp	yes	yes	N		4G	4G	Y		32		2006	2012	en.wikipedia.org/wiki/La	optional data & inst caches	
latticemicro32		stable	Yann Siommeau, Micha	RISC	32	32	kintex-7-3	James Brakefield		2292	6	3	8	155	14.7	0.80	1.0	54	verilog	24	lm32_cp	yes	yes	N		4G	4G	Y		32		2006	2012	en.wikipedia.org/wiki/La	optional data & inst caches	
latticemicro8		stable	Lattice Semiconductor	RISC	8	18	LFE2	Lattice Semiconducto		265	4			104			1.0		vhdl	10	isp8_cor	yes	yes	N		256	4K	Y		32		2005	2010	en.wikipedia.org/wiki/La	16 deep call stack, four configurations	
natalius_8bit	Natalius 8 bit RIS	beta	Fabio Guzman	RISC	8	16	spartan-3-4	James Brakefield		418	4		4	64	14.7	0.33	1.0	50	verilog	12	natalius_	yes	asm	N		32	2K	Y		8		2012	2012		return stack & register file	
natalius_8bit	Natalius 8 bit RIS	beta	Fabio Guzman	RISC	8	16	kintex-7-3	James Brakefield		232	6		1	175	14.7	0.33	1.0	249	verilog	12	natalius_	yes	asm	N		32	2K	Y		8		2012	2012		return stack & register file	
open8_urisc	Open8 uRISC	stable	Kirk Hays, Jshamlet	RISC	8	8	kintex-7-3	James Brakefield		691	6	1		263	14.7	0.33	1.0	126	VHDL	9	Open8	yes	yes	N		64K	64K	Y		8		2006	2013		accum & 8 regs, clone of Vautomation uRISC processor, in use	
rise	RISE Microproce	beta	Jlechner etal	RISC	16	16	kintex-7-3	James Bra	missing blox boxe		6	1			14.7	0.67	1.0	####	vhdl	26	rise	yes	asm	N		64K	64K			16	5	2006	2010	en.wikiversity.org/wiki/C	ARM style register usage	
sayeh_proces	SAYEH educatior	stable	Alireza Haghdoost, Arm	RISC	16	16	kintex-7-3	James Brakefield		479	6	1		164	14.7	0.67	1.0	230	verilog	13	Sayeh	yes		N		64K	64K			32		2008	2009	haghdoost.persiangig.co	simple RISC	
scarts	Scarts Processor	beta	Jlechner, Martin Walte	RISC	16	16	kintex-7-3	James Bra	missing signal dec		6				14.7	0.67	1.0	####	vhdl	18	scarts		yes	N		64K	64K		122	16	4	2011	2012		GCC compiler	
sxp	SXP (Simple eXte	beta	Sam Gladstone etal	RISC	32	32			too many los										verilog		sxp			N		4G	4G			32		2001	2009		basic RISC	too many los
tiny64	Tiny64	stable	Ulrich Riedel	RISC	64		kintex-7-3	James Bra	bit length mismat		6				14.7	1.00	1.0	####	vhdl	7	TinyX		asm	N		64K	64K		16	8		2004	2009		word size configurable from 32 to 64	
xr16		stable	Jan Gray	RISC	16	16	kintex-7-3	James Brakefield		371	6			7	14.7	0.67	1.0	13	verilog	12	xsoc	yes		N		64K	64K			16		1999	2001		handcrafted FPGA layout & instruction set	
diogenes	diogenes	beta	Fekknhifer	RISC	16	16	kintex-7-3	James Bra	missing file "types		6				14.7	0.67	1.0	####	vhdl	11	cpu						1K					2008	2009			
eco32	SOC:ECO32	alpha	Hellwing Geisse	RISC	32	32	cyclone-4-6	James Brakefield		5153	4			84	13.1	1.00	1.0	16	verilog	23	cpu	yes	yes	N		512M	256M	Y	61	32		2003	2014		MIPS like, MMU	
eco32	SOC:ECO32	alpha	Hellwing Geisse	RISC	32	32	arria-2	James Brakefield		2711	A			129	13.1	1.00	1.0	48	verilog	23	cpu	yes	yes	N		512M	256M	Y	61	32		2003	2014		MIPS like, MMU	

eco32	SOC:ECO32	alpha	Hellwing Geisse	RISC	32	32	spartan-3-5	James Brakefield	3034	4		2	55	14.7	1.00	1.0	18	verilog	23	cpu	yes	yes	N		512M	256M	Y	61	32		2003	2014		MIPS like, MMU	
eco32	SOC:ECO32	alpha	Hellwing Geisse	RISC	32	32	spartan-6-3	James Brakefield	2271	6		1	92	14.7	1.00	1.0	41	verilog	23	cpu	yes	yes	N		512M	256M	Y	61	32		2003	2014		MIPS like, MMU	
eco32	SOC:ECO32	alpha	Hellwing Geisse	RISC	32	32	kintex-7-3	James Brakefield	2210	6		1	160	14.7	1.00	1.0	72	verilog	23	cpu	yes	yes	N		512M	256M	Y	61	32		2003	2014		MIPS like, MMU	
eight_bit_uc		stable	Synplicity	RISC	8	12	kintex-7-3	James Bra	signal/variable mi	6				14.7	0.67	1.0	####	vhdl	10	eight_bit_uc						2K	Y		32						part of Amplify documentation	
hicovec	HiCoVec a config	beta	Harald Manske, Gundo	RISC	32	32	kintex-7-3	James Bra	compiler errors	6				14.7	1.00	1.0	####	vhdl	28	cpu	yes	asm	N				Y				2008	2010		hybrid scalar & vector processor	
hpc-16	HPC-16	beta	Umair Siddiqui	RISC	16	16	kintex-7-3	James Brakefield	875	6			136	14.7	0.67	1.0	104	vhdl	20	cpu	yes	asm	N		64K	64K			16		2005	2009			
jam		stable	Johan Thelin etal	RISC	64	32	kintex-7-3	James Brakefield	1369	6			143	14.7	1.00	1.0	104	vhdl	17	cpu	yes		N		128K	128K			32	5	2002				
manik		stable	Sandeeo Dytta	RISC	32	32	arria-2	James Bra	vcomponents mis	A				13.1	0.33	1.0	####	vhdl	45	manik2t	yes	yes	N		4K	4K	Y		16		2002	2006	www.niktech.com/	optional data & inst caches	
marca	McAdam's RISC	stable	Wolfgang Puffitsch	RISC	16	16	kintex-7-3	James Bra	syntax errors	6				14.7	0.67	1.0	####	vhdl	40	marca	yes		N		8K	16K		75	16	4	2007	2009			
raptor64	Raptor64	planning	Robert Finch	RISC	64	32	kintex-7-3	James Bra	missing port nam	6				14.7	1.50	1.0	####	verilog	48	Raptor6	yes	yes	Y		2<<64	2<<64	Y		32		2012	2013		8-16-32-64 bit data, cache, MMU, hyper-threaded version also	
risc0		beta	Niklaus Wirth	RISC	32	32	kintex-7-3	James Brakefield	1186	6	4	6	110	14.7	0.67	1.0	62	verilog	8	RISC0	yes	yes	N		4G	4G					2011			minimalist Wirth, education tool	
risc5		beta	Niklaus Wirth	RISC	32	32	kintex-7-3	James Bra	missing prom.me	6	4	6		14.7	1.00	1.0	####	verilog	17	RISC5To	yes	yes	Y		4G	4G					2013			minimalist Wirth, part of Project Oberon 2013	
yasep		alpha	Yann Guidon	RISC	16	32	kintex-7-3	James Bra	syntax errors	6				14.7	1.00	1.0	####	vhdl		microYA	yes	asm	N			2K			16		2008	2014	www.yaesp.org	Java generated VHDL, revisions ongoing	funky web site
lemberg		stable	Wolfgang Puffitsch	VLIW	32	32	cyclone-4-6	James Bra	fitter failed	4				13.1	1.00	1.0	####	vhdl	32	core	yes	yes	Y		4G	2M	Y		32	4	2011		www2.imm.dtu.dk/~wo	upto 4 inst/clock	
bobcat		beta	Stan Drey		16	24	kintex-7-3	James Brakefield	1622	6	1		107	14.7	0.67	1.0	44	vhdl							64K	64K					1998			appears to be a DSP	
cowgirl	Cowgirl	beta	Thebeekeeper		16	16	kintex-7-3	James Bra	empty design	6				14.7	0.67	1.0	####	vhdl	14	cowgirl						64K					2006	2009			
vtach	VTACH Bell Labs	mature	Al Williams		13	12	spartan-3-4	James Brakefield	557	4			71	14.7	0.50	1.0	64	verilog	16	vtach			N		256	256	Y				2913	2013		ISE project only, BCD arithmetic	
vtach	VTACH Bell Labs	mature	Al Williams		13	12	kintex-7-3	James Bra	xilinx core proble	6				14.7	0.50	1.0	####	verilog	16	vtach			N		256	256	Y				2913	2013		ISE project only, BCD arithmetic	

58 # usable(beta, stable or mature): "A"(clones) & "W"(originals # reg bits

35 "B" or "X" of limited interest

adr locations

Web page DMIPS per clock cycle per core en.wikiped community.freescale.com/thread/60391

MIPS/MHz Pro-rating for data size:

1-bit	0.04
8-bit	0.33
16-bit	0.67
32-bit	1.00

Under the assumption that the core is capable of one instuction per clock

Silicon Area equivalents

LUTS/DSP48	16:1
LUTS/Block RAM	32:1

Following has DMIPS per clock for many microprocessors

http://en.wikipedia.org/wiki/Instructions_per_second

uP	MIPS			CoreMarks /MHz	MHz	
4004	0.10					
6502	0.50		0.02	0.06		
8051			0.08	0.24		
8080	0.17			0.25		
68K	0.10			0.15		
ARM Cortex A9	2.50	DMIPS		5.93	1000	
ARM Cortex M0	0.90	DMIPS		1.50	70	
ARM Cortex M3	1.25	DMIPS		2.92	25	
ARM7	0.90		0.74	2.04	600	
AVR	1.00		0.21	0.53	8	
AVR32				1.62	60	
BA21				2.44	400	
Coldfire				2.80	400	
Coldfire				0.77	150	Virtex-5
HCS08			0.04	0.12		
LEON3/Spartan-6				1.96	100	
MC6809	1.24		0.07	1.86		
MicroBlaze 3-stage	1.03			1.50		
MicroBlaze 5-stage	1.38			1.90	125	
MIPS32	1.51			2.28		
MSP430			0.40	1.20		
MSP430				1.10	25	
Nios II	0.64	DMIPS		0.93	200	
Nios II -e	0.15	DMIPS		0.25		
Nios II -f	1.13	DMIPS		1.60	200	
PIC16	0.25					
PIC18				0.04	40	
PIC24			0.72	1.86	40	
PIC32				3.45	80	
Super H-2				1.44	180	
VAX780	1.00	DMIPS		1.50		
Z80	1.60		0.01	0.03		
	2X		1X	3X		

Column Titles	Details
"A"	A: 1st choice clone, B: 2nd choice clone, W: 1st choice original, X: 2nd choice original
"B"	currently unused and hidden
_uP_cores_test folder	if opencores design is their folder name, otherwise my folder name
opencores name	
status	ASIC, planning, alpha, beta, stable, mature, proprietary
author	First Name, Last Name
style / clone	part number or "forth", RISC, accumulator, etc
data size	data memory word size
inst size	instruction size
FPGA	FPGA family for compile, place, route & timing
reporter	First Name, Last Name
comments	compile, place, route & timing problems
LUTs ALM	4-LUT, 6-LUT, Altera ALM, Actel Tile
LUT?	total number of LUTs or ALMs used including route-thrus & otherwise unavailable
mults	total number of multipliers/DSPs used
blk RAM	total number of block RAMs used, does not include small and extra large Altera block RAMs, Xilinx half block RAM rounded up
Fmax	maximum primary clock speed from compile, place, route & timing run
tool ver	Altera, Xilinx, Lattice Semiconductor or MicroSemi tool version number
MIPS /clk	prorated DMIPS per clock, reduced for data word sizes under 32-bits, greater than one for multiple issue processors
clks/ inst	number of clocks per instruction, typically 1.0 for modern pipelined processors
KIPS /LUT	figure of merit, does not include effects of memory capacity, floating point or instruction set quality
src code	VHDL or Verilog or other
# src files	number of source files for compile, place, route & timing
top file	top file for compile, place, route & timing run
doc	is documentation provided
tool chain	is there a compiler or assembler provided or available
fltg pt	does the compile, place, route & timing run include floating point
Ha vd	separate instruction and data memory(s), there can be more than one data memory, M for MMU & caches
max data	maximum data address
max inst	maximum instruction address
byte adrs	is byte addressing provided
# inst	number of unique instructions, somewhat subjective
# reg	number of registers in register file
pipe len	number of pipeline stages
start year	year of first design activity
last revis	last year for revisions
reference	web address or generic information (for clones)
note worthy	anything special about the design
comments	catchall