Small soft core uP Inventory **©2014 James Brakefield**

Opencore and other soft core processors

_uP_cores_test folder	opencores name	status	author	style / clone	data size	inst size	FPGA	reporter	comment	LUTs ALM	LUT?	mults	blk ram	F max	tool ver	MIPS /clk	clks/ inst	KIPS /LUT	src code	# src files	top file	doc	tool chain	fltg pt	Ha vd	max data	max inst	byte adrs	# inst	# reg	pipe len	start year	last revis	reference	note worthy	comments
iDEA		proprietar	Cheah etal	RISC	16	32	virtex-6	Cheah		190	6	1	1	534		0.67	1.0	1883	not avail													2011	A Lean FPGA Soft Pro	uses DSP slice in barrel mode for ALU	by Xilinx, no source
leros	Leros	stable	Martin Schoeberl	accum	16	16	kintex-7-3	James	adjust	115	6		1	277	14.7	0.67	1.0	1614	vhdl	6	leros "top	yes	yes	N		64K	64K			2	2	2008	2012	Leros: A Tiny Microco	short LUT inst ROM	256 word data RAM, PIC like
mcpu	MCPU A minima	stable	Tim Boscke	accum	8	8	spartan-6-3	James Brakef		41	6			384	14.7	0.17	1.0	1592	vhdl	1	tb02cpu2	yes	asm	N		64	64	Y	4			2007	2014		fits into 32 macrocell CPLD	reduced MIPS/clk due to only 4 inst
risc_core_i	RISC_Core_I	planning	Manuel Imhof	RISC	16	16	kintex-7-3	James Brakef		349	6	1		717	14.7	0.67	1.0	1377	vhdl	13	CPU	yes	asm	N		1K	1K		8	4	2001	2009		Havard arch	dubious Fmax
leros	Leros	stable	Martin Schoeberl	accum	16	16	spartan-6	Martin Schoe		112	6		1	182	14.7	0.67	1.0	1089	vhdl	6	leros "top	yes	yes	N		64K	64K			2	2	2008	2012	Leros: A Tiny Microco	short LUT inst ROM	256 word data RAM, PIC like
leros	Leros	stable	Martin Schoeberl	accum	16	16	cyclone-4-6	James Brakef		132	4		1	199	13.1	0.67	1.0	1010	vhdl	6	leros "top	yes	yes	N		64K	64K			2	2	2008	2012	Leros: A Tiny Microco	short LUT inst ROM	256 word data RAM, PIC like
risc16f84	risc16f84	stable	John Clayton	PIC16	8	14	kintex-7-3	James Brakef		331	6			333	14.7	1.00	1.0	1007	verilog	1	risc16f84	yes	yes	N	Y	256	4K	Y				2002	2013	PIC16 data sheets	derived from CQPIC by Sumio Morioka	
Lutiac		custom	David Galloway, David	2 reg	16	NA	stratix-4	David Gallow		140	A	4		198		0.67	1.0	948	either							64	N	64	32	3		2010	Lutiac – Small Soft Pro	no inst RAM, instead microcode	no inst mem: small state machine, ~200 inst optimal
leros	Leros	stable	Martin Schoeberl	accum	16	16	spartan-3-5	James	proba	116	4		1	155	14.7	0.67	1.0	898	vhdl	6	leros "top	yes	yes	N		64K	64K			2	2	2008	2012	Leros: A Tiny Microco	short LUT inst ROM	256 word data RAM, PIC like
avr8	Reduced AVR Co	beta	Nick Kovach	AVR	8	16	kintex-7-3	James Brakef		174	6			418	14.7	0.33	1.0	792	verilog	1	rAVR	yes	yes	N		64K	64K	Y	17	4		2010	2010	AVR data sheets	not a full clone, doc is opencores page	
octavo		beta	Charles LaForest	reg	16	16	stratix-4	Charles LaFor		500	A	1		550		0.67	1.0	737	verilog	18	Octavo	yes	asm	N					14	16	10		2012	Octavo: an FPGA-Cent	8 core barrel, adjustable data width	~= performance across word sizes, no call/rtn inst
ourisc	16-bit Open uRIS	alpha	Joao Carlos		16	16	kintex-4	Joao Carlos		500	A	1		550		0.67	1.0	737	vhdl										26			2013	2013		very incomplete source code	
cpu16		beta	C. H. Ting	forth	16	5	kintex-7-3	James	case c	367	6			355	14.7	0.67	1.0	648	vhdl	1	cpu16	yes	asm	N		64K	64K					2000			part of eForth?	
ARM_Cortex_A9		ASIC	ARM	ARM a9	32	16	arria V	altera		4500	A			1050		2.50	1.0	583	asic				yes	yes	Y		4G	4G	Y	80	16	10		2012	altera data sheets	uses pro-rated LC area	dual issue, includes fltg-pt & MMU & caches
leros	Leros	stable	Martin Schoeberl	accum	16	16	cyclone-4-6	Martin Schoe		189	4		1	160		0.67	1.0	567	vhdl	6	leros "top	yes	yes	N		64K	64K			2	2	2008	2012	Leros: A Tiny Microco	short LUT inst ROM	256 word data RAM, PIC like
msl16		beta	Philip Leong, Tsang, Le	forth	16	4	kintex-7-3	James Brakef		303	6			256	14.7	0.67	1.0	566	vhdl	13	cpu	yes	asm	N		256						2001			CPLD prototype	
ARM_Cortex_A9		ASIC	ARM	ARM a9	32	16	zynq	xilinx		4500	6			1000		2.50	1.0	556	asic				yes	yes	Y		4G	4G	Y	80	16	10		2012	xilinx plan ahead: an A	uses pro-rated LC area	dual issue, includes fltg-pt & MMU & caches
alwcpu	Alwcpu	alpha	Andreas Hilvarsson	RISC	16	16	kintex-7-3	James Brakef		298	6			237	14.7	0.67	1.0	533	vhdl	7	top	some		N		64K	64K	Y		16		2009	2009		400 LUTs	
ARM_Cortex_A9		ASIC	ARM	ARM a9	32	16	cyclone V	altera		4500	A			925		2.50	1.0	514	asic				yes	yes	Y		4G	4G	Y	80	16	10		2012	altera data sheets	uses pro-rated LC area	dual issue, includes fltg-pt & MMU & caches
microblaze		proprieta	Xilinx	uBlaze	32	32	kintex-7	Xilinx		546	6		1	264		1.03	1.0	498	not avail				yes	yes	opt		32	32	Y	86	32	3	2002		www.xilinx.com/tools	area optimized	70 configuration options, MMU optional
usimplez	MicroSimplez	stable	Pablo Salvadeo etal	accum	12	12	stratix-2	Pablo Salvad		48	4			134	9.1	0.17	1.0	476	vhdl	3	usimplez_cpu			N		512	512		8			2011			von Neuman arch, Simplez processor	MIPS/Mhz reduced due to few inst
leros	Leros	stable	Martin Schoeberl	accum	16	16	spartan-3	Martin Schoe		188	4		1	129		0.67	1.0	460	vhdl	6	leros "top	yes	yes	N		64K	64K			2	2	2008	2012	Leros: A Tiny Microco	short LUT inst ROM	256 word data RAM, PIC like
microblaze		proprieta	Xilinx	uBlaze	32	32	kintex-7	Xilinx		1201	6		32	408		1.30	1.0	441	not avail			yes	yes	opt		32	32	Y	86	32	5	2002		www.xilinx.com/tools	performance optimized	70 configuration options, MMU optional
nios2		proprietar	Altera	Nios II	32	32	stratix-5	Altera		895	6			310		1.13	1.0	390	no source			yes	yes	opt		4G	4G	Y		32		2004		NIOS2 data sheets	fltg-pt, caches & MMU options	Nios II/f: fastest version
lem1_9	lem1_9	stable	James Brakefield	accum	1	9	kintex-7	James Brakef		40	6		1	357	14.5	0.04	1.0	357	vhdl	3	lem1_9m	yes	asm	N	Y	6	11	N	8	64	1	2003	2009		very small, 2 pipe stage is twice as fast	"logic emulation machine"
micro16b		beta	John Kent	accum	16	16	kintex-7	Xilinx		205	6			434	14.7	0.33	2.0	349	vhdl	1	u16bcpu	yes	asm	N	N	64K	4K	Y	8			2002	2008	members.optushome	very limited inst set	MIPS/clk adj'd, 2 clks/inst
picoblaze	picoblaze	stable	Ken Chapman	picoBlaze	8	18	spartan-3-4	James Brakef		178	4			182	14.7	0.33	1.0	338	vhdl	1	kcspm3	yes	asm	N		256	2K	Y				2003		picoblaze data sheets	2 clocks per inst	this is the original picoBlaze author
nios2		proprietar	Altera	Nios II	32	32	stratix-5	Altera		650	A			300		0.64	1.0	293	no source			yes	yes	opt		4G	4G	Y		32		2004		NIOS2 data sheets	fltg-pt, caches & MMU options	Nios II: balanced version
J1		stable	James Bowman	forth	16	16	spartan-6	James Brakef		333	6		1	117	14.7	0.80	1.0	280	vhdl	1	j1	yes	forth	N		64K	64K		16		2	2006	2010	excamera.com/sphinx	uCode inst, dual port block RAM	32 deep data & return stacks
Lutiac		custom	David Galloway, David	2 reg	16	NA	stratix-4	David Gallow		480	A	4		197		0.67	1.0	275	either						Y		128	N	64	32	3		2010	Lutiac – Small Soft Pro	no inst RAM, instead microcode	no inst mem: large state machine, ~200 inst optimal
J1		stable	James Bowman	forth	16	16	kintex-7-3	James Brakef		387	6		4	133	14.7	0.80	1.0	275	verilog	1	j1	yes	forth	N		64K	64K		16		2	2006	2010	excamera.com/sphinx	uCode inst, dual port block RAM	32 deep data & return stacks
light8080	Lightweight 8080	stable	Jose Ruiz, Moti Litoche	8080	8	8x	kintex-7-3	James Brakef		154	6		1	247	14.7	0.17	1.0	265	verilog	5	i80soc	yes	yes	N	N	64K	64K	Y				2007	2012	8080 data sheets	targeted to area, includes UART, interrupt ctlr & RAM	
light8080	Lightweight 8080	stable	Jose Ruiz, Moti Litoche	8080	8	8x	kintex-7-3	James Brakef		154	6		1	247	14.7	0.17	1.0	265	verilog	5	light8080	yes	yes	N	N	64K	64K	Y				2007	2012	8080 data sheets	targeted to area, bare core	
lem16_18m		alpha	James Brakefield	accum	16	18	spartan-6-3	James	incom	471	6		1	178	14.7	0.67	1.0	253	vhdl	2	lem16_18	yes		N	Y	16	16	Y	100	3	1	2009	2013		LUT instructions, bit fields to/from data memory	
natalius_8bit	Natalius 8 bit RIS	beta	Fabio Guzman	RISC	8	16	kintex-7-3	James Brakef		232	6		1	175	14.7	0.33	1.0	249	verilog	12	natalius_	yes	asm	N		32	2K	Y		8		2012	2012		return stack & register file	
atlas_core	Atlas Processor (	beta	Stephan Nolting	RISC	16	16	kintex-7-3	James Brakef		655	6	1	1	192	14.7	0.80	1.0	235	vhdl	13	ATLAS_C(	yes	asm	N		4G	4G	N	80	8		2013	2013		ARM thumb like inst set, also X2 versio	both MMU and non-MMU versions
nios2		proprietar	Altera	Nios II	32	32	arria-5	Altera		1355	A			280		1.13	1.0	232	no source			yes	yes	opt		4G	4G	Y		32		2004		NIOS2 data sheets	fltg-pt, caches & MMU options	Nios II/f: fastest version
sayeh_proces	SAYEH education	stable	Alireza Haghdoost, Arm	RISC	16	16	kintex-7-3	James Brakef		479	6	1		164	14.7	0.67	1.0	230	verilog	13	Sayeh	yes		N		64K	64K			32		2008	2009	haghdoost.persiangig	simple RISC	
eric5		proprieta	enter-electronics.com	forth	9	8	cyclone-4-6	enter-electro		110	4	opt		60		0.42	1.0	229	not avail							512	1K		3-4			2007			25 MIPS: ERIC5xs, ERIC5Q	
pacoBlaze		mature	Pablo Kocik	picoBlaze	8	18	spartan-3	Pablo Kocik		177	4		1	117		0.33	1.0	218	verilog	18	pacoblaze	yes	asm			8	11	Y	57		2	2006		bleyer.org/pacoblaze	3 versions, behavioral coding	
popcorn		stable	Jeung Joon Lee	accum	8	8x	spartan-6-3	James Brakef		268	6			171	14.7	0.33	1.0	211	verilog	4	pc	yes		N		64K	64K	Y	43			2000			small 8 bit uP	
light8080	Lightweight 8080	stable	Jose Ruiz, Moti Litoche	8080	8	8x	spartan-6	James Brakef		148	6		3	172	14.7	0.17	1.0	192	verilog	5	light8080	yes	yes	N	N	64K	64K	Y				2007	2012	8080 data sheets	targeted to area, bare core	
pdp8verilog		stable	Brad Parker	PDP8	12	12	kintex-7-3	James Brakef		505	6			366	14.7	0.50	2.0	181	verilog	18	pdp8	yes	yes	N	N	32K	32K			8		2005	2010	PDP8 data sheets	boots & runs TSS/8 & Basic	www.heeltoe.com/download/pdp8/README.html
nios2		proprietar	Altera	Nios II	32	32	cyclone-5	Altera		1050	A			160		1.13	1.0	171	no source			yes	yes	opt		4G	4G	Y		32		2004		NIOS2 data sheets	fltg-pt, caches & MMU options	Nios II/f: fastest version
aeMB	aeMB	beta	Shawn Tan	uBlaze	32	32	kintex-7-3	James Brakef		1018	6	3		131	14.7	1.30	1.0	167	verilog	29	aeMB_co	yes	yes	N		4G	4G	Y				2004	2009	xilinx documentation	not 100% compatable	
t65	T65 CPU	stable	Daniel Wallner	6502	8	8x	kintex-7-3	James Brakef		575	6			291	14.7	0.33	1.0	167	vhdl	7	T65	yes	yes	N	N	64K	64K	Y				2002	2010	6502 data sheets	6502, 65C02 & 65C816; wide use	
b16		stable	Bernd Paysan	forth	16	5	spartan-6-3	James Brakef		554	6			134		0.67	1.0	162	verilog	1	b16	yes	yes	N								2002	2011	bernd-paysan.de/b16	two versions: one/15 source files, derived from c18	
light8080	Lightweight 8080	stable	Jose Ruiz, Moti Litoche	8080	8	8x	spartan-6	James Brakef		150	6		3	142	14.7	0.17	1.0	156	vhdl	5	light8080	yes	yes	N	N	64K	64K	Y				2007	2012	8080 data sheets	targeted to area, bare core	
nios2		proprietar	Altera	Nios II	32	32	arria-5	Altera		1045	A			250		0.64	1.0	152	no source			yes	yes	opt		4G	4G	Y		32		2004		NIOS2 data sheets	fltg-pt, caches & MMU options	Nios II: balanced version
nios2		proprietar	Altera	Nios II	32	32	arria-2	Altera		1355	A			170		1.13	1.0	141	no source			yes	yes	opt		4G	4G	Y		32		2004		NIOS2 data sheets	fltg-pt, caches & MMU options	Nios II/f: fastest version
dragonfly		beta	LEOX team	MISC	16	16	kintex-7-3	James Brakef		788	6			164	14.7	0.67	1.0	139	vhdl	6	dgf_core	yes		N		256	2K					2001		www.leox.org	unusual, uses FIFOs	
free_risc8		stable	Thomas Coonan	PIC16	8	14	kintex-7-3	James Brakef		355	6			142	14.7	0.33	1.0	132	verilog	8	cpu	yes	yes	N		256	4K	Y				2002	2011	PIC16 data sheets		
ae18	ae18	beta	Shawn Tan	PIC18	16	24	arria-2	James Brakef		1084	A	1		207	13.1	0.67	1.0	128	verilog	1	ae18_core		yes	N	Y	4K	1M					2003	2009	PIC18 data sheets	not 100% compatable	negative edge reset "clock"
open8_urisc	Open8 uRISC	stable	Kirk Hays, Jshamlet	RISC	8	8	kintex-7-3	James Brakef		691	6	1		263	14.7	0.33	1.0	126	VHDL	9	Open8	yes	yes	N		64K	64K	Y		8		2006	2013		accum & 8 regs, clone of Vautomation u	RISC processor, in use
atlas_core	Atlas Processor (	beta	Stephan Nolting	RISC	16	16	spartan-6	James Brakef		677	6	1	1	103	14.7	0.80	1.0	122	vhdl	13	ATLAS_C(	yes	asm	N		4G	4G	N	80	8		2013	2013		ARM thumb like inst set, also X2 versio	both MMU and non-MMU versions
atlas_core	Atlas Processor (	beta	Stephan Nolting	RISC	16	16	arria-2	James Brakef		906	A	2	2	138	14.7	0.80	1.0	122	vhdl	13	ATLAS_C(	yes	asm	N		4G	4G	N	80	8		2013	2013		ARM thumb like inst set, also X2 versio	both MMU and non-MMU versions
hive	hive	stable	Eric Wallin	4-8 stack	32	16	cyclone-5	Eric Wallin		1877	4	4	3	226		1.00	1.0	120	verilog				yes	N				N	40	10	8	2013	2014		4-8 symetrical stacks, eight threads via pipeline barrel	
microcore		beta	Klaus Schleisiek	forth	32	8	spartan-6-3	James Brakef		591	6		1	71	14.7	1.00	1.0	120	vhdl	10	core	yes	asm	N		2M	512K					2004			good documentation	
mips789	mips789	stable	Li Wei	MIPS	32	32	kintex-7-3	James Brakef		1432	6		1	171	14.7	1.00	1.0	119	verilog	10	mips_cor	yes	yes	N		4G	4G	Y		32		2007	2009	MIPS data sheets		
nios2		proprietar	Altera	Nios II	32	32	stratix-5	Altera		445	A			340		0.15	1.0	115	no source			yes	yes	N		4G	4G	Y		32		2004		NIOS2 data sheets	serial arithmetic	Nios II/e: minimum LUTs version
nios2		proprietar	Altera	Nios II	32	32	cyclone-5	Altera		785	A			140		0.64	1.0	113	no source			yes	yes	opt		4G	4G	Y		32		2004		NIOS2 data sheets	fltg-pt, caches & MMU options	Nios II: balanced version
ensilica		proprieta	ensilica.com	eSi-3200	32		stratix-4	ensilica		1800	A			200		1.00	1.0	111	not avail				yes	yes			4G	4G			16	5			www.ensilica.com	verilog source included with license	10 addressing modes
hive	hive	stable	Eric Wallin	4-8 stack	32	16	cyclone-3	Eric Wallin		1800	4	4	3	200		1.00	1.0	111	verilog				yes		N				N	40	10	8	2013	2014		4-8 symetrical stacks, eight threads via pipeline barrel	
dfp	dfp	stable	Ron Chapman	forth	X	Y	spartan-6-3	James Brakef		334	6			112	14.7	0.33	1.0	111	vhdl	25	top	yes										2003	2009		8-bitter, generates a custom VHDL stack machine, compiler is in Forth	
ion	Ion MIPS compa	mature	Jose Ruiz	MIPS	32	32	kintex-7-3	James Brakef		1533	6			163	14.7	1.00	1.0	106	vhdl	12	mips_soc	yes	yes	N		4G	4G	Y		32		2011	2014		MIPS R3000 clone	
jam		stable	Johan Thelin etal	RISC	64	32	kintex-7-3	James Brakef		1369	6			143	14.7	1.00	1.0	104	vhdl	17	cpu	yes		N		128K	128K			32	5	2002				
hpc-16	HPC-16	beta	Umair Siddiqui	RISC	16	16	kintex-7-3	James Brakef		875	6			136	14.7	0.67	1.0	104	vhdl	20	cpu	yes	asm	N		64K	64K			16		2005	2009			
nios2		proprietar	Altera	Nios II	32	32	arria-2	Altera		1045	A			170		0.64	1.0	103	no source			yes	yes	opt		4G	4G	Y		32		2004		NIOS2 data sheets	fltg-pt, caches & MMU options	Nios II: balanced version
tv80	TV80	mature	Guy Hutchison, Howard	Z80	8	8x	kintex-7-3	James Brakef		1207	6			182	14.7	0.67	1.0	101	verilog	6	tv80n	yes	yes	N	N	64K	64K	Y				2004	2012	z80 data sheets	derived from Daniel Wallner's T80, ASIC	implementations
tisc	Tiny Instruction	beta	Vincent Crabtree	accum	8	8x	spartan-6-3	James Brakef		198	6			60	14.7	0.33	1.0	100	vhdl	1	TISC			N		256	1K	Y		2		2009	2009		minimal accumulator machine	