Small soft core uP Inventory
under 500 LUTs with source code

_uP_cores_test folder	opencores name	status	author	style / clone	data size	inst size	FPGA	reporter	comments	LUTs ALM	LUT?	mults	blk ram	F max	date	tool ver	MIPS /clk	clks/ inst	KIPS /LUT	src code	# src files	top file	doc	tool chain	fltg pt	Hard vd	max data	max inst	byte adrs	# inst	# reg	pipe len	start year	last revis	reference	note worthy	comments
mc6809e		beta	Flint Weller	6809	8	8x	kintex-7-3	James Bra	gate level prin	6						14.7	0.33	3.0		vhdl	26	core_68	yes	yes	N	N	64K	64K	Y				1999		6809 data sheets	course work, ASIC orientation	
Lutiac		custom	David Galloway, David	2 reg	16	NA	stratix-4	David Galloway		140	A	4		198			0.67	1.0	947.6	vhdl & verilog								64	N	64	32	3		2010	Lutiac – Small Soft Proc	no inst RAM, instead microcode	no inst mem: small state machine, ~200 in
hive	hive	stable	Eric Wallin	4-8 stack	32	16	cyclone-3	Eric Wallin		1800	4	4	3	200		13.0	1.00	1.0	111.1	verilog		core	yes		N				N	40	10	8	2013	2014		4-8 symetrical stacks, eight threads via pipeline barrel	
hive	hive	stable	Eric Wallin	4-8 stack	32	16	cyclone-5	James Brakefield		628	A	3	3	217	##	13.1	1.00	1.0	345.0	verilog		core	yes		N				N	40	10	8	2013	2014		4-8 symetrical stacks, eight threads via pipeline barrel	
hive	hive	stable	Eric Wallin	4-8 stack	32	16	arria-2	James Brakefield		905	A	8	19	284	##	13.1	1.00	1.0	313.4	verilog		core	yes		N				N	40	10	8	2013	2014		4-8 symetrical stacks, eight threads via pipeline barrel	
blue	16-bit CPU Blue	stable	Al Williams	accum	16	16	spartan-3-5	James Bra	removi	1025	4			63	##	14.7	0.67	1.0	41.1	verilog	16	topbox	web		N		4K	4K	N	16	2		2009	2010		Caxton Foster's Blue derivative	http://www.youtube.com/watch?v=dt4ze
lem1_9	lem1_9	stable	James Brakefield	accum	1	9	spartan-3-5	James Brakefield		55	4		1	136	##	14.5	0.04	1.0	98.7	vhdl	3	lem1_9r	yes	asm	N	Y	64	2K	N	8	64	1	2003	2009		very small, 2 pipe stage is faster with no i	"logic emulation machine"
lem1_9	lem1_9	stable	James Brakefield	accum	1	9	spartan-6-3	James Brakefield		42	6		1	217	##	14.5	0.04	1.0	207.0	vhdl	3	lem1_9r	yes	asm	N	Y	64	2K	N	8	64	1	2003	2009		very small, 2 pipe stage is faster with no i	"logic emulation machine"
lem1_9	lem1_9	stable	James Brakefield	accum	1	9	kintex-7	James Brakefield		40	6		1	358	##	14.5	0.04	1.0	357.5	vhdl	3	lem1_9r	yes	asm	N	Y	64	2K	N	8	64	1	2003	2009		very small, 2 pipe stage is faster with no i	"logic emulation machine"
leros	Leros	stable	Martin Schoeberl	accum	16	16	cyclone-4-6	Martin Schoeberl		189	4		1	160			0.67	1.0	567.2	vhdl	5	leros	yes	yes	N	Y	256	64K			2	2	2008	2012	Leros: A Tiny Microcont	short LUT inst ROM	256 word data RAM, PIC like
leros	Leros	stable	Martin Schoeberl	accum	16	16	spartan-3	Martin Schoeberl		188	4		1	129			0.67	1.0	459.7	vhdl	5	leros	yes	yes	N	Y	256	64K			2	2	2008	2012	Leros: A Tiny Microcont	short LUT inst ROM	256 word data RAM, PIC like
leros	Leros	stable	Martin Schoeberl	accum	16	16	spartan-6	Martin Schoeberl		112	6		1	182			0.67	1.0	1088.8	vhdl	5	leros	yes	yes	N	Y	256	64K			2	2	2008	2012	Leros: A Tiny Microcont	short LUT inst ROM	256 word data RAM, PIC like
leros	Leros	stable	Martin Schoeberl	accum	16	16	cyclone-2	James Bra	missing	243	4		1	137	##	11.1	0.67	1.0	378.7	vhdl	5	leros	yes	yes	N	Y	256	64K			2	2	2008	2012	Leros: A Tiny Microcont	short LUT inst ROM	256 word data RAM, PIC like
leros	Leros	stable	Martin Schoeberl	accum	16	16	cyclone-4-6	James Bra	missing	238	4		1	149	##	13.1	0.67	1.0	420.7	vhdl	5	leros	yes	yes	N	Y	256	64K			2	2	2008	2012	Leros: A Tiny Microcont	short LUT inst ROM	256 word data RAM, PIC like
leros	Leros	stable	Martin Schoeberl	accum	16	16	arria-2	James Bra	missing	164	A		1	266	##	13.1	0.67	1.0	1086.2	vhdl	5	leros	yes	yes	N	Y	256	64K			2	2	2008	2012	Leros: A Tiny Microcont	short LUT inst ROM	256 word data RAM, PIC like
leros	Leros	stable	Martin Schoeberl	accum	16	16	spartan-3-5	James Bra	missing	247	4		1	105	##	14.7	0.67	1.0	285.7	vhdl	5	leros	yes	yes	N	Y	256	64K			2	2	2008	2012	Leros: A Tiny Microcont	short LUT inst ROM	256 word data RAM, PIC like
leros	Leros	stable	Martin Schoeberl	accum	16	16	spartan-6	James Bra	missing	174	6		1	155	##	14.7	0.67	1.0	595.9	vhdl	5	leros	yes	yes	N	Y	256	64K			2	2	2008	2012	Leros: A Tiny Microcont	short LUT inst ROM	256 word data RAM, PIC like
leros	Leros	stable	Martin Schoeberl	accum	16	16	kintex-7-3	James Bra	missing	169	6		1	274	##	14.7	0.67	1.0	1084.7	vhdl	5	leros	yes	yes	N	Y	256	64K			2	2	2008	2012	Leros: A Tiny Microcont	short LUT inst ROM	256 word data RAM, PIC like
lwrisc	ClaiRISC	stable	Li Wu	accum	8	12	arria-2	James Brakefield		88	A		1	230	##	13.1	0.17	1.0	443.6	verilog	9	risc_core		asm	N	Y	256	2K	Y	16			2008	2009		simplified PIC, 4 reg rtn stack	absolute addressing only, lowered MIPS/c
mcpu	MCPU A minima	stable	Tim Boscke	accum	8	8	spartan-6-3	James Brakefield		41	6			384	##	14.7	0.08	1.0	749.0	vhdl	1	tb02cpu	yes	asm	N		64	64	Y	4			2007	2014		fits into 32 macrocell CPLD	reduced MIPS/clk due to only 4 inst
micro16b		beta	John Kent	accum	16	16	kintex-7	James Brakefield		205	6			434	##	14.7	0.33	2.0	349.0	vhdl	1	u16bcpu	yes	asm	N	N	64K	4K	Y	8			2002	2008	members.optushome.c	very limited inst set	MIPS/clk adj'd, 2 clks/inst
micro8a		beta	John Kent	accum	8	16	kintex-7	James Brakefield		531	6			204	##	14.7	0.33	3.0	42.3	vhdl	11	Micro8	yes		N	N	2K	2K	Y				2002	2002	members.optushome.c	derived from Tim Boscke's mcpu, not perfected	
popcorn		stable	Jeung Joon Lee	accum	8	8x	spartan-6-3	James Brakefield		268	6			171	##	14.7	0.33	1.0	210.9	verilog	4	pc	yes		N		64K	64K	Y	43			2000			small 8 bit uP	
popcorn		stable	Jeung Joon Lee	accum	8	8x	kintex-7-3	James Brakefield		267	6			347	##	14.7	0.33	1.0	428.4	verilog	4	pc	yes		N		64K	64K	Y	43			2000			small 8 bit uP	
tisc	Tiny Instruction	beta	Vincent Crabtree	accum	8	8x	spartan-6-3	James Brakefield		198	6			60	##	14.7	0.33	1.0	99.5	vhdl	1	TISC			N		256	1K	Y		2		2009	2009		minimal accumulator machine	
tisc	Tiny Instruction	beta	Vincent Crabtree	accum	8	8x	kintex-7-3	James Brakefield		195	6			87	##	14.7	0.33	1.0	147.1	vhdl	1	TISC			N		256	1K	Y		2		2009	2009		minimal accumulator machine	
usimplez	MicroSimplez	stable	Pablo Salvadeo etal	accum	12	12	stratix-2	Pablo Salvadeo		48	4			134		9.1	0.17	1.0	475.9	vhdl	3	usimplez_cpu			N		512	512		8			2011		http://www-gti.det.uvig	part of university course, simplez+i4 has	MIPS/Mhz reduced due to few inst
c16	16 Bit Microcon	stable	Jsauermann	C	16	8x	spartan-3-5	James Brakefield		1850	4		16	57	##	14.7	0.33	1.0	10.1	vhdl	22	Board_c	min	C,asm	N		64K	64K	Y		5		2003	2012		8080 derivative, optional UART, 8-bit memory port	
tiny8	tiny8	mature	Ulrich Riedel	CISC	8	8x			Flex10K design									1.0		ahdl & schematic				asm	N		64K	64K	Y				2002	2009		registers in RAM like TMS9900, uses Altera AHDL, megafunctions & schematic entry
xproz		stable	Herbert Kleebauer	CISC	16	16x												1.0		schematic			yes	asm	N		64K	64K					1995			documentation in German	
oc54x	OpenCores54x b	beta	Richard Herveille	DSP	16	16	kintex-7-3	James Brakefield		2225	6	1		180	##	14.7	0.67	1.0	54.1	verilog	10	oc54_cp	yes	yes	Y	Y	64K	64K					2002	2009		40-bit accumulator, barrel shifter	
ensilica		proprieta	ensilica.com	eSi-1600	16		virtex-5	ensilica		1100	6			160			0.67	1.0	97.5	not avail			yes	yes	N		64K	64K			16				www.ensilica.com	verilog source included with license	10 addressing modes
ensilica		proprieta	ensilica.com	eSi-3200	32		stratix-4	ensilica		1800	A			200			1.00	1.0	111.1	not avail			yes	yes			4G	4G			16	5			www.ensilica.com	verilog source included with license	10 addressing modes
b16		stable	Bernd Paysan	forth	16	5	spartan-6-3	James Brakefield		554	6			134	##	14.7	0.67	1.0	161.7	verilog	1	b16	yes	yes	N								2002	2011	bernd-paysan.de/b16.h	two versions: one/15 source files, derived from c18	
dfp	dfp	stable	Ron Chapman	forth	8	Y	spartan-6-3	James Brakefield		334	6			112	##	14.7	0.33	1.0	110.7	vhdl	25	DataFlov	yes										2003	2009		8-bitter, generates a custom VHDL stack machine, compiler is in Forth	
dfp	dfp	stable	Ron Chapman	forth	8	Y	kintex-7-3	James Brakefield		297	6			192	##	14.7	0.33	1.0	213.2	vhdl	25	DataFlov	yes										2003	2009		8-bitter, generates a custom VHDL stack machine, compiler is in Forth	
eric5		proprieta	enter-electronics.com	forth	9	8	cyclone-4-6	enter-electronics.		110	4	opt		60			0.42	1.0	229.1	not avail							512	1K			3-4		2007			25 MIPS: ERIC5xs, ERIC5Q	
J1		stable	James Bowman	forth	16	16	spartan-6	James Brakefield		333	6		1	117	##	14.7	0.80	1.0	280.2	vhdl	1	j1	yes	forth	N		64K	64K		16		2	2006	2010	excamera.com/sphinx/f	uCode inst, dual port block RAM	32 deep data & return stacks
J1		stable	James Bowman	forth	16	16	kintex-7-3	James Brakefield		387	6		4	133	##	14.7	0.80	1.0	274.6	verilog	1	j1	yes	forth	N		64K	64K		16		2	2006	2010	excamera.com/sphinx/f	uCode inst, dual port block RAM	32 deep data & return stacks
jop	JOP a Java Optin	stable	Martin Schoeberl etal	forth	16	16	cyclone-1	Martin Schoeberl		2000	4			100		10	0.67	1.0	33.5	vhdl	11	core	yes	yes	N		256K	256K					2004	2014		opencores download is empty	https://github.com/jop-devel/jop
microcore		beta	Klaus Schleisiek	forth	32	8	spartan-6-3	James Brakefield		591	6		1	71	##	14.7	1.00	1.0	120.1	vhdl	10	core	yes	asm	N	Y	2M	512K					2004		has several PDFs	indexing into return stack, auto inc/dec,	AKA uCore110
microcore		beta	Klaus Schleisiek	forth	32	8	kintex-7-3	James Brakefield		644	6			149	##	14.7	1.00	1.0	231.3	vhdl	10	core	yes	asm	N	Y	2M	512K					2004		has several PDFs	indexing into return stack, auto inc/dec,	AKA uCore110
myforthproce	FORTH processc	stable	Gerhard Hohner	forth	32		spartan-3	James Bra	xilinx primitive	4						14.7	1.00	1.0		vhdl	51	mycpu	yes	yes	Y								2012	2012		DPANS'94 32-bit Forth, masters thesis, four variants	
nige_machine		stable	Andrew Read	forth	32	8	kintex-7-3	James Brakefield		5033	6	8	33	123	##	14.7	1.00	1.0	24.5	vhdl	29	Board	yes	yes	N		16M	16M		512	512			2014		standalone Forth system	
ssbcc	Smal Stack Base	stable	Rodney Sinclair	forth	8	9			syntax errors									1.0		verilog	3	core	yes	asm	N				Y				2012	2014		Python program generates the Verilog	
zpu	ZPU the worlds	stable	Oyvind Harboe	forth	32	8	spartan-6	Oyvind Harboe		1259	6			135			0.10	1.0	10.7	vhdl	23	zpu_cor	yes	yes	N		4G	4G	Y	37			2008	2009	www.zylin.com	zpu4: 16 & 32 bit versions, code size 80% of	ARM (thumb), low MIPs/MHz
zpu	ZPU the worlds	stable	Oyvind Harboe	forth	32	8	spartan-3	Oyvind Harboe		440	4			85			0.05	1.0	9.7	vhdl	23	zpu_cor	yes	yes	N		4G	4G	Y	37			2008	2009	www.zylin.com	zpu4: 16 & 32 bit versions, code size 80% of	ARM (thumb), low MIPs/MHz
8bit_chapman		beta	Rob Chapman, Steven	forth	8	8	kintex-7-3	James Bra	syntax errors		6					14.7	0.33	1.0		vhdl	10	top	yes		N		256	256					1998			course work	
cpu16		beta	C. H. Ting	forth	16	5	kintex-7-3	James Bra	case co	367	6			355	##	14.7	0.67	1.0	648.1	vhdl	1	cpu16	yes	asm	N		64K	64K		28			2000			part of eForth?	data width can be expanded
dataflow_chapman		alpha	Rob Chapman, Steven	forth			kintex-7-3	James Bra	file WebCase		6					14.7	0.33	1.0		vhdl	27	DataFlov	yes		N		256	256					2003			course work	
msl16		beta	Philip Leong, Tsang, Le	forth	16	4	kintex-7-3	James Brakefield		303	6			256	##	14.7	0.67	1.0	566.4	vhdl	13	cpu	yes	asm	N		256			16			2001			CPLD prototype	
p16		alpha	Don Golding	forth	16	5	kintex-7-3	James Bra	bad syntax		6					14.7	0.67	1.0		vhdl	1	p16			N		64K	64K					2000				
x32		stable	Sijmen Woutersen	forth	32	8	kintex-7-3	James Bra	missing define		6					14.7	1.00	1.0		vhdl	32	core	yes	yes	N		4G	4G	Y				2006	2007		MS thesis, byte code, needs caches	
theia_gpu	Theia: ray graph	beta	Diego Valverde	GPU														1.0		verilog	32	Theia	yes	asm	N						12		2011	2012		multi-core, 3D rendering & shader	
edge	Edge Processor	alpha	Hesham ALMatary	MIPS	32	32	spartan-6-3	Hesham A	unkown modu		6	7		50		14.7	1.00	1.0		verilog	30	edge_at	yes	yes	N	N	4G	4G	Y		32	5	2014		MIPS data sheets	MIPS1 clone, on Atlys Spartan-6 LX45	
edge	Edge Processor	alpha	Hesham ALMatary	MIPS	32	32	spartan-6-3	James Brakefield		5345	6	7	1	8	##	14.7	1.00	1.0	1.5	verilog	30	edge_cc	yes	yes	N	N	4G	4G	Y		32	5	2014		MIPS data sheets	MIPS1 clone	
dragonfly		beta	LEOX team	MISC	16	16	kintex-7-3	James Brakefield		788	6			164	##	14.7	0.67	1.0	139.3	vhdl	6	dgf_cor	yes		N		256	2K					2001		www.leox.org	unusual, uses FIFOs	
minsoc	minsoc	stable	Raul Fajardo etal	OpenRISC	32	32	kintex-7-3	James Brakefield		4945	6	4	8	107	##	14.7	1.00	1.0	21.7	verilog	88	or1200_	yes	yes	Y	M	4G	4G	Y		32		2009	2013	www.minsoc.com	minimal OR1200, vendor neutral, has caches	
or1k	OpenRISC	stable	Adam Edvardsson etal	OpenRISC	32	32												1.0		verilog			yes	yes	N		4G	4G	Y		32		2001	2014		extensive documentation	
octavo		beta	Charles LaForest	reg	16	16	stratix-4	Charles LaForest		500	A	1		550			0.67	1.0	737.0	verilog	18	Octavo	yes	asm	N					14	16	10		2012	Octavo: an FPGA-Centri	8 core barrel, adjustable data width	"~= performance across word sizes, no call
alwcpu	Alwcpu	alpha	Andreas Hilvarsson	RISC	16	16	kintex-7-3	James Brakefield		298	6			237	##	14.7	0.67	1.0	533.3	vhdl	7	top	some		N		64K	64K	Y		16		2009	2009		lightweight CPU	
atlas_2K	Atlas Processor	beta	Stephan Nolting	RISC	16	16	kintex-7-3	James Brakefield		2434	4	1	9	85	##	14.7	0.80	1.0	28.0	vhdl	19	ATLAS_2	yes	asm	N	Y	64K	64K	M	80	8		2013	2014	opencore page	ARM thumb like inst set	has MMU & full SOC features
atlas_2K	Atlas Processor	beta	Stephan Nolting	RISC	16	16	cyclone-4-6	Stephan Nolting		2730	4	1	32	98	##	13.1	0.80	1.0	28.6	vhdl	19	ATLAS_2	yes	asm	N	Y	64K	64K	M	80	8		2013	2014	opencore page	ARM thumb like inst set	has MMU & full SOC features
atlas_2K	Atlas Processor	beta	Stephan Nolting	RISC	16	16	cyclone-2	James Brakefield		2711	4	1	64	71	##	11.1	0.80	1.0	21.0	vhdl	19	ATLAS_2	yes	asm	N	Y	64K	64K	M	80	8		2013	2014	opencore page	ARM thumb like inst set	has MMU & full SOC features
atlas_2K	Atlas Processor	beta	Stephan Nolting	RISC	16	16	arria-2	James Brakefield		1624	A	2	32	118	##	13.1	0.80	1.0	58.3	vhdl	19	ATLAS_2	yes	asm	N	Y	64K	64K	M	80	8		2013	2014	opencore page	ARM thumb like inst set	has MMU & full SOC features
atlas_2K	Atlas Processor	beta	Stephan Nolting	RISC	16	16	spartan-3a	James Brakefield		2450	4	1	9	76	##	14.7	0.80	1.0	24.9	vhdl	19	ATLAS_2	yes	asm	N	Y	64K	64K	M	80	8		2013	2014	opencore page	ARM thumb like inst set	has MMU & full SOC features
atlas_2K	Atlas Processor	beta	Stephan Nolting	RISC	16	16	spartan-6-3	James Brakefield		1545	6	1	10	100	##	14.7	0.80	1.0	51.5	vhdl	19	ATLAS_2	yes	asm	N	Y	64K	64K	M	80	8		2013	2014	opencore page	ARM thumb like inst set	has MMU & full SOC features
atlas_2K	Atlas Processor	beta	Stephan Nolting	RISC	16	16	kintex-7-3	James Brakefield		1512	6	1	5	149	##	14.7	0.80	1.0	79.1	vhdl	19	ATLAS_2	yes	asm	N	Y	64K	64K	M	80	8		2013	2014	opencore page	ARM thumb like inst set	has MMU & full SOC features
atlas_core	Atlas Processor	beta	Stephan Nolting	RISC	16	16	arria-2	James Brakefield		810	A	2	0	123	##	13.1	0.80	1.0	121.2	vhdl	8	ATLAS_(	yes	asm	N	Y	64K	64K	Y	80	8		2013	2014	opencore page	ARM thumb like inst set	non-MMU version
atlas_core	Atlas Processor	beta	Stephan Nolting	RISC	16	16	spartan-6	James Brakefield		643	6	1	0	103	##	14.7	0.80	1.0	127.9	vhdl	8	ATLAS_(	yes	asm	N	Y	64K	64K	Y	80	8		2013	2014	opencore page	ARM thumb like inst set	non-MMU version
atlas_core	Atlas Processor	beta	Stephan Nolting	RISC	16	16	kintex-7-3	James Brakefield		648	6	1	0	168	##	14.7	0.80	1.0	207.6	vhdl	8	ATLAS_(	yes	asm	N	Y	64K	64K	Y	80	8		2013	2014	opencore page	ARM thumb like inst set	non-MMU version
ba22		proprieta	CAST Inc	RISC	32	16x	spartan-6	CAST Inc		1800	6		32	72			1.00	1.0	40.0	not avail							4G	4G			32				www.cast-inc.com		
dcpu16		beta	Marcus Persson , Shav	RISC	16	16	kintex-7-3	James Brakefield		662	6	1		318	##	14.7	0.67	4.0	80.4	vhdl &	5	dcpu16_	yes	asm	N	N	64K	64K	N	37	8		2009	2012	https://github.com/dcp	for the 0X10c game	4+ addressing modes, 4 & 5-bit reg /mode
fpgammix		stable	Tommy Thorn	RISC	64	32	arria-2	James Brakefield		####	A	8	10	94	##	13.1	1.50	4.0	3.0	system	2	core	yes	yes	Y	Y	4G	4G	Y	256	288		2006	2008		clone of Knuth's MMIX	micro-coded
gumnut		stable	Peter Ashenden	RISC	8	18	kintex-7-3	James Brakefield		420	6			275	##	14.7	0.33	1.0	216.2	vhdl	20	gumnut	yes		N		256	4K	Y		8		2007			see Digital Design: An Embedded System	does not seem complete
jane_nn		stable	Suresh Devanathan	RISC	4	8	kintex-7-3	James Brakefield		723	6			178	##	14.7	0.33	1.0	81.4	vhdl	3	Processe	yes								27	16		2002			neural network microprocessor, specialized registers	
latticemicro32		stable	Yann Siommeau, Mich	RISC	32	32	spartan-6	James Brakefield		2093	6	3	15	85	##	14.7	0.80	1.0	32.4	verilog	24	lm32_cp	yes	yes	N		4G	4G	Y		32		2006	2012	en.wikipedia.org/wiki/L	optional data & inst caches	
latticemicro32		stable	Yann Siommeau, Mich	RISC	32	32	kintex-7-3	James Brakefield		2292	6	3	8	155	##	14.7	0.80	1.0	54.2	verilog	24	lm32_cp	yes	yes	N		4G	4G	Y		32		2006	2012	en.wikipedia.org/wiki/L	optional data & inst caches	
latticemicro8		stable	Lattice Semiconductor	RISC	8	18	LFE2	Lattice Semicondu		265	4			104			0.33	2.0	64.4	vhdl	10	isp8_cor	yes	yes	N		256	4K	Y		32		2005	2010	en.wikipedia.org/wiki/L	16 deep call stack, four configurations	
natalius_8bit	Natalius 8 bit RI	beta	Fabio Guzman	RISC	8	16	spartan-3e	James Brakefield		385	4		2	59	##	14.7	0.11	3.0	5.7	verilog	12	natalius	yes	asm	N	Y	256	2K	Y	29	8		2012	2012		return stack & register file	3 clocks/inst
natalius_8bit	Natalius 8 bit RI	beta	Fabio Guzman	RISC	8	16	kintex-7-3	James Brakefield		232	6		1	175	##	14.7	0.11	3.0	27.7	verilog	12	natalius	yes	asm	N	Y	256	2K	Y	29	8		2012	2012		return stack & register file	3 clocks/inst
open8_urisc	Open8 uRISC	stable	Kirk Hays, Jshamlet	RISC	8	8	kintex-7-3	James Brakefield		691	6	1		263	##	14.7	0.33	1.0	125.6	vhdl	9	Open8	yes	yes	N		64K	64K	Y		8		2006	2013		accum & 8 regs, clone of Vautomation uRISC	processor, in use
risc5		beta	Niklaus Wirth	RISC	32	32	cyclone-4	James Brakefield		3503	4		1	54	##	13.1	1.00	1.0	15.4	verilog	8	RISC5	yes	yes	Y		4G	4G			16		2013			minimalist Wirth, part of Project Oberon	32x32 multiplier ?
risc5		beta	Niklaus Wirth	RISC	32	32	arria-2	James Brakefield		2362	A		3	73	##	13.1	1.00	1.0	31.0	verilog	8	RISC5	yes	yes	Y		4G	4G			16		2013			minimalist Wirth, part of Project Oberon	32x32 multiplier
risc5		beta	Niklaus Wirth	RISC	32	32	spartan-3-5	James Brakefield		3005	4	4	1	34	##	14.7	1.00	1.0	11.4	verilog	8	RISC5	yes	yes	Y		4G	4G			16		2013			minimalist Wirth, part of Project Oberon	32x32 multiplier
risc5		beta	Niklaus Wirth	RISC	32	32	spartan-6-3	James Brakefield		2283	6	4	1	55	##	14.7	1.00	1.0	24.3	verilog	8	RISC5	yes	yes	Y		4G	4G			16		2013			minimalist Wirth, part of Project Oberon	32x32 multiplier

risc5		beta	Niklaus Wirth	RISC	32	32	kintex-7-3	James Brakefield	2441	6	4	1	92	##	14.7	1.00	1.0	37.8	verilog	8	RISC5	yes	yes	Y		4G	4G			16		2013				minimalist Wirth, part of Project Oberon	32x32 multiplier
rise	RISE Microproce	beta	Jlechner etal	RISC	16	16	kintex-7-3	James Bra	missing black l	6	1				14.7	0.67	1.0		vhdl	26	rise	yes	asm	N		64K	64K			16	5	2006	2010	en.wikiversity.org/wiki/	ARM style register usage	
sayeh_proces	SAYEH educatio	stable	Alireza Haghdoost, Arr	RISC	16	16	kintex-7-3	James Brakefield	479	6	1		164	##	14.7	0.67	1.0	229.7	verilog	13	Sayeh	yes		N		64K	64K			32		2008	2009	haghdoost.persiangig.co	simple RISC	
scarts	Scarts Processor	beta	Jlechner, Martin Walte	RISC	16	16	kintex-7-3	James Bra	missing signal	6					14.7	0.67	1.0		vhdl	18	scarts		yes	N		64K	64K		122	16	4	2011	2012		GCC compiler	
sxp	SXP (Simple eXt	beta	Sam Gladstone etal	RISC	32	32			too many los										verilog		sxp			N		4G	4G			32		2001	2009		basic RISC	too many los
tiny64	Tiny64	stable	Ulrich Riedel	RISC	64		kintex-7-3	James Bra	bit length miss	6					14.7	1.00	1.0		vhdl	7	TinyX		asm	N		64K	64K		16	8		2004	2009		word size configurable from 32 to 64	
xr16		stable	Jan Gray	RISC	16	16	kintex-7-3	James Brakefield	371	6			7	##	14.7	0.67	1.0	13.0	verilog	12	xsoc	yes		N		64K	64K			16		1999	2001		handcrafted FPGA layout & instruction se	source code written for simulation
cole_c16		beta	Cole Design & Develop	RISC	16	16	spartan-6-3	James Brakefield	554	6			298	##	14.7	0.67	7.0	51.4	vhdl	1	core	yes	asm	N		64K	64K	N	20	8		2002	2012		(7) clks per inst, complete SOC	for teaching
diogenes	diogenes	beta	Fekknhifer	RISC	16	16	kintex-7-3	James Brakefield	807	6		1	297	##	14.7	0.67	1.0	246.3	vhdl	11	cpu	yes	yes	N			1K					2008	2009		"student RISC system"	
eco32	SOC:ECO32	stable	Hellwing Geisse	RISC	32	32	cyclone-4-6	James Brakefield	5153	4			79	##	13.1	1.00	1.5	10.2	verilog	23	eco32	yes	yes	N		512M	256M	Y	61	32		2003	2014		MIPS like, slow mul & div	
eco32	SOC:ECO32	stable	Hellwing Geisse	RISC	32	32	spartan-3-5	James Brakefield	4564	4		10	51	##	14.7	1.00	1.5	7.4	verilog	23	eco32	yes	yes	N		512M	256M	Y	61	32		2003	2014		MIPS like, slow mul & div	downloaded ISE project run, has *.ucf
eco32	SOC:ECO32	stable	Hellwing Geisse	RISC	32	32	cyclone-4-6	James Brakefield	5153	4			79	##	13.1	1.00	1.5	10.2	verilog	23	cpu	yes	yes	N		512M	256M	Y	61	32		2003	2014		MIPS like, slow mul & div	
eco32	SOC:ECO32	stable	Hellwing Geisse	RISC	32	32	arria-2	James Brakefield	2711	A			116	##	13.1	1.00	1.5	28.6	verilog	23	cpu	yes	yes	N		512M	256M	Y	61	32		2003	2014		MIPS like, slow mul & div	
eco32	SOC:ECO32	stable	Hellwing Geisse	RISC	32	32	spartan-3-5	James Brakefield	3034	4		2	55		14.7	1.00	1.5	12.0	verilog	23	cpu	yes	yes	N		512M	256M	Y	61	32		2003	2014		MIPS like, slow mul & div	
eco32	SOC:ECO32	stable	Hellwing Geisse	RISC	32	32	spartan-6-3	James Brakefield	2271	6		1	92		14.7	1.00	1.5	27.0	verilog	23	cpu	yes	yes	N		512M	256M	Y	61	32		2003	2014		MIPS like, slow mul & div	
eco32	SOC:ECO32	stable	Hellwing Geisse	RISC	32	32	atrix-7-3	James Brakefield	2107	6		1	121		14.7	1.00	1.5	38.4	verilog	23	cpu	yes	yes	N		512M	256M	Y	61	32		2003	2014		MIPS like, slow mul & div	
eco32	SOC:ECO32	stable	Hellwing Geisse	RISC	32	32	kintex-7-3	James Brakefield	2210	6		1	160		14.7	1.00	1.5	48.1	verilog	23	cpu	yes	yes	N		512M	256M	Y	61	32		2003	2014		MIPS like, slow mul & div	
eight_bit_uc		stable	Synplicity	RISC	8	12	kintex-7-3	James Bra	signal/variable	6					14.7	0.67	1.0		vhdl	10	eight_bit_uc						2K	Y		32						part of Amplify documentation	
erp	Educational RISC	stable	Shahzadjk	RISC	8	16	spartan-3-5	James Brakefield	366	4	1	1	70	##	14.7	0.33	1.0	63.5	verilog	1	ERPveril	yes							15	6	2004	2009		two report PDFs & one Verilog file	
erp	Educational RISC	stable	Shahzadjk	RISC	8	16	kintex-7-3	James Bra	4K primitives	6				##	14.7	0.33	1.0		verilog	1	ERPveril	yes							15	6	2004	2009		two report PDFs & one Verilog file	
hicovec	HiCoVec a config	beta	Harald Manske, Gundc	RISC	32	32	kintex-7-3	James Bra	compiler error	6					14.7	1.00	1.0		vhdl	28	cpu	yes	asm	N				Y				2008	2010		hybrid scalar & vector processor	
hpc-16	HPC-16	beta	Umair Siddiqui	RISC	16	16	kintex-7-3	James Brakefield	875	6			136	##	14.7	0.67	1.0	104.2	vhdl	20	cpu	yes	asm	N		64K	64K			16		2005	2009			
iDEA		proprietar	Liu Cheah etal	RISC	16	32	virtex-6	Liu Cheah		190	6	1	1	534			0.67	1.0	1883.1	not avail										20	32	9		2011	A Lean FPGA Soft Proce	uses DSP slice in barrel mode for ALU	by Xilinx, no source
jam		stable	Johan Thelin etal	RISC	32	32	kintex-7-3	James Brakefield	1369	6			143	##	14.7	1.00	1.0	104.2	vhdl	17	cpu	yes		N	Y	128K	128K			32	5	2002			serial multiply & divide	
jpu16		stable	Joksan Alvarado	RISC	16	26	kintex-7-3	James Bra	missing define	6					14.7	0.67	1.0		vhdl	9	JPU16	yes	asm	N		64K	64K			16		2012			32 deep call stack, 8 addressing modes	
manik		stable	Sandeeo Dytta	RISC	32	32	kintex-7-3	James Bra	needs editing	6					14.7	0.33	1.0		vhdl	45	manik2t	yes	yes	N		4K	4K	Y		16		2002	2006	www.niktech.com/	optional data & inst caches	supports Xilinx, Altera, Actel, Lattice
marca	McAdam's RISC	stable	Wolfgang Puffitsch	RISC	16	16	arria-2	James Brakefield	1763	A		22	157	##	13.1	0.67	6.0	10.0	vhdl	40	marca	yes		N		8K	16K		75	16	4	2007	2009		serial multiply & divide	clks/inst is approx
myrisc1	myRISC1	stable	Muza Byte	RISC	8	8	cyclone-2	Muza Byte	Altera	185	4		1	57		0.33	1.0	101.8	verilog		myRISC1	yes		N	Y	256	256	Y	16	4		2011	2011		Verilog source included in PDF file	LPM macros
qrisc32	qrisc32 wishbon	alpha	Viacheslav	RISC	32	32	arria-2	James Brakefield	3075	A	4		144	##	13.1	1.00	1.0	46.9	system	8	qrisc32	yes	yes	N		4G	4G	Y		32	4	2010	2011		for PhD thesis	
raptor64	Raptor64	planning	Robert Finch	RISC	64	32	kintex-7-3	James Bra	missing port n	6					14.7	1.50	1.0		verilog	48	Raptor64	yes	yes	Y		2<<64	2<<64	Y		32		2012	2013		8-16-32-64 bit data, cache, MMU, hyper-threaded version also	
risc0		beta	Niklaus Wirth	RISC	32	32	kintex-7-3	James Brakefield	1186	6	4	6	110	##	14.7	0.67	1.0	61.9	verilog	8	RISC0	yes	yes	N		4G	4G					2011			minimalist Wirth, education tool	
tinycpu	TinyCPU	alpha	Jordan Earls	RISC	8	16	kintex-7-3	James Bra	bit leng	1182	6			200	##	14.7	0.33	2.0	28.0	vhdl	10	top		asm	N	N	64K	64K			16		2012	2012			
yasep		alpha	Yann Guidon	RISC	16	32	kintex-7-3	James Bra	syntax errors	6					14.7	1.00	1.0		vhdl		microYA	yes	asm	N			2K			16		2008	2014	www.yaesp.org	Java generated VHDL, revisions ongoing	funky web site
lemberg		stable	Wolfgang Puffitsch	VLIW	32	32	cyclone-4-6	James Bra	fitter failed		4				13.1	1.00	1.0		vhdl	32	core	yes	yes	Y		4G	2M	Y		32	4	2011		www2.imm.dtu.dk/~wo	upto 4 inst/clock	
bobcat		beta	Stan Drey		16	24	kintex-7-3	James Brakefield	1622	6	1		107	##	14.7	0.67	1.0	44.0	vhdl							64K	64K					1998			appears to be a DSP	
vtach	VTACH Bell Labs	mature	Al Williams		13	12	spartan-3-4	James Brakefield	557	4			71	##	14.7	0.50	1.0	64.1	verilog	16	vtach			N		256	256	Y				2913	2013		ISE project only, BCD arithmetic	
vtach	VTACH Bell Labs	mature	Al Williams		13	12	kintex-7-3	James Bra	xilinx core pro	6					14.7	0.50	1.0		verilog	16	vtach			N		256	256	Y				2913	2013		ISE project only, BCD arithmetic	

71 # usable(beta, stable or mature): "A"(clones) & "W"(original # reg bits

33 "B" or "X" of limited interest

adr locations

MIPS/MHz Pro-rating for data size:

1-bit	0.04
8-bit	0.33
16-bit	0.67
32-bit	1.00

Under the assumption that the core is capable of one instuction per clock

Silicon Area equivalents

LUTS/DSP48	16:1
LUTS/Block RAM	32:1

Following has DMIPS per clock for many microprocessors

http://en.wikipedia.org/wiki/Instructions_per_second

Web page DMIPS per clock cycle per cc en.wikipe community.freescale.com/thread/60391

uP	MIPS			CoreMarks /MHz	MHz	
4004	0.10					
6502	0.50		0.02	0.06		
8051	0.01	DMIPS	0.08	0.24		
8080	0.17			0.25		
68K	0.10			0.15		
ARM Cortex A9	2.50	DMIPS		2.90	1000	
ARM Cortex M0	0.90	DMIPS		1.50	70	
ARM Cortex M3	1.25	DMIPS		2.17	25	
ARM7	0.90		0.74	2.04	600	
AVR	1.00		0.21	0.53	8	
AVR32				1.62	60	
BA21				2.44	400	
Coldfire				2.80	400	
Coldfire				0.77	150	Virtex-5
HCS08			0.04	0.12		
LEON3/Spartan-6				1.96	100	
MC6809	1.24		0.07	1.86		
MicroBlaze 3-stage	1.03			1.50		
MicroBlaze 5-stage	1.38			1.90	125	
MIPS32	1.51			2.28		
MSP430			0.40	1.20		
MSP430				1.10	25	
Nios II	0.64	DMIPS		0.93	200	
Nios II -e	0.15	DMIPS		0.25		
Nios II -f	1.13	DMIPS		1.60	200	
PIC16	0.25					
PIC18				0.04	40	
PIC24			0.72	1.86	40	
PIC32				3.45	80	
Super H-2				1.44	180	
VAX780	1.00	DMIPS		1.50		DMIPS # is by definition
Z80	1.60		0.01	0.03		
eSi-1600				1.98		

2X 1X 3X

Column Titles	Details
"A"	A: 1st choice clone, B: 2nd choice clone, W: 1st choice original, X: 2nd choice original
"B"	currently unused and hidden
_uP_cores_test folder	if opencores design is their folder name, otherwise my folder name
opencores name	
status	ASIC, planning, alpha, beta, stable, mature, proprietary
author	First Name, Last Name
style / clone	part number or "forth", RISC, accumulator, etc
data size	data memory word size
inst size	instruction size
FPGA	FPGA family for compile, place, route & timing
reporter	First Name, Last Name
comments	compile, place, route & timing problems
LUTs ALM	4-LUT, 6-LUT, Altera ALM, Actel Tile
LUT?	total number of LUTs or ALMs used including route-thrus & otherwise unavailable
mults	total number of multipliers/DSPs used
blk RAM	total number of block RAMs used, does not include small and extra large Altera block RAMs, Xilinx half block RAM rounded up
Fmax	maximum primary clock speed from compile, place, route & timing run
date	date of compile, place & route; serves to identify source version
tool ver	Altera, Xilinx, Lattice Semiconductor or MicroSemi tool version number
MIPS /clk	prorated DMIPS per clock, reduced for data word sizes under 32-bits, greater than one for multiple issue processors
clks/ inst	number of clocks per instruction, typically 1.0 for modern pipelined processors
KIPS /LUT	figure of merit, does not include effects of memory capacity, floating point or instruction set quality
src code	VHDL or Verilog or other
# src files	number of source files for compile, place, route & timing
top file	top file for compile, place, route & timing run
doc	is documentation provided
tool chain	is there a compiler or assembler provided or available
fltg pt	does the compile, place, route & timing run include floating point
Ha vd	separate instruction and data memory(s), there can be more than one data memory, M for MMU & caches
max data	maximum data address
max inst	maximum instruction address
byte adrs	is byte addressing provided
# inst	number of unique instructions, somewhat subjective
# reg	number of registers in register file
pipe len	number of pipeline stages
start year	year of first design activity
last revis	last year for revisions
reference	web address or generic information (for clones)
note worthy	anything special about the design