Opencore and other soft core processors

_or_cores _test	opencores name	status	author	style / clone	data size	inst size	FPGA	reporter	comment	LUTs ALM	LUT	multiPs	blk ram	F max	date	tool ver	MIPS /clk	clks/ inst	KIPS /LUT	src code	# src files	top file	doc	tool chain	fltg pt	Hav	max data	max inst	byte adrs	# inst	# reg	pipe	start year	last revis	reference	note worthy	comments
X 1	iDEA		proprietar	Liu Cheah etal	RISC	16	32	virtex-6	Liu Cheah	190	6	1	1	534			0.67	1.0	1883.1	not avail										20	32	9		2011	A Lean FPGA Soft Pro	uses DSP slice in barrel mode for ALU	by Xilinx, no source
	risc_core_i	RISC_Core_I	planning	Manuel Imhof	RISC	16	16	kintex-7-3	James Brakef	349	6	1		717	##	14.7	0.67	1.0	1377.2	vhdl	13	CPU	yes	asm	N		1K	1K			8	4	2001	2009	Havard arch	dubious Fmax
W 1	leros	Leros	stable	Martin Schoeberl	accum	16	16	spartan-6	Martin Schoe	112	6		1	182			0.67	1.0	1088.8	vhdl	5	leros	yes	yes	N	Y	256	64K		2	2	2008	2012	Leros: A Tiny Microco	short LUT inst ROM	256 word data RAM, PIC like
W	leros	Leros	stable	Martin Schoeberl	accum	16	16	arria-2	James missir	164	A		1	266	##	13.1	0.67	1.0	1086.2	vhdl	5	leros	yes	yes	N	Y	256	64K		2	2	2008	2012	Leros: A Tiny Microco	short LUT inst ROM	256 word data RAM, PIC like
W	leros	Leros	stable	Martin Schoeberl	accum	16	16	kintex-7-3	James missir	169	6		1	274	##	14.7	0.67	1.0	1084.7	vhdl	5	leros	yes	yes	N	Y	256	64K		2	2	2008	2012	Leros: A Tiny Microco	short LUT inst ROM	256 word data RAM, PIC like
	lem1_9	lem1_9	stable	James Brakefield	accum	1	9	arria-2	James shoul	12	A			313	##	13.1	0.04	1.0	1043.3	vhdl	3	lem1_9min	yes	asm	N	Y	64	2K	N	8	64	1	2003	2009		very small, 2 pipe stage is faster with	"logic emulation machine"
W 1	Lutiac		custom	David Galloway, David	2 reg	16	NA	stratix-4	David Gallow	140	A	4		198			0.67	1.0	947.6	vhdl & verilog								64	N	64	32	3		2010	Lutiac – Small Soft Pr	no inst RAM, instead microcode	no inst mem: small state machine, ~200 inst optimal
A 1	avr8	Reduced AVR Co	beta	Nick Kovach	AVR	8	16	kintex-7-3	James Brakef	174	6			418	##	14.7	0.33	1.0	792.2	verilog	1	rAVR	yes	yes	N		64K	64K	Y	17	4		2010	2010	AVR data sheets	not a full clone, doc is opencores page	
X 1	mcpu	MCPU A minima	stable	Tim Boscke	accum	8	8	spartan-6-3	James Brakef	41	6			384	##	14.7	0.08	1.0	749.0	vhdl	1	tb02cpu2	yes	asm	N		64	64	Y	4			2007	2014		fits into 32 macrocell CPLD	reduced MIPS/clk due to only 4 inst
W 1	octavo		beta	Charles LaForest	reg	16	16	stratix-4	Charles LaFo	500	A	1		550			0.67	1.0	737.0	verilog	18	Octavo	yes	asm	N					14	16	10		2012	Octavo: an FPGA-Cen	8 core barrel, adjustable data width	~= performance across word sizes, no call/rtn inst
	ourisc	16-bit Open uRIS	alpha	Joao Carlos		16	16	stratix-4	Joao Carlos	500	A	1		550			0.67	1.0	737.0	vhdl										26			2013	2013		very incomplete source code	
X 1	cpu16		beta	C. H. Ting	forth	16	5	kintex-7-3	James case c	367	6			355	##	14.7	0.67	1.0	648.1	vhdl	1	cpu16	yes	asm	N		64K	64K		28			2000		part of eForth?	data width can be expanded	
A 1	microblaze		proprieta	Xilinx	uBlaze	32	32	kintex-7	Xilinx	546	6		1	320			1.03	1.0	603.7	not avail			yes	yes	opt		4G	4G	Y	86	32	3	2002		www.xilinx.com/tool	MicroBlaze MCS, smallest configuratio	70 configuration options, MMU optional
W	leros	Leros	stable	Martin Schoeberl	accum	16	16	spartan-6	James missir	174	6		1	155	##	14.7	0.67	1.0	595.9	vhdl	5	leros	yes	yes	N	Y	256	64K		2	2	2008	2012	Leros: A Tiny Microco	short LUT inst ROM	256 word data RAM, PIC like
A 1	ARM_Cortex_A9		ASIC	ARM	ARM a9	32	16	arria V	altera	4500	A			1050			2.50	1.0	583.3	asic			yes	yes	Y		4G	4G	Y	80	16	10		2012	altera data sheets	uses pro-rated LC area	dual issue, includes fltg-pt & MMU & caches
W	leros	Leros	stable	Martin Schoeberl	accum	16	16	cyclone-4-6	Martin Schoe	189	4		1	160			0.67	1.0	567.2	vhdl	5	leros	yes	yes	N	Y	256	64K		2	2	2008	2012	Leros: A Tiny Microco	short LUT inst ROM	256 word data RAM, PIC like
X 1	msl16		beta	Philip Leong, Tsang, Le	forth	16	4	kintex-7-3	James Brakef	303	6			256	##	14.7	0.67	1.0	566.4	vhdl	13	cpu	yes	asm	N		256			16			2001			CPLD prototype	
A	ARM_Cortex_A9		ASIC	ARM	ARM a9	32	16	zynq	xilinx	4500	6			1000			2.50	1.0	555.6	asic			yes	yes	Y	Y	4G	4G	Y	80	16	10		2012	xilinx plan ahead: an	uses pro-rated LC area	dual issue, includes fltg-pt & MMU & caches
W 1	alwcpu	Alwcpu	alpha	Andreas Hilvarsson	RISC	16	16	kintex-7-3	James Brakef	298	6			237	##	14.7	0.67	1.0	533.3	vhdl	7	top	yes	some		N	64K	64K	Y	16			2009	2009		lightweight CPU	
A	ARM_Cortex_A9		ASIC	ARM	ARM a9	32	16	cyclone V	altera	4500	A			925			2.50	1.0	513.9	asic			yes	yes	Y		4G	4G	Y	80	16	10		2012	altera data sheets	uses pro-rated LC area	dual issue, includes fltg-pt & MMU & caches
X 1	usimplez	MicroSimplez	stable	Pablo Salvadeo etal	accum	12	12	stratix-2	Pablo Salvad	48	4			134		9.1	0.17	1.0	475.9	vhdl	3	usimplez_cpu			N		512	512		8			2011		http://www-gti.det.u	part of university course, simplez+i4 h	MIPS/Mhz reduced due to few inst
W	leros	Leros	stable	Martin Schoeberl	accum	16	16	spartan-3	Martin Schoe	188	4		1	129			0.67	1.0	459.7	vhdl	5	leros	yes	yes	N	Y	256	64K		2	2	2008	2012	Leros: A Tiny Microco	short LUT inst ROM	256 word data RAM, PIC like
A 1	lwrisc	ClaiRISC	stable	Li Wu	accum	8	12	arria-2	James Brakef	88	A		1	230	##	13.1	0.17	1.0	443.6	verilog	9	risc_core		asm	N	Y	256	2K	Y	16			2008	2009		simplified PIC, 4 reg rtn stack	absolute addressing only, lowered MIPS/clk
A	microblaze		proprieta	Xilinx	uBlaze	32	32	kintex-7	Xilinx	1201	6		32	408			1.30	1.0	441.4	not avail			yes	yes	opt		4G	4G	Y	86	32	5	2002		www.xilinx.com/tool	performance optimized	70 configuration options, MMU optional
X 1	popcorn		stable	Jeung Joon Lee	accum	8	8x	kintex-7-3	James Brakef	267	6			347	##	14.7	0.33	1.0	428.4	verilog	4	pc	yes		N		64K	64K	Y	43			2000			small 8 bit uP	
W	leros	Leros	stable	Martin Schoeberl	accum	16	16	cyclone-4-6	James missir	238	4		1	149	##	13.1	0.67	1.0	420.7	vhdl	5	leros	yes	yes	N	Y	256	64K		2	2	2008	2012	Leros: A Tiny Microco	short LUT inst ROM	256 word data RAM, PIC like
A 1	nios2		proprietar	Altera	Nios II	32	32	stratix-5	Altera	895	A			310			1.13	1.0	389.7	not avail			yes	yes	opt		4G	4G	Y		32		2004		NIOS2 data sheets	fltg-pt, caches & MMU options	Nios II/f: fastest version
W	leros	Leros	stable	Martin Schoeberl	accum	16	16	cyclone-2	James missir	243	4		1	137	##	11.1	0.67	1.0	378.7	vhdl	5	leros	yes	yes	N	Y	256	64K		2	2	2008	2012	Leros: A Tiny Microco	short LUT inst ROM	256 word data RAM, PIC like
W 1	lem1_9	lem1_9	stable	James Brakefield	accum	1	9	kintex-7	James Brakef	40	6		1	358	##	14.5	0.04	1.0	357.5	vhdl	3	lem1_9min	yes	asm	N	Y	64	2K	N	8	64	1	2003	2009		very small, 2 pipe stage is faster with	"logic emulation machine"
X 1	micro16b		beta	John Kent	accum	16	16	kintex-7	James Brakef	205	6			434	##	14.7	0.33	2.0	349.0	vhdl	1	u16bcpu	yes	asm	N	N	64K	4K	Y	8			2002	2008	members.optushome	very limited inst set	MIPS/clk adj'd, 2 clks/inst
W 1	hive	hive	stable	Eric Wallin	4-8 stack	32	16	cyclone-5	James Brakef	628	A	3	3	217	##	13.1	1.00	1.0	345.0	verilog		core	yes						N	40	10	8	2013	2014		4-8 symetrical stacks, eight threads via pipeline barrel	
A 1	risc16f84	risc16f84	stable	John Clayton	PIC16	8	14	kintex-7-3	James Brakef	331	6			333	##	14.7	0.33	1.0	332.3	verilog	1	risc16f84_c	yes	yes	N	Y	256	4K					2002	2013	PIC16 data sheets	derived from CQPIC by Sumio Morioka	
W	hive	hive	stable	Eric Wallin	4-8 stack	32	16	arria-2	James	905	A	8	19	284	##	13.1	1.00	1.0	313.4	verilog		core	yes		N				N	40	10	8	2013	2014		4-8 symetrical stacks, eight threads via pipeline barrel	
A	nios2		proprietar	Altera	Nios II	32	32	stratix-5	Altera	650	A			300			0.64	1.0	293.4	not avail			yes	yes	opt		4G	4G	Y		32		2004		NIOS2 data sheets	fltg-pt, caches & MMU options	Nios II: balanced version
W	leros	Leros	stable	Martin Schoeberl	accum	16	16	spartan-3-5	James missir	247	4		1	105	##	14.7	0.67	1.0	285.7	vhdl	5	leros	yes	yes	N	Y	256	64K		2	2	2008	2012	Leros: A Tiny Microco	short LUT inst ROM	256 word data RAM, PIC like
W 1	J1		stable	James Bowman	forth	16	16	spartan-6	James Brakef	333	6		1	117	##	14.7	0.80	1.0	280.2	vhdl	1	j1	yes	forth	N		64K	64K		16		2	2006	2010	excamera.com/sphin	uCode inst, dual port block RAM	32 deep data & return stacks
	Lutiac		custom	David Galloway, David	2 reg	16	NA	stratix-4	David Gallow	480	A	4		197			0.67	1.0	275.0	vhdl & verilog						Y		128	N	64	32	3		2010	Lutiac – Small Soft Pr	no inst RAM, instead microcode	no inst mem: large state machine, ~200 inst optimal
W	J1		stable	James Bowman	forth	16	16	kintex-7-3	James Brakef	387	6		4	133	##	14.7	0.80	1.0	274.6	verilog	1	j1	yes	forth	N		64K	64K		16		2	2006	2010	excamera.com/sphin	uCode inst, dual port block RAM	32 deep data & return stacks
X 1	diogenes	diogenes	beta	Fekknhifer	RISC	16	16	kintex-7-3	James Brakef	807	6		1	297	##	14.7	0.67	1.0	246.3	vhdl	11	cpu	yes	yes	N			1K					2008	2009		"student RISC system"	
A	nios2		proprietar	Altera	Nios II	32	32	arria-5	Altera	1355	A			280			1.13	1.0	232.5	not avail			yes	yes	opt		4G	4G	Y		32		2004		NIOS2 data sheets	fltg-pt, caches & MMU options	Nios II/f: fastest version
W 1	microcore		beta	Klaus Schleisiek	forth	32	8	kintex-7-3	James Brakef	644	6			149	##	14.7	1.00	1.0	231.3	vhdl	10	core	yes	asm	N	Y	2M	512K					2004		has several PDFs	indexing into return stack, auto inc/de	AKA uCore110
W 1	sayeh_proc	SAYEH educatio	stable	Alireza Haghdoost, Arr	RISC	16	16	kintex-7-3	James Brakef	479	6	1		164	##	14.7	0.67	1.0	229.7	verilog	13	Sayeh	yes				64K	64K		32			2008	2009	haghdoost.persiangig	simple RISC	
W 1	eric5		proprieta	enter-electronics.com	forth	9	8	cyclone-4-6	enter-electro	110	4	opt		60			0.42	1.0	229.1	not avail							512	1K		3-4			2007			25 MIPS: ERIC5xs, ERIC5Q	
W 1	gumnut		stable	Peter Ashenden	RISC	8	18	kintex-7-3	James Brakef	420	6			275	##	14.7	0.33	1.0	216.2	vhdl	20	gumnut-rtl	yes		N		256	4K	Y		8		2007			see Digital Design: An Embedded Syst	does not seem complete
W 1	dfp	dfp	stable	Ron Chapman	forth	16	8	kintex-7-3	James Brakef	298	6			192	##	14.7	0.33	1.0	213.2	vhdl	25	DataFlowPr	yes									2003	2009		8-bitter, generates a custom VHDL stack	machine, compiler is in Forth
X	popcorn		stable	Jeung Joon Lee	accum	8	8x	spartan-6-3	James Brakef	268	6			171	##	14.7	0.33	1.0	210.9	verilog	4	pc	yes		N		64K	64K	Y	43			2000			small 8 bit uP	
W 1	atlas_core	Atlas Processor	beta	Stephan Nolting	RISC	16	16	kintex-7-3	James Brakef	648	6	1	0	168	##	14.7	0.80	1.0	207.6	vhdl	8	ATLAS_CPU	yes	asm	N	Y	64K	64K	Y	80	8		2013	2014	opencore page	ARM thumb like inst set	non-MMU version
W	lem1_9	lem1_9	stable	James Brakefield	accum	1	9	spartan-6-3	James Brakef	42	6		1	217	##	14.5	0.04	1.0	207.0	vhdl	3	lem1_9min	yes	asm	N	Y	64	2K	N	8	64	1	2003	2009		very small, 2 pipe stage is faster with	"logic emulation machine"
	lem1_9	lem1_9	stable	James Brakefield	accum	1	9	cyclone-4	James shoul	23	4			116	##	13.1	0.04	1.0	201.5	vhdl	3	lem1_9min	yes	asm	N	Y	64	2K	N	8	64	1	2003	2009		very small, 2 pipe stage is faster with	"logic emulation machine"
A 1	pdp8verilog		stable	Brad Parker	PDP8	12	12	kintex-7-3	James Brakef	505	6			366	##	14.7	0.50	2.0	181.3	verilog	18	pdp8	yes	yes	N	N	32K	32K			8		2005	2010	PDP8 data sheets	boots & runs TSS/8 & Basic	www.heeltoe.com/download/pdp8/README.html
	lem1_9	lem1_9	stable	James Brakefield	accum	1	9	cyclone-2	James shoul	23	4			104	##	11.1	0.04	1.0	180.8	vhdl	3	lem1_9min	yes	asm	N	Y	64	2K	N	8	64	1	2003	2009		very small, 2 pipe stage is faster with	"logic emulation machine"
A	nios2		proprietar	Altera	Nios II	32	32	cyclone-5	Altera	1050	A			160			1.13	1.0	171.4	not avail			yes	yes	opt		4G	4G	Y		32		2004		NIOS2 data sheets	fltg-pt, caches & MMU options	Nios II/f: fastest version
A 1	picoblaze	picoblaze	stable	Ken Chapman	picoBlaze	8	18	Spartan-3-4	James Brakef	178	4			182	##	14.7	0.33	2.0	168.9	vhdl	1	kcsprm3	yes	asm	N	N	256	2K	Y				2003		picoblaze data sheets	2 clocks per inst	this is the original picoBlaze author
A	aeMB	aeMB	beta	Shawn Tan	uBlaze	32	32	kintex-7-3	James Brakef	1018	6	3		131	##	14.7	1.30	1.0	167.1	verilog	29	aeMB_core	yes	yes	N		4G	4G	Y				2004	2009	xilinx documentation	not 100% compatable	
B 1	pic_coonan		alpha	Tom Coonan	PIC16	8	14	kintex-7-3	James Brakef	328	6		1	165	##	14.7	0.33	1.0	166.1	verilog	7	piccpu	yes	yes	N	Y	256	4K	Y				1999		PIC16 data sheets		
W 1	b16		stable	Bernd Paysan	forth	16	5	spartan-6-3	James Brakef	554	6			134	##	14.7	0.67	1.0	161.7	verilog	1	b16	yes	yes	N								2002	2011	bernd-paysan.de/b16	two versions: one/15 source files, derived from c18	
A	nios2		proprietar	Altera	Nios II	32	32	arria-5	Altera	1045	A			250			0.64	1.0	152.1	not avail			yes	yes	opt		4G	4G	Y		32		2004		NIOS2 data sheets	fltg-pt, caches & MMU options	Nios II: balanced version
X 1	tisc	Tiny Instruction	beta	Vincent Crabtree	accum	8	8x	kintex-7-3	James Brakef	195	6			87	##	14.7	0.33	1.0	147.1	vhdl	1	TISC			N		256	1K	Y		2		2009	2009		minimal accumulator machine	
A	nios2		proprietar	Altera	Nios II	32	32	arria-2	Altera	1355	A			170			1.13	1.0	141.1	not avail			yes	yes	opt		4G	4G	Y		32		2004		NIOS2 data sheets	fltg-pt, caches & MMU options	Nios II/f: fastest version
W 1	dragonfly		beta	LEOX team	MISC	16	16	kintex-7-3	James Brakef	788	6			164	##	14.7	0.67	1.0	139.3	vhdl	6	dgf_core	yes		N		256	2K					2001		www.leox.org	unusual, uses FIFOs	
A 1	free_risc8		stable	Thomas Coonan	PIC16	8	14	kintex-7-3	James Brakef	355	6			142	##	14.7	0.33	1.0	132.2	verilog	8	cpu	yes	yes	N		256	4K	Y				2002	2011	PIC16 data sheets		
A 1	ae18	ae18	beta	Shawn Tan	PIC18	16	24	arria-2	James Brakef	1084	A	1		207	##	13.1	0.67	1.0	128.2	verilog	1	ae18_core		yes	N	Y	4K	1M					2003	2009	PIC18 data sheets	not 100% compatable	negative edge reset "clock"
W	atlas_core	Atlas Processor	beta	Stephan Nolting	RISC	16	16	spartan-6	James Brakef	643	6	1	0	103	##	14.7	0.80	1.0	127.9	vhdl	8	ATLAS_CPU	yes	asm	N	Y	64K	64K	Y	80	8		2013	2014	opencore page	ARM thumb like inst set	non-MMU version
W 1	open8_uris	Open8 uRISC	stable	Kirk Hays, Jshamlet	RISC	8	8	kintex-7-3	James Brakef	691	6	1		263	##	14.7	0.33	1.0	125.6	vhdl	9	Open8	yes	yes	N	Y	64K	64K	Y		8		2006	2013		accum & 8 regs, clone of Vautomation	uRISC processor, in use
W	atlas_core	Atlas Processor	beta	Stephan Nolting	RISC	16	16	arria-2	James Brakef	810	A	2	0	123	##	13.1	0.80	1.0	121.2	vhdl	8	ATLAS_CPU	yes	asm	N	Y	64K	64K	Y	80	8		2013	2014	opencore page	ARM thumb like inst set	non-MMU version
W	microcore		beta	Klaus Schleisiek	forth	32	8	spartan-6-3	James Brakef	591	6		1	71	##	14.7	1.00	1.0	120.1	vhdl	10	core	yes	asm	N	Y	2M	512K					2004		has several PDFs	indexing into return stack, auto inc/de	AKA uCore110
A 1	mips789	mips789	stable	Li Wei	MIPS	32	32	kintex-7-3	James Brakef	1432	6		1	171	##	14.7	1.00	1.0	119.1	verilog	10	mips_core	yes	yes	N		4G	4G	Y		32		2007	2009	MIPS data sheets		
A	nios2		proprietar	Altera	Nios II	32	32	stratix-5	Altera	445	A			340			0.15	1.0	114.6	not avail			yes	yes	N		4G	4G	Y		32		2004		NIOS2 data sheets	serial arithmetic	Nios II/e: minimum LUTs version
A	nios2		proprietar	Altera	Nios II	32	32	cyclone-5	Altera	785	A			140			0.64	1.0	113.4	not avail			yes	yes	opt		4G	4G	Y		32		2004		NIOS2 data sheets	fltg-pt, caches & MMU options	Nios II: balanced version
W 1	ensilica		proprieta	ensilica.com	eSi-3200	32		stratix-4	ensilica	1800	A			200			1.00	1.0	111.1	not avail			yes	yes			4G	4G			16	5			www.ensilica.com	verilog source included with license	10 addressing modes
W	hive	hive	stable	Eric Wallin	4-8 stack	32	16	cyclone-3	Eric Wallin	1800	4	4	3	200		13.0	1.00	1.0	111.1	verilog			yes		N				N	40	10	8	2013	2014		4-8 symetrical stacks, eight threads via pipeline barrel	
W	dfp	dfp	stable	Ron Chapman	forth	8	Y	spartan-6-3	James Brakef	334	6			112	##	14.7	0.33	1.0	110.7	vhdl	25	DataFlowPr	yes									2003	2009		8-bitter, generates a custom VHDL stack	machine, compiler is in Forth
A 1	pacoBlaze		mature	Pablo Kocik	picoBlaze	8	18	spartan-3	Pablo Kocik	177	4		1	117			0.33	2.0	109.1	verilog	18	pacoblaze	yes	asm	N		256	2K	Y	57		2		2006	bleyer.org/pacoblaze	3 versions, behavioral coding	
A 1	ion	Ion MIPS compa	mature	Jose Ruiz	MIPS	32	32	kintex-7-3	James Brakef	1533	6			163	##	14.7	1.00	1.0	106.0	vhdl	12	mips_soc	yes	yes	N		4G	4G	Y		32		2011	2014		MIPS R3000 clone	
X 1	jam		stable	Johan Thelin etal	RISC	32	32	kintex-7-3	James Brakef	1369	6			143	##	14.7	1.00	1.0	104.2	vhdl	17	cpu	yes		N	Y	128K	128K			32	5	2002			serial multiply & divide	
X 1	hpc-16	HPC-16	beta	Umair Siddiqui	RISC	16	16	kintex-7-3	James Brakef	875	6			136	##	14.7	0.67	1.0	104.2	vhdl	20	cpu	yes	asm	N		64K	64K			16		2005	2009			
A	nios2		proprietar	Altera	Nios II	32	32	arria-2	Altera	1045	A			170			0.64	1.0	103.4	not avail			yes	yes	opt		4G	4G	Y		32		2004		NIOS2 data sheets	fltg-pt, caches & MMU options	Nios II: balanced version
X 1	myrisc1	myRISC1	stable	Muza Byte	RISC	8	8	cyclone-2	Muza	Altera	185	A		1	57			1.0	101.8	verilog		myRISC1	yes		N	Y	256	256	Y	16	4		2011	2011		Verilog source included in PDF file	LPM macros
X	tisc	Tiny Instruction	beta	Vincent Crabtree	accum	8	8x	spartan-6-3	James Brakef	198	6			60	##	14.7	0.33	1.0	99.5	vhdl	1	TISC			N		256	1K	Y		2		2009	2009		minimal accumulator machine	
W	lem1_9	lem1_9	stable	James Brakefield	accum	1	9	spartan-3-5	James Brakef	55	4		1	136	##	14.5	0.04	1.0	98.7	vhdl	3	lem1_9min	yes	asm	N	Y	64	2K	N	8	64	1	2003	2009		very small, 2 pipe stage is faster with	"logic emulation machine"
W	ensilica		proprieta	ensilica.com	eSi-1600	16		virtex-5	ensilica	1100	6			160			0.67	1.0	97.5	not avail			yes	yes	N		64K	64K			16				www.ensilica.com	verilog source included with license	10 addressing modes
A 1	ucore	Ucore	stable	Whitewill	MIPS	32	32	kintex-7-3	James Brakef	2469	6		1	231	##	14.7	1.00	1.0	93.5	verilog	25	ucore	yes	yes	N		4G	4G	Y		32	6	2005	2010	MIPS data sheets	MMU & caches	
W 1	altor32_lite	AltOr32	stable	Ultra Embedded	OpenRISC	32	32	arria-2	James Brakef	1809	A			161	##	13.1	1.00	1.0	88.8	system v	8	altor32		yes	N		4G	4G	Y				2012	2014	OpenRISC 1000	simplified OpenRISC 1000	LPMs & systemVerilog
A 1	openfire2	OpenFIRE	beta	Antonio Anton	uBlaze	32	32	kintex-7-3	James Brakef	1201	6	3	2	105	##	14.7	1.00	1.0	87.4	verilog	27	openfire_sc	yes	yes	N	N	4G	4G	Y		32		2007	2012	uBlaze data sheets	"FPGA Proven"	derived from Stephen Craven's OpenFire
A	nios2		proprietar	Altera	Nios II	32	32	cyclone-4-6	Altera	2035	A			160			1.13	1.0	87.2	not avail			yes	yes	opt		4G	4G	Y		32		2004		NIOS2 data sheets	fltg-pt, caches & MMU options	Nios II/f: fastest version
W 1	jane_nn		stable	Suresh Devanathan	RISC	4	8	kintex-7-3	James Brakef	723	6			178	##	14.7	0.33	1.0	81.4	vhdl	3	Processor	yes							27	16		2002			neural network microprocessor, specialized registers	
W 1	dcpu16		beta	Marcus Persson , Shaw	RISC	16	16	kintex-7-3	James Brakef	662	6	1		318	##	14.7	0.67	4.0	80.4	vhdl & w	5	dcpu16_cpu	yes	asm	N	N	64K	64K	N	37	8		2009	2012	https://github.com/d	for the 0X10c game	4+ addressing modes, 4 & 5-bit reg /modefields
A	pdp8verilog		stable	Brad Parker	PDP8	12	12	spartan-6-3	James Brakef	509	6			162	##	14.7	0.50	2.0	79.5	verilog	18	pdp8	yes	yes	N	N	32K	32K			8		2005	2010	PDP8 data sheets	boots & runs TSS/8 & Basic	www.heeltoe.com/download/pdp8/README.html
W 1	atlas_2K	Atlas Processor	beta	Stephan Nolting	RISC	16	16	kintex-7-3	James Brakef	1512	6	1	5	149	##	14.7	0.80	1.0	79.1	vhdl	19	ATLAS_2K	yes	asm	N	Y	64K	64K	M	80	8		2013	2014	opencore page	ARM thumb like inst set	has MMU & full SOC features
A 1	storm_core	Storm Core (ARM	beta	Stephan Nolting	ARM7	32	32	kintex-7-3	James Brakef	2312	6	3		179	##	14.7	1.00	1.0	77.4	vhdl	16	CORE	yes	yes	N		4G	4G	Y		32	8	2011	2014		I & D caches not compiled	
A 1	aspida	ASPIDA DLX cor	stable	Sotiriou	DLX	32	32	kintex-7-3	James Brakef	3586	6			257	##	14.7	1.00	1.0	71.7	verilog	10	DLX top	yes	yes			4G	4G					2002	2009	Knuth DLX		compiled sync version
A	nios2		proprietar	Altera	Nios II	32	32	cyclone-5	Altera	420	A			200			0.15	1.0	71.4	not avail			yes	yes	N		4G	4G	Y		32		2004		NIOS2 data sheets	serial arithmetic	Nios II/e: minimum LUTs version
A	ae18	ae18	beta	Shawn Tan	PIC18	16	24	virtex-6-3	James Brakef	1133	6	1		117	##	14.7	0.67	1.0	69.1	verilog	1	ae18_core		yes	N	Y	4K	1M					2003	2009	PIC18 data sheets	not 100% compatable	negative edge reset "clock"
A 1	navre	Navre AVR clone	stable	Sebastien Bourdeaudu	AVR	8	16	kintex-7-3	James Brakef	990	6			207	##	14.7	0.33	1.0	69.0	verilog	1	softusb_na	yes	yes	N		64K	64K	Y		32	2	2010

	_dp_cores_test	opencores name	status	author	style / clone	data size	inst size	FPGA	reporter	comment	LUTs ALM	LUT	multfs	blk ram	F max	date	tool ver	MIPS /clk	clks/ inst	KIPS /LUT	src code	# src files	top file	doc	tool chain	fltg pt	Hard	max data	max inst	byte adrs	# inst	# reg	pipe	start year	last revis	reference	note worthy	comments
W		atlas_2K	Atlas Processor	beta	Stephan Nolting	RISC	16	16	spartan-6-3	James Brakef	1545	6	1	10	100	##	14.7	0.80	1.0	51.5	vhdl	19	ATLAS_2K_t	yes	asm	N	Y	64K	64K	M	80	8		2013	2014	opencore page	ARM thumb like inst set	has MMU & full SOC features
A	1	avrtinyx61c	avrtinyx61core	beta	Andreas Hilvarsson	AVR	8	16	kintex-7-3	James Brakef	1243	6			194	##	14.7	0.33	1.0	51.5	vhdl	1	mcu_core		yes	N		64K	128K	Y		32		2008	2009	AVR data sheets		
X	1	cole_c16		beta	Cole Design & Develop	RISC	16	16	spartan-6-3	James Brakef	554	6			298	##	14.7	0.67	7.0	51.4	vhdl	1	core	yes	asm	N		64K	64K	N	20	8		2002	2012		(7) clks per inst, complete SOC	for teaching
X	1	eco32	SOC:ECO32	stable	Hellwing Geisse	RISC	32	32	kintex-7-3	James Brakef	2210	6		1	160		14.7	1.00	1.5	48.1	verilog	23	cpu	yes	yes	N		512M	256M	Y	61	32		2003	2014		MIPS like, slow mul & div	
X	1	avr_hp	avr_hp	stable	Strauch Tobias	AVR	8	16	kintex-7-3	James 2 slot	1554	6			223	##	14.7	0.33	1.0	47.4	vhdl	10	avr_core_cr	some	yes	N		64K	128K	Y		32		2010	2010	AVR data sheets	hyper pipelined (eg barrel) AVR	
X	1	qrisc32	qrisc32 wishbon	alpha	Viacheslav	RISC	32	32	arria-2	James Brakef	3075	A	4		144	##	13.1	1.00	1.0	46.9	system v	8	qrisc32	yes	yes	N		4G	4G	Y		32	4	2010	2011		for PhD thesis	
A		ae18	ae18	beta	Shawn Tan	PIC18	16	24	spartan-6-3	James Brakef	1176	6	1		81	##	14.7	0.67	1.0	46.2	verilog	1	ae18_core		yes	N	Y	4K	1M					2003	2009	PIC18 data sheets	not 100% compatable	negative edge reset "clock"
A		navre	Navre AVR clone	stable	Sebastien Bourdeaudu	AVR	8	16	arria-2	James Brakef	1126	A			154	##	13.1	0.33	1.0	45.1	verilog	1	softusb_nav	yes	yes	N		64K	64K	Y		32	2	2010	2013	AVR data sheets	AVR clone, part of www.milkymist.org	
A		storm_core	Storm Core (ARM	beta	Stephan Nolting	ARM7	32	32	kintex-7-3	James Brakef	3514	6	3	4	157	##	14.7	1.00	1.0	44.8	vhdl	16	STORM_TOI	yes	yes	N	M	4G	4G	Y		32	8	2011	2014		I & D caches	
A		avr_hp	avr_hp	stable	Strauch Tobias	AVR	8	16	kintex-7-3	James 4 slot	2054	6			278	##	14.7	0.33	1.0	44.7	vhdl	10	avr_core_cr	some	yes	N		64K	128K	Y		32		2010	2010	AVR data sheets	hyper pipelined (eg barrel) AVR	
A		avr_hp	avr_hp	stable	Strauch Tobias	AVR	8	16	kintex-7-3	James 3 slot	1812	6			243	##	14.7	0.33	1.0	44.2	vhdl	10	avr_core_cr	some	yes	N		64K	128K	Y		32		2010	2010	AVR data sheets	hyper pipelined (eg barrel) AVR	
X	1	bobcat		beta	Stan Drey		16	24	kintex-7-3	James Brakef	1622	6	1		107	##	14.7	0.67	1.0	44.0	vhdl							64K	64K						1998		appears to be a DSP	
A		navre	Navre AVR clone	stable	Sebastien Bourdeaudu	AVR	8	16	cyclone-5	James Brakef	783	A			103	##	13.1	0.33	1.0	43.6	verilog	1	softusb_nav	yes	yes	N		64K	64K	Y		32	2	2010	2013	AVR data sheets	AVR clone, part of www.milkymist.org	
A		nios2		proprietar	Altera	Nios II	32	32	cyclone-4-6	Altera	1915	4			130			0.64	1.0	43.2	not avail				yes	opt		4G	4G	Y		32		2004		NIOS2 data sheets	fltg-pt, caches & MMU options	Nios II: balanced version
A		light8080	Lightweight 808	stable	Jose Ruiz, Moti Litoche	8080	8	8x	spartan-6	James Brakef	148	6		3	172	##	14.7	0.33	9.0	42.7	verilog	5	light8080	yes	yes	N	N	64K	64K	Y				2007	2012	8080 data sheets	targeted to area, bare core	typically 9 clocks per inst, .04=.33/9
X	1	micro8a		beta	John Kent	accum	8	16	kintex-7	James Brakef	531	6			204	##	14.7	0.33	3.0	42.3	vhdl	11	Micro8	yes		N	N	2K	2K	Y				2002	2002	members.optushome	derived from Tim Boscke's mcpu, not perfected	
A	1	t65	T65 CPU	stable	Daniel Wallner	6502	8	8x	kintex-7-3	James Brakef	575	6			291	##	14.7	0.33	4.0	41.7	vhdl	7	T65	yes	yes	N	N	64K	64K	Y				2002	2010	6502 data sheets	6502, 65C02 & 65C816; wide use	
W	1	blue	16-bit CPU Blue	stable	Al Williams	accum	16	16	spartan-3-5	James remov	1025	4			63	##	14.7	0.67	1.0	41.1	verilog	16	topbox	web		N		4K	4K	N	16	2		2009	2010	Caxton Foster's Blue derivative	http://www.youtube.com/watch?v=dt4zezZP8w8	
A		ae18	ae18	beta	Shawn Tan	PIC18	16	24	kintex-7-3	James Brakef	1131	6	1		68	##	14.7	0.67	1.0	40.5	verilog	1	ae18_core	yes	yes	N	Y	4K	1M					2003	2009	PIC18 data sheets	not 100% compatable	negative edge reset "clock"
A	1	minimips	miniMIPS	stable	Poppy etal	MIPS	32	32	kintex-7-3	James Brakef	2939	6	8		118	##	14.7	1.00	1.0	40.1	vhdl	12	minimips	yes	yes	N		4G	4G	Y		32	5			MIPS I		
W	1	ba22		proprieta	CAST Inc	RISC	32	16x	spartan-6	CAST Inc	1800	6		32	72			1.00	1.0	40.0	not avail							4G	4G			32				www.cast-inc.com		
W		altor32	AltOr32	stable	Ultra Embedded	OpenRISC	32	32	arria-2	James Brakef	2395	A		6	96	##	13.1	1.00	1.0	39.9	system v	19	altor32		yes	N		4G	4G	Y				2012	2014	OpenRISC 1000	simplified OpenRISC 1000	LPMs & systemVerilog
A	1	plasma	Plasma most MI	stable	Steve Rhoads	MIPS	32	32	kintex-7-3	James Brakef	2462	6		3	97	##	14.7	1.00	1.0	39.5	vhdl	22	plasma	yes	yes	N		4G	4G	Y		32		2001	2013	MIPS data sheets	wide outside use, opencores page has list of related publications	
X		eco32	SOC:ECO32	stable	Hellwing Geisse	RISC	32	32	atrix-7-3	James Brakef	2107	6		1	121		14.7	1.00	1.5	38.4	verilog	23	cpu	yes	yes	N		512M	256M	Y	61	32		2003	2014		MIPS like, slow mul & div	
W	1	risc5		beta	Niklaus Wirth	RISC	32	32	kintex-7-3	James Brakef	2441	6	4	1	92	##	14.7	1.00	1.0	37.8	verilog	8	RISC5	yes	yes	Y		4G	4G			16		2013			minimalist Wirth, part of Project Oberon	32x32 multiplier
A	1	pdp8	PDP-8 Processor	alpha	Joe Manojlovick, Rob D	PDP8	12	12	kintex-7-3	James Brakef	1219	6	1		183	##	14.7	0.50	2.0	37.5	vhdl	55	cpu	yes	yes	N	N	32K	32K			8		2012	2013	PDP8 data sheets	Boots OS/8, runs apps, several variants	
A		navre	Navre AVR clone	stable	Sebastien Bourdeaudu	AVR	8	16	spartan-6-3	James Brakef	1038	6			116	##	14.7	0.33	1.0	36.9	verilog	1	softusb_nav	yes	yes	N		64K	64K	Y		32	2	2010	2013	AVR data sheets	AVR clone, part of www.milkymist.org	
A	1	mipsr2000	mipsr2000	stable	Lazaridis Dimitris	MIPS	32	32	kintex-7-3	James Brakef	1971	6	4	6	71	##	14.7	1.00	1.0	36.2	vhdl	35	Dm	yes	yes	N		4G	4G	Y		32	5	2012	2013	MIPS data sheets	course project	
A		avr_hp	avr_hp	stable	Strauch Tobias	AVR	8	16	kintex-7-3	James 1 slot	1199	6			127	##	14.7	0.33	1.0	35.0	vhdl	9	avr_core	some	yes	N		64K	128K	Y		32		2010	2010	AVR data sheets	hyper pipelined (eg barrel) AVR	
A		light8080	Lightweight 808	stable	Jose Ruiz, Moti Litoche	8080	8	8x	spartan-6	James Brakef	150	6		3	142	##	14.7	0.33	9.0	34.6	verilog	5	light8080	yes	yes	N	N	64K	64K	Y				2007	2012	8080 data sheets	targeted to area, bare core	typically 9 clocks per inst, .04=.33/9
W	1	jop	JOP a Java Optim	stable	Martin Schoeberl etal	forth	16	16	cyclone-1	Martin Schoe	2000	4			100		10	0.67	1.0	33.5	vhdl	11	core	yes	yes	N		256K	256K					2004	2014		opencores download is empty	https://github.com/jop-devel/jop
W		latticemicro32		stable	Yann Siommeau, Mich	RISC	32	32	spartan-6	James Brakef	2093	6	3	15	85	##	14.7	0.80	1.0	32.4	verilog	24	lm32_cpu	yes	yes	N		4G	4G	Y		32		2006	2012	en.wikipedia.org/wiki	optional data & inst caches	
W		risc5		beta	Niklaus Wirth	RISC	32	32	arria-2	James Brakef	2362	A		3	73	##	13.1	1.00	1.0	31.0	verilog	8	RISC5	yes	yes	Y		4G	4G			16		2013			minimalist Wirth, part of Project Oberon	32x32 multiplier
A		openfire2	OpenFIRE	beta	Antonio Anton	uBlaze	32	32	spartan-3-5	James Brakef	1352	4	3	6	39	##	14.7	1.00	1.0	28.8	verilog	27	openfire_sc	yes	yes	N	N	4G	4G	Y		32		2007	2012	uBlaze data sheets	"FPGA Proven"	derived from Stephen Craven's OpenFire
W		atlas_2K	Atlas Processor	beta	Stephan Nolting	RISC	16	16	cyclone-4-6	Stephan Nolt	2730	4	1	32	98	##	13.1	0.80	1.0	28.6	vhdl	19	ATLAS_2K_t	yes	asm	N	Y	64K	64K	M	80	8		2013	2014	opencore page	ARM thumb like inst set	has MMU & full SOC features
X		eco32	SOC:ECO32	stable	Hellwing Geisse	RISC	32	32	arria-2	James Brakef	2711	A			116	##	13.1	1.00	1.5	28.6	verilog	23	cpu	yes	yes	N		512M	256M	Y	61	32		2003	2014		MIPS like, slow mul & div	
A	1	openmsp43	openMSP430	stable	Oliver Girard	msp430	16	16x	stratix-3-2	Oliver Girard	1147	A	1		98			0.67	2.0	28.5	verilog	30	openMSP43	yes	yes	N	N	64K	64K	Y		16		2009	2014	msp430 data sheets	performance spreadsheet	
W		atlas_2K	Atlas Processor	beta	Stephan Nolting	RISC	16	16	spartan-3a-	Stephan Nolt	2434	4	1	9	85	##	14.7	0.80	1.0	28.0	vhdl	19	ATLAS_2K_t	yes	asm	N	Y	64K	64K	M	80	8		2013	2014	opencore page	ARM thumb like inst set	has MMU & full SOC features
X		tinycpu	TinyCPU	alpha	Jordan Earls	RISC	8	16	kintex-7-3	James bit ler	1182	6			200	##	14.7	0.33	2.0	28.0	vhdl	10	top		asm	N	N	64K	64K			16		2012	2012			
A		openmsp43	openMSP430	stable	Oliver Girard	msp430	16	16x	virtex-6-3	Oliver Girard	1387	6	1		116			0.67	2.0	27.9	verilog	30	openMSP43	yes	yes	N	N	64K	64K	Y		16		2009	2014	msp430 data sheets	performance spreadsheet	
W	1	natalius_8b	Natalius 8 bit RIS	beta	Fabio Gruber	RISC	8	12	kintex-7-3	James Brakef	256	6		1	175	##	14.7	0.11	3.0	27.7	verilog	12	natalius_pro	yes	asm	N	Y	256	2K	Y	29	8		2012	2012		return stack & register file	3 clocks/inst
X		eco32	SOC:ECO32	stable	Hellwing Geisse	RISC	32	32	spartan-6-3	James Brakef	2271	6		1	92		14.7	1.00	1.5	27.0	verilog	23	cpu	yes	yes	N		512M	256M	Y	61	32		2003	2014		MIPS like, slow mul & div	
		micro16b		beta	John Kent	accum	16	16	spartan-3E-	James Brakef	467	4		3	76	##	14.7	0.33	2.0	26.9	vhdl	13	Micro16b_t	yes	asm	N	N	64K	4K	Y	8			2002	2008	members.optushome	SOC version, very limited inst set	MIPS/clk adj'd, 2 clks/inst
A	1	rtf8088	rtf8088	planning	Robert Finch	8086	8x	8x	kintex-7-3	James Brakef	4514	6	4		174	##	14.7	0.67	1.0	25.8	verilog	57	rtf8088	yes	yes	N	N	1M	1M	Y				2012	2013	x86 data sheets		
A		t65	T65 CPU	stable	Daniel Wallner	6502	8	8x	arria-2	James Brakef	617	A			190	##	13.1	0.33	4.0	25.4	vhdl	7	T65	yes	yes	N	N	64K	64K	Y				2002	2010	6502 data sheets	6502, 65C02 & 65C816; wide use	
W		atlas_2K	Atlas Processor	beta	Stephan Nolting	RISC	16	16	spartan-3a-	James Brakef	2450	4	1	9	76	##	14.7	0.80	1.0	24.9	vhdl	19	ATLAS_2K_t	yes	asm	N	Y	64K	64K	M	80	8		2013	2014	opencore page	ARM thumb like inst set	has MMU & full SOC features
A	1	free6502		stable	David Kessner	6502	8	8x	kintex-7-3	James Brakef	646	6			193	##	14.7	0.33	4.0	24.6	vhdl	5	free6502	yes	yes	N	N	64K	64K	Y				1999	2000	6502 data sheets	microcoded	
W	1	nige_machine		stable	Andrew Read	forth	32	8	kintex-7-3	James Brakef	5033	6	8	33	123	##	14.7	1.00	1.0	24.5	vhdl	29	Board	yes	yes	N		16M	16M		512	512			2014			standalone Forth system	
W		risc5		beta	Niklaus Wirth	RISC	32	32	spartan-6-3	James Brakef	2283	6	4	1	55	##	14.7	1.00	1.0	24.3	verilog	8	RISC5	yes	yes	Y		4G	4G			16		2013			minimalist Wirth, part of Project Oberon	32x32 multiplier
A		nios2		proprietar	Altera	Nios II	32	32	cyclone-4-6	Altera	1080	4			170			0.15	1.0	23.6	not avail				yes	yes		4G	4G	Y		32		2004		NIOS2 data sheets	serial arithmetic	Nios II/e: minimum LUTs version
		copyblaze	copyBlaze	stable	Abdallah Ellbrahimi	picoBlaze	8	18	spartan-6-3	James missir	619	6			86	##	14.7	0.33	2.0	22.8	vhdl	16	cp_copyblaz	yes	asm	N		256	2K	Y				2011	2013	microBlaze data shee	wishbone extras	does not infer RAM for registers
W	1	minsoc	minsoc	stable	Raul Fajardo etal	OpenRISC	32	32	kintex-7-3	James Brakef	4945	6	4	8	107	##	14.7	1.00	1.0	21.7	verilog	88	or1200_top	yes	yes	Y	M	4G	4G	Y		32		2009	2013	www.minsoc.com	minimal OR1200, vendor neutral, has caches	
A	1	aquarius	aquarius	stable	Thorn Corbett	SuperH2	32	16	kintex-7-3	James Brakef	3925	6	2		86	##	14.7	1.00	1.0	21.6	verilog	21	top		yes	N		4G	4G	Y		16		2003	2009	SuperH data sheets		
A		navre	Navre AVR clone	stable	Sebastien Bourdeaudu	AVR	8	16	cyclone-4-6	James Brakef	1561	4			102	##	13.1	0.33	1.0	21.5	verilog	1	softusb_nav	yes	yes	N		64K	64K	Y		32	2	2010	2013	AVR data sheets	AVR clone, part of www.milkymist.org	
A	1	mips32r1	MIPS32 Release	stable	Grant Ayers	MIPS	32	32	arria-2	James Brakef	3716	A	8		79	##	13.1	1.00	1.0	21.3	verilog	20	processor	yes	yes	N		4G	4G	Y		32		2012	2014	MIPS data sheets	Harvard arch	
A	1	m16c5x	M16C5x	mature	Michael Morris	PIC16	8	14	spartan-3-4	Michael Mor	1265	4		3	81			0.33	1.0	21.1	verilog	3	m16C5x	yes	yes	N	Y	256	4K	Y				2013	2014	PIC16 data sheets	SOC LUT count	was P16C5X, name could be in flux
W		atlas_2K	Atlas Processor	beta	Stephan Nolting	RISC	16	16	cyclone-2	James Brakef	2711	4	1	64	71	##	11.1	0.80	1.0	21.0	vhdl	19	ATLAS_2K_t	yes	asm	N	Y	64K	64K	M	80	8		2013	2014	opencore page	ARM thumb like inst set	has MMU & full SOC features
B	1	68hc05	68hc05	stable	Ulrich Riedel	6805	8	8x	kintex-7-3	James Brakef	1225	6			300	##	14.7	0.33	4.0	20.2	vhdl	1	6805		yes	N	N	64K	64K	Y				2007	2009	6805 data sheets		
A	1	system05	SOC:system05	beta	John Kent	6805	8	8x	kintex-7-3	James Brakef	834	6			204	##	14.7	0.33	4.0	20.2	vhdl	10	System05	yes	yes	N	N	64K	64K	Y				2003	2009	6805 data sheets		
A	1	avr_core	avr core	stable	Rusian Lepetenok	AVR	8	16	kintex-7-3	James Brakef	2135	6			127	##	14.7	0.33	1.0	19.7	verilog	15	avr_core	yes	yes	N		64K	128K	Y		32		2002	2012	AVR data sheets	VHDL core included	
B		m65		stable	Naohiko Shimizu	6502	8	8x	arria-2	James Brakef	483	A			110	##	13.1	0.33	4.0	18.8	sfl & TDI	8	m65cpu	yes	yes	N	N	4K	4K	Y				2001	2002	6502 data sheets		
A		mips32r1	MIPS32 Release	stable	Grant Ayers	MIPS	32	32	kintex-7-3	James Brakef	4822	6	8		90	##	14.7	1.00	1.0	18.6	verilog	20	processor	yes	yes	N		4G	4G	Y		32		2012	2014	MIPS data sheets	Harvard arch	
A	1	ag_6502	ag_6502 soft co	beta	Oleg Odintsov	6502	8	8x	kintex-7-3	James Brakef	824	6	0	0	176	##	14.7	0.33	4.0	17.7	verilog	2	ag_6502		yes	N	N	64K	64K	Y				2012	2012	6502 data sheets	verilog code generation, "phase level accurate"	
A		light8080	Lightweight 808	stable	Jose Ruiz, Moti Litoche	8080	8	8x	spartan-3-5	Jose Ruiz	209	4		1	100		9.1	0.33	9.0	17.5	vhdl	5	light8080	yes	yes	N	N	64K	64K	Y				2007	2012	8080 data sheets	targeted to speed, bare core	typically 9 clocks per inst, .04=.33/9
A	1	pdp11-34verilog		stable	Brad Parker	PDP11	16	16x	arria-2	James Brakef	2532	A			126	##	13.1	0.67	2.0	16.7	verilog	24	pdp11	yes	yes	N	N	64K	64K			8		2009		PDP11 data sheets	boots & runs RT-11, EIS inst & MMU	www.heeltoe.com/download/pdp11/README.html
A	1	tv80	TV80	mature	Guy Hutchison, Howar	Z80	8	8x	kintex-7-3	James Brakef	1207	6			182	##	14.7	0.33	3.0	16.6	verilog	6	tv80n	yes	yes	N	N	64K	64K	Y				2004	2012	z80 data sheets	derived from Daniel Wallner's T80, ASIC implementations	
A		pdp11-34verilog		stable	Brad Parker	PDP11	16	16x	kintex-7-3	James Brakef	3089	6			153	##	14.7	0.67	2.0	16.6	verilog	24	pdp11	yes	yes	N	N	64K	64K			8		2009		PDP11 data sheets	boots & runs RT-11, EIS inst & MMU	www.heeltoe.com/download/pdp11/README.html
A		navre	Navre AVR clone	stable	Sebastien Bourdeaudu	AVR	8	16	cyclone-2	James Brakef	1502	4			73	##	13.1	0.33	1.0	15.9	verilog	1	softusb_nav	yes	yes	N		64K	64K	Y		32	2	2010	2013	AVR data sheets	AVR clone, part of www.milkymist.org	
A		openmsp43	openMSP430	stable	Oliver Girard	msp430	16	16x	spartan-6-4	Oliver Girard	1424	6	1		68			0.67	2.0	15.9	verilog	30	openMSP43	yes	yes	N	N	64K	64K	Y		16		2009	2014	msp430 data sheets	performance spreadsheet	
A		storm_core	Storm Core (ARM	beta	Stephan Nolting	ARM7	32	32	cyclone-2-6	Stephan Nolt	11469	4	3	75	179			1.00	1.0	15.6	vhdl	16	STORM_TOI	yes	yes	N	M	4G	4G	Y		32	8	2011	2014		I & D caches	
W		risc5		beta	Niklaus Wirth	RISC	32	32	cyclone-4	James Brakef	3503	4		1	54	##	13.1	1.00	1.0	15.4	verilog	8	RISC5	yes	yes	Y		4G	4G			16		2013			minimalist Wirth, part of Project Oberon	32x32 multiplier ?
A		pdp8	PDP-8 Processor	alpha	Joe Manojlovick, Rob D	PDP8	12	12	spartan-6-3	James Brakef	1332	6	1		81	##	14.7	0.50	2.0	15.1	vhdl	55	cpu	yes	yes	N	N	32K	32K			8		2012	2013	PDP8 data sheets	Boots OS/8, runs apps, several variants	
A		t65	T65 CPU	stable	Daniel Wallner	6502	8	8x	spartan-6-3	James Brakef	725	6			128	##	14.7	0.33	4.0	14.5	vhdl	7	T65	yes	yes	N	N	64K	64K	Y				2002	2010	6502 data sheets	6502, 65C02 & 65C816; wide use	
A	1	pdp8l	Minimal PDP8/L	beta	Ian Schofield	PDP8	12	12	cyclone-3	James Brakef	1088	4		48	63	##	14.7	0.50	2.0	14.4	vhdl	11	top	yes	yes	N	N	4K	4K					2013		PDP8 data sheets		
A	1	v1_coldfire		stable	IPextreme	68000	16	16x	cyclone-3	freescale	5000	4			80			0.89	1.0	14.2				yes	yes	N	N	4G	4G	Y		16		2008		68000 data sheets	free for Cyclone III	
A		storm_core	Storm Core (ARM	beta	Stephan Nolting	ARM7	32	32	cyclone-4-6	Stephan Nolt	11518	4	3	67.5	157			1.00	1.0	13.7	vhdl	16	STORM_TOI	yes	yes	N	M	4G	4G	Y		32	8	2011	2014		I & D caches	
A	1	next186	Next 80186 proc	stable	Nicolae Dumitrache	8086	16	8x	arria-2	James Brakef	1966	A	2		77	##	13.1	0.67	2.0	13.1	verilog	4	Next186_CP	yes	yes	N	N	1M	1M	Y				2012	2013	x86 data sheets	boots DOS	
W	1	xr16		stable	Jan Gray	RISC	16	16	kintex-7-3	James Brakef	371	6			7	##	14.7	0.67	1.0	13.0	verilog	12	xsoc	yes		N		64K	64K			16		1999	2001		handcrafted FPGA layout & instructio	source code written for simulation
A	1	t80	T80 cpu	stable	Daniel Wallner	Z80	8	8x	kintex-7-3	James Z80 m	1389	6			163	##	14.7	0.33	3.0	12.9	vhdl	5	T80a	yes	yes	N	N	64K	64K	Y				2002	2011	z80 data sheets	Z80 & 8080 inst sets, several usage	
A	1	dalton_8051		stable	Tony Givargis	8051	8	8x	kintex-7-3	James Brakef	2725	6	1	1	105	##	14.7	0.33	1.0	12.7	vhdl	7	i8051_all	yes	yes	N	N	64K	64K	Y				1999	2003	8051 data sheets	ASIC	www.cs.ucr.edu/~dalton/
A		next186	Next 80186 proc	stable	Nicolae Dumitrache	8086	16	8x	kintex-7-3	James Brakef	2500	6	1		94	##	14.7	0.67	2.0	12.6	verilog	4	Next186_CP	yes	yes	N	N	1M	1M	Y				2012	2013	x86 data sheets	boots DOS	
A	1	zet86	Zet The x86 (IA-3	alpha	Zeus Marmolejo	8086	8	8x	kintex-7-3	James Brakef	3642	6	1		68	##	14.7	0.67	1.0	12.5	verilog	32	fpga_zet_tc	yes	yes	N	N	1M	1M	Y				2008	2014	x86 data sheets	equivalent to 80186, boots MS-DOS	zet.aluzina.org/index.php/Zet_processor
X		eco32	SOC:ECO32	stable	Hellwing Geisse	RISC	32	32	spartan-3-5	James Brakef	3034	4		2	55		14.7	1.00	1.5	12.0	verilog	23	cpu	yes	yes	N		512M	256M	Y	61	32		2003	2014		MIPS like, slow mul & div	
W		risc5		beta	Niklaus Wirth	RISC	32	32	spartan-3-5	James Brakef	3005	4	4	1	34	##	14.7	1.00	1.0	11.4	verilog	8	RISC5	yes	yes	Y		4G	4G			16		2013			minimalist Wirth, part of Project Oberon	32x32 multiplier
A		gup	HC11 Compatibl	stable	Kevin Phillipson	68HC11	8	8x	arria-2	James Brakef	925	A	1	1	127	##	13.1	0.33	4.0	11.3	vhdl	25	gator_uprog	yes	yes	N	N	64K	64K	Y				2008	2009	6811 data sheets	68HC11 compatible	top level is schematic
A		free6502		stable	David Kessner	6502	8	8x	spartan-6-3	James Brakef	663	6			89	##	14.7	0.33	4.0	11.1	vhdl	5	free6502	yes	yes	N	N	64K	64K	Y				1999	2000	6502 data sheets	microcoded	
A	1	next280	NextZ80	stable	Nicolae Dumitrache	Z80	8	8x	kintex-7-3	James Brakef	1064	6			106	##	14.7	0.33	3.0	10.9	verilog	3	Next280CPU	yes	yes	N	N	64K	64K	Y				2011	2014	z80 data sheets		
A		t65	T65 CPU	stable	Daniel Wallner	6502	8	8x	cyclone-4	James Brakef	831	4			110	##	13.1	0.33	4.0	10.9	vhdl	7	T65	yes	yes	N	N	64K	64K	Y				2002	2010	6502 data sheets	6502, 65C02 & 65C816; wide use	
A		next186	Next 80186 proc	stable	Nicolae Dumitrache	8086	16	8x	cyclone-5	James Brakef	1355	A	1		44	##	13.1	0.67	2.0	10.9	verilog	4	Next186_CP	yes	yes	N	N	1M	1M	Y				2012	2013	x86 data sheets	boots DOS	did not infer multiplier
A		tv80	TV80	mature	Guy Hutchison, Howar	Z80	8	8x	arria-2	James Brakef	1413	A			139	##	13.1	0.33	3.0	10.9	verilog	6	tv80n	yes	yes	N	N	64K	64K	Y				2004	2012	z80 data sheets	derived from Daniel Wallner's T80, ASIC implementations	
A	1	ao68000	ao68000	beta	Aleksander Osman	68000	16	16x	arria-2	James Brakef	3479	A		6	169	##	13.1	0.67	3.0	10.8	verilog	1

		_uP_cores _test f...	opencores name	status	author	style / clone	data size	inst size	FPGA	reporter	comment	LUTs ALM	LUT?	mults	blk ram	F max	date	tool ver	MIPS /clk	clks/ inst	KIPS /LUT	src code	# src files	top file	doc	tool chain	fltg pt	Ha vd	max data	max inst	byte adrs	# inst	# reg	pipe ...	start year	last revis	reference	note worthy	comments
A		light8080	Lightweight 8080	stable	Jose Ruiz, Moti Litoche	8080	8	8x	cyclone-2-7	Jose Ruiz		413	4		4	80		9.0	0.33	9.0	7.1	vhdl	5	light8080	yes	yes	N	N	64K	64K	Y				2007	2012	8080 data sheets	targeted to balanced, bare core	typically 9 clocks per inst, .04=.33/9
A	1	t48	T48 uController	stable	Arnim Laeuger	MCS-48	8	8x	cyclone-1	Arnim Laeuge		738	4		1	59			0.33	4.0	6.6	vhdl	70	t48_core	yes	asm	N		256	1K					2004	2009	MCS-48 data sheets	used in several projects	
A		pdp11-34verilog		stable	Brad Parker	PDP11	16	16x	cyclone-4	James Brakef		3439	4			64	##	13.1	0.67	2.0	6.2	verilog	24	pdp11	yes	yes	N	N	64K	64K			8		2009		PDP11 data sheets	boots & runs RT-11, EIS inst & MMU	www.heeltoe.com/download/pdp11/README.html
A	1	t51	T51 mcu	stable	Andreas Voggeneder	8051	8	8x	kintex-7-3	James Brakef		1942	6	1		147	##	14.7	0.33	4.0	6.2	vhdl	17	T8032	yes	yes	N	N	64K	64K	Y				2002	2010	8032 data sheets	8052 & 8032	8032 SoC
A		t80	T80 cpu	stable	Daniel Wallner	Z80	8	8x	spartan-6-3	James	Z80 m	1462	6			83	##	14.7	0.33	3.0	6.2	vhdl	5	T80a	yes	yes	N	N	64K	64K	Y				2002	2011	z80 data sheets	Z80 & 8080 inst sets, several usage	
A		mips32r1	MIPS32 Release	stable	Grant Ayers	MIPS	32	32	spartan-3-5	James Brakef		6322	4	8		38	##	14.7	1.00	1.0	6.0	verilog	20	processor	yes	yes	N		4G	4G	Y		32		2012	2014	MIPS data sheets	Harvard arch	
A		6809_6309	6809_6309_com	beta	Alejandro Paz Schmidt	6809	8	8x	spartan-6-3	James Brakef		2061	6			109	##	14.7	0.33	3.0	5.8	verilog	5	MC6809_cpu	yes	yes	N	N	64K	64K	Y				2012	2013	6809 data sheets	includes 6309 op-codes, xilinx & lattice projects	
W		natalius_8b	Natalius 8 bit RIS	beta	Fabio Guzman	RISC	8	16	spartan-3e-	James Brakef		385	4		2	59	##	14.7	0.11	3.0	5.7	verilog	12	natalius_pro	yes	asm	N	Y	256	2K	Y	29	8		2012	2012		return stack & register file	3 clocks/inst
A		t51	T51 mcu	stable	Andreas Voggeneder	8051	8	8x	kintex-7-3	James Brakef		1921	6	1	2	127	##	14.7	0.33	4.0	5.5	vhdl	17	T8052	yes	yes	N	N	64K	64K	Y				2002	2010	8052 data sheets	8052 & 8032	8052 SoC
A		next186	Next 80186 proc	stable	Nicolae Dumitrache	8086	16	8x	spartan-6-3	James Brakef		2716	6	1		44	##	14.7	0.67	2.0	5.4	verilog	4	Next186_CP	yes	yes	N	N	1M	1M	Y				2012	2013	x86 data sheets	boots DOS	
A	1	turbo8051	turbo 8051	beta	Dinesh Annayya	8051	8	8x	kintex-7-3	James Brakef		1985	6	1		127	##	14.7	0.33	4.0	5.3	verilog	74	oc8051_top	yes	yes	N	N	64K	64K	Y				2011	2013	8051 data sheets	includes perpherials	
A		mips32r1	MIPS32 Release	stable	Grant Ayers	MIPS	32	32	cyclone-4	James Brakef		9556	4			48	##	13.1	1.00	1.0	5.0	verilog	20	processor	yes	yes	N		4G	4G	Y		32		2012	2014	MIPS data sheets	Harvard arch	did not infer multipliers
A	1	pdp1	PDP-1 reimplem	alpha	Yann Vernier	PDP11	18	18	spartan-3a-	James Brakef		1390	4		6	138	##	14.7	0.50	10.0	5.0	vhdl		top	yes	yes	N	N	4K	4K		28			2011	2011	http://pdp-1.comput	PDP-1 descended from MIT TX-0	uses Minimal UART from opencores
A		next186	Next 80186 proc	stable	Nicolae Dumitrache	8086	16	8x	cyclone-4	James Brakef		3252	4			48	##	13.1	0.67	2.0	4.9	verilog	4	Next186_CP	yes	yes	N	N	1M	1M	Y				2012	2013	x86 data sheets	boots DOS	did not infer multiplier
A		hc11core		stable	Green Mountain Comp	68HC11	8	8x	arria-2	James Brakef		1962	A			116	##	13.1	0.33	4.0	4.9	vhdl	1	hc11rtl	yes	yes	?	N	64K	64K	N	53	8	2	2000		6811 data sheets	restricted use license, with correction	http://www.gmvhdl.com/hc11core.html
A		pdp11-34verilog		stable	Brad Parker	PDP11	16	16x	spartan-3-5	James Brakef		3842	4			56	##	14.7	0.67	2.0	4.8	verilog	24	pdp11	yes	yes	N	N	64K	64K			8		2009		PDP11 data sheets	boots & runs RT-11, EIS inst & MMU	www.heeltoe.com/download/pdp11/README.html
A		pdp11-34verilog		stable	Brad Parker	PDP11	16	16x	cyclone-2-7	James Brakef		3410	4			49	##	11.1	0.67	2.0	4.8	verilog	24	pdp11	yes	yes	N	N	64K	64K			8		2009		PDP11 data sheets	boots & runs RT-11, EIS inst & MMU	www.heeltoe.com/download/pdp11/README.html
A	1	hc11core		stable	Green Mountain Comp	68HC11	8	8x	kintex-7-3	James Brakef		2190	6			127	##	14.7	0.33	4.0	4.8	vhdl	1	hc11rtl	yes	yes	?	N	64K	64K	N	53	8	2	2000		6811 data sheets	restricted use license, with correction	http://www.gmvhdl.com/hc11core.html
A		next186	Next 80186 proc	stable	Nicolae Dumitrache	8086	16	8x	cyclone-2	James Brakef		2865	4			39	##	11.1	0.67	2.0	4.5	verilog	4	Next186_CP	yes	yes	N	N	1M	1M	Y				2012	2013	x86 data sheets	boots DOS	did not infer multiplier
A		tv80	TV80	mature	Guy Hutchison, Howar	Z80	8	8x	cyclone-4	James Brakef		2193	4			86	##	13.1	0.33	3.0	4.3	verilog	6	tv80n	yes	yes	N	N	64K	64K	Y				2004	2012	z80 data sheets	derived from Daniel Wallner's T80, ASIC implementations	
A		amber	Amber ARM-cor	stable	Conor Santifort	ARM7	32	32	spartan-6-3	James Brakef		6901	6		4	40	##	14.7	0.75	1.0	4.3	verilog	25	a23_core	yes	yes	N		4G	4G	Y			3	2010	2013	ARM7 data sheets	no MMU, shared cache	2048 LUTs used as single port RAM
A	1	t400	T400 uController	stable	Arnim Laeuger	COP400	4	8x	cyclone-1	Arnim Laeuge		583	4		2	59			0.17	4.0	4.3	vhdl	53	t400_core	yes	asm	N		256	1K					2006	2009	COP400 data sheets	several variants	
A		ag_6502	ag_6502 soft co	beta	Oleg Odintsov	6502	8	8x	spartan-3e-	Oleg Odintso		978	4	0	0	50			0.33	4.0	4.2	verilog	2	ag_6502	yes	yes	N	N	64K	64K	Y				2012	2012	6502 data sheets	verilog code generation, "phase level accurate"	
A		next186	Next 80186 proc	stable	Nicolae Dumitrache	8086	16	8x	spartan-3-5	James Brakef		2763	4	1		34	##	14.7	0.67	2.0	4.2	verilog	4	Next186_CP	yes	yes	N	N	1M	1M	Y				2012	2013	x86 data sheets	boots DOS	
A	1	df6805		proprietar	Hitech Global	6805	8	8x	stratix-1	Hitech Globa		1690	4			83			0.33	4.0	4.1	not avail			yes	yes	N	N	64K	64K	Y						6805 data sheets		www.hitechglobal.com/IPCores/DF6805.htm
A		t400	T400 uController	stable	Arnim Laeuger	COP400	4	8x	spartan-2	Arnim Laeuge		643	4		2	60			0.17	4.0	4.0	vhdl	53	t400_core	yes	asm	N		256	1K					2006	2009	COP400 data sheets	several variants	
A	1	cpu8080	8080 Compatible	stable	Scott Moore	8080	8	8x	spartan-6-3	James Brakef		1269	6			129	##	14.7	0.33	9.0	3.7	verilog	1	m8080	yes	yes	N	N	64K	64K	Y				2006	2009	8080 data sheets	includes VGA display generator, three variants	
B	1	68hc08	68hc08	stable	Ulrich Riedel	6808	8	8x	kintex-7-3	James Brakef		2290	6			101	##	14.7	0.33	4.0	3.6	vhdl	1	x68urt08		yes	N	N	64K	64K	Y				2007	2009	6808 data sheets		
A		t80	T80 cpu	stable	Daniel Wallner	8080	8	8x	spartan-6-3	James	8080	958	6			95	##	14.7	0.33	9.0	3.6	vhdl	5	T8080se	yes	yes	N	N	64K	64K	Y				2002	2011	8080 data sheets	Z80 & 8080 inst sets, several usage	
A	1	lattice6502	Lattice 6502	beta	Ian Chapman	6502	8	8x	kintex-7-3	James Brakef		4942	6			214	##	14.7	0.33	4.0	3.6	vhdl	3	ghdl_proce	yes	yes	N	N	64K	64K	Y				2010	2010	6502 data sheets	targeted to LCMXO2280	huge LUT count
A	1	z80soc	Z80 System on C	stable	Ronivon Costa	Z80	8	8x	spartan-3e-	James Brakef		2474	4	2	19	78	##	14.7	0.33	3.0	3.4	vhdl	19	top_s3e	yes	yes	N	N	64K	64K	Y				2008	2010	z80 data sheets	based on Daniel Wallner's T80	
A		system09	SOC:system09	stable	John Kent	6809	8	8x	spartan-6-3	James Brakef		2127	6			64	##	14.7	0.33	3.0	3.3	vhdl	40	cpu09l	yes	yes	N	N	64K	64K	Y				2003	2012	6809 data sheets	from John Kent web page	
A		amber	Amber ARM-cor	stable	Conor Santifort	ARM7	32	32	spartan-6-3	James Brakef		12834	6		8	40	##	14.7	1.05	1.0	3.3	verilog	25	a25_core	yes	yes	N	Y	4G	4G	Y			5	2010	2013	ARM7 data sheets	no MMU, data & inst caches	4096 LUTs used as single port RAM
A		t48	T48 uController	stable	Arnim Laeuger	MCS-48	8	8x	spartan-2	Arnim Laeuge		771	4		1	30			0.33	4.0	3.2	vhdl	70	t48_core	yes	asm	N		256	1K					2004	2009	MCS-48 data sheets	used in several projects	
A		z80soc	Z80 System on C	stable	Ronivon Costa	Z80	8	8x	cyclone-3	James Brakef		2831	4		22	82	##	13.1	0.33	3.0	3.2	vhdl	19	top_de1	yes	yes	N	N	64K	64K	Y				2008	2010	z80 data sheets	based on Daniel Wallner's T80	removed pin assignments
A	1	tg68	TG68 execute 68	stable	Tobias Gubener	68000	16	16x	kintex-7-3	James Brakef		2331	6			44	##	14.7	0.67	4.0	3.2	vhdl	2	TG68_fast	yes	yes	N	N	4G	4G	Y		16		2007	2012	68000 data sheets	for use with Minimig	
A		tv80	TV80	mature	Guy Hutchison, Howar	Z80	8	8x	cyclone-2	James Brakef		2148	4			61	##	11.1	0.33	3.0	3.1	verilog	6	tv80n	yes	yes	N	N	64K	64K	Y				2004	2012	z80 data sheets	derived from Daniel Wallner's T80, ASIC implementations	
A	1	cpu86		beta	ht-lab.com	8086	8	8x	kintex-7-3	James Brakef		3421	6	1		127	##	14.7	0.17	2.0	3.1	vhdl	23	cpu86_top	yes	yes	N	N	1M	1M	Y				2002	2010	x86 data sheets	8088 clone	www.ht-lab.com
W	1	fpgammix		stable	Tommy Thorn	RISC	64	32	arria-2	James Brakef		11605	A	8	10	94	##	13.1	1.50	4.0	3.0	system v	2	core	yes	yes	Y	Y	4G	4G	Y	256	288		2006	2008		clone of Knuth's MMIX	micro-coded
A		t51	T51 mcu	stable	Andreas Voggeneder	8051	8	8x	arria-2	James	proba	3049	6	1		111	##	13.1	0.33	4.0	3.0	vhdl	17	T8032	yes	yes	N	N	64K	64K	Y				2002	2010	8032 data sheets	8052 & 8032	8032 SoC
A		t80	T80 cpu	stable	Daniel Wallner	Z80	8	8x	spartan-3-5	James	Z80 m	1991	4			54	##	14.7	0.33	3.0	3.0	vhdl	5	T80a	yes	yes	N	N	64K	64K	Y				2002	2011	z80 data sheets	Z80 & 8080 inst sets, several usage	
A		tv80	TV80	mature	Guy Hutchison, Howar	Z80	8	8x	spartan-3-5	James Brakef		2095	4			54	##	14.7	0.33	3.0	2.9	verilog	6	tv80n	yes	yes	N	N	64K	64K	Y				2004	2012	z80 data sheets	derived from Daniel Wallner's T80, ASIC implementations	
A		light52	Lightweight 805	beta	Jose Ruiz	8051	8	8x	cyclone-2-7	Jose Ruiz		1339	4	1	29	62			0.33	6.0	2.5	vhdl	8	light52_cpu	yes	yes	N	N	64K	64K	Y				2012	2013	8051 data sheets	targeted to area	0.0187 DMIPS/MHz, i8051 is 0.0094 DMIPS/MHz
A	1	mc8051		stable	Helmut Mayrhofer	8051	8	8x	kintex-7-3	James Brakef		3022	6	1		83	##	14.7	0.33	4.0	2.3	vhdl	49	mc8051core	yes	yes	N	N	256	64K	Y				1999	2013	www.oreganosystem	fast 8051, version available with floating-point by David Lundgren	
A	1	hd63701	HD63701 compa	planning	Tsuyoshi Hasegawa	6801	8	8x	spartan-6-3	James Brakef		1412	6	1	3	31	##	14.7	0.33	4.0	1.8	verilog	6	HD63701_CORE			N	N	64K	64K	Y				2014			Used in Atari game console, 6801 clone?	
A	1	system68	System68	stable	John Kent, David Burne	6801	8	8x	spartan-3-5	James Brakef		2235	4		4	46	##	14.7	0.33	4.0	1.7	vhdl	21	cpu68	yes	yes	N	N	64K	64K	Y				2003	2009	6801 data sheets		
A	1	k68	K68	alpha	Shawn Tan	68000	8	16x	kintex-7-3	James Brakef		2392	6			24	##	14.7	0.67	4.0	1.7	verilog	15	k68_cpu	yes	yes	N	N	4K	4G	Y		16		2003	2009	68000 data sheets	68K binary compatible	
A		t51	T51 mcu	stable	Andreas Voggeneder	8051	8	8x	arria-2	James	proba	4704	6	1	1	89	##	13.1	0.33	4.0	1.6	vhdl	17	T8052	yes	yes	N	N	64K	64K	Y				2002	2010	8052 data sheets	8052 & 8032	8052 SoC
X	1	edge	Edge Processor	alpha	Hesham ALMatary	MIPS	32	32	spartan-6-3	James Brakef		5345	6	7	1	8	##	14.7	1.00	1.0	1.5	verilog	30	edge_core	yes	yes	N	N	4G	4G	Y		32	5	2014		MIPS data sheets	MIPS1 clone	
A		light52	Lightweight 805	beta	Jose Ruiz	8051	8	8x	spartan-3-4	Jose Ruiz		1424	4	1	10	35			0.33	6.0	1.4	vhdl	8	light52_cpu	yes	yes	N	N	64K	64K	Y				2012	2013	8051 data sheets	targeted to area	~ 6 clocks/inst
A	1	suska-III		beta	Wolfgang Forster	68000	16	16x	arria-2	James Brakef		7388	A			55	##	13.1	0.67	4.0	1.3	vhdl	11	wf68k00ip	yes	yes	N	N	4G	4G	Y		16		2003	2013	68000 data sheets	for use as an Atari ST	http://www.experiment-s.de/en/
A	1	ao486	ao486	beta	Aleksander Osman	x86	32	8x	cyclone-4-7	James Brakef		35872	4	4	34	44	##	13.1	1.00	1.0	1.2	verilog	85	ao486	yes	yes			4G	4G	Y				2014	2014	x86 data sheets	complete 486, SoC configuration	non-SoC, no MMU
A	1	s1_core	S1 Core	stable	Fabrizio Fazzino etal	SPARC	64	32	kintex-7-3	James Brakef		54434	6	8	57	50	##	14.7	1.00	1.0	0.9	verilog	136	s1_top	yes	yes	N	N	4G	4G	Y		32		2007	2012	SPARC data sheets	reduced version of OpenSPARC T1	
A		hd63701	HD63701 compa	planning	Tsuyoshi Hasegawa	6801	8	8x	spartan-3-5	James Brakef		1937	4	1	3	20	##	14.7	0.33	4.0	0.9	verilog	6	HD63701_CORE			N	N	64K	64K	Y				2014			Used in Atari game console, 6801 clone?	
A		cpu65c02_t	cpu65c02_tc	stable	Jens Gutschmidt	6502	8	8x	spartan-6-3	James	latch v	4794	6			47	##	14.7	0.33	4.0	0.8	vhdl	8	core		yes	N	N	64K	64K	Y				2008	2013	6502 data sheets		
A		turbo8051	turbo 8051	beta	Dinesh Annayya	8051	8	8x	cyclone-2	Dinesh Anna		5072	4			39			0.33	4.0	0.6	verilog	74	oc8051_top	yes	yes	N	N	64K	64K	Y				2011	2013	8051 data sheets	includes perpherials	
		suska-III		beta	Wolfgang Forster	68000	16	16x	cyclone-4-6	James Brakef		9894	4			34	##	13.1	0.67	4.0	0.6	vhdl	11	wf68k00ip	yes	yes	N	N	4G	4G	Y		16		2003	2013	68000 data sheets	for use as an Atari ST	http://www.experiment-s.de/en/
A		ao486	ao486	beta	Aleksander Osman	x86	32	8x	cyclone-4-7	Aleksander O		91256	4	22	106	39		13.1	1.00	1.0	0.4	verilog	85	soc	yes	yes			4G	4G	Y				2014	2014	x86 data sheets	complete 486, SoC configuration	running on Terasic DE2-115 board

66 # usable(beta, stable or mature): "A"(clones) & "W"(originals)
4 34 "B" or "X" of limited interest

171 unique usable designs

5

MIPS/MHz Pro-rating for data size:

1-bit	0.04
8-bit	0.33
16-bit	0.67
32-bit	1.00

Under the assumption that the core is capable of one instuction per clock

Silicon Area equivalents

LUTS/DSP48	16:1
LUTS/Block RAM	32:1

Following has DMIPS per clock for many microprocessors
http://en.wikipedia.org/wiki/Instructions_per_second

adrs

Web page DMIPS per clock cycle per core en.wikipedia.org/wiki/Instructions community.freescale www.eembc.org/coremark/index.php

uP	MIPS			CoreMarks /MHz	MHz		guessed average clocks/inst
4004	0.10						
6502	0.50		0.02	0.06			4
8051	0.01	DMIPS	0.08	0.24			1, 4 or 6
8080	0.17			0.25			9
68K	0.10			0.15			4
ARM Cortex A9	2.50	DMIPS		2.90	1000		
ARM Cortex M0	0.90	DMIPS		1.50	70		
ARM Cortex M3	1.25	DMIPS		2.17	25		
ARM7	0.90		0.74	2.04	600		
AVR	1.00		0.21	0.53	8		
AVR32				1.62	60		
BA21				2.44	400		
Coldfire				2.80	400		
Coldfire				0.77	150	Virtex-5	2
HC508			0.04	0.12			4
HC11							4
LEON3/Spartan-6				1.96	100		
MC6809	1.24		0.07	1.86			3
MicroBlaze 3-stage	1.03			1.50			
MicroBlaze 5-stage	1.38			1.90	125		
MIPS32	1.51			2.28			
MSP430			0.40	1.20			2
MSP430				1.10	25		2
Nios II	0.64	DMIPS		0.93	200		
Nios II -e	0.15	DMIPS		0.25			
Nios II -f	1.13	DMIPS		1.60	200		
PIC16	0.25						
PIC18				0.04	40		
PIC24			0.72	1.86	40		
PIC32				3.45	80		
Super H-2				1.44	180		
VAX780	1.00	DMIPS		1.50		DMIPS # is by definition	
Z80	1.60		0.01	0.03			3
eSi-1600				1.98			

Column Titles	Details
"A"	A: 1st choice clone, B: 2nd choice clone, W: 1st choice original, X: 2nd choice original
"B"	used to indicate best KIPS/LUT for a given design, usually using fast FPGA family
_uP_cores_test folder	if opencores design is their folder name, otherwise my folder name
opencores name	
status	ASIC, planning, alpha, beta, stable, mature, proprietary
author	First Name, Last Name
style / clone	part number or "forth", RISC, accumulator, etc
data size	data memory word size
inst size	instruction size
FPGA	FPGA family for compile, place, route & timing, usually using fastest part grade
reporter	First Name, Last Name
comments	compile, place, route & timing problems
LUTs ALM	4-LUT, 6-LUT, Altera ALM, Actel Tile
LUT?	total number of LUTs or ALMs used including route-thrus & otherwise unavailable
mults	total number of multipliers/DSPs used; 9x9 multiplier counts divided by two and rounded up
blk RAM	total # of block RAMs used, Xilinx half block RAM counts divided by two and rounded up, Altera count is percent used times # avail
Fmax	maximum primary clock speed from compile, place, route & timing run
date	date of compile, place & route; serves to identify source version
tool ver	Altera, Xilinx, Lattice Semiconductor or MicroSemi tool version number
MIPS /clk	prorated DMIPS per clock, reduced for data word sizes under 32-bits, greater than one for multiple issue processors
clks/ inst	number of clocks per instruction, typically 1.0 for modern pipelined processors, subjective for older uP
KIPS /LUT	figure of merit, does not include effects of memory capacity, floating point or instruction set quality
src code	VHDL or Verilog or System Verilog or schematic or gates
# src files	number of source files for compile, place, route & timing
top file	top file for compile, place, route & timing run
doc	is documentation provided
tool chain	is there a compiler or assembler provided or available
fltg pt	does the compile, place, route & timing run include floating point
Ha vd	separate instruction and data memory(s), there can be more than one data memory, M for MMU & caches
max data	maximum data address
max inst	maximum instruction address
byte adrs	is byte addressing provided
max inst	number of unique instructions, somewhat subjective
# reg	number of registers in register file
pipe len	number of pipeline stages
start year	year of first design activity
last revis	last year for revisions
reference	web address or generic information (for clones)
note worthy	anything special about the design
comments	catchall