Opencore and other soft core processors

		_uP_cores_test folder	opencores name	status	author	style / clone	data size	inst size	FPGA	reporter	comment	LUTs ALM	LUT?	mults	blk ram	F max	date	tool ver	MIPS /clk	clks/ inst	KIPS /LUT	src code	# src files	top file	doc	tool chain	fltg pt	Hard	max data	max inst	byte adrs	# inst	# reg	pipe len	start year	last revis	reference	note worthy	comments
A	1	cray1		alpha	Christopher Fenton	cray1	64	16	kintex-7-3	James Brakef		13463	6	19	10	127	##	14.7	6.00	1.0	56.6	verilog	46	cray_sys	yes	yes	Y	N	4M	4M	N		512		2010		CRAY data sheets	homebrew Cray1	www.chrisfenton.com/homebrew-cray-1a/
W	1	fpgammix		stable	Tommy Thorn	RISC	64	32	arria-2	James Brakef		11605	A	8	10	94	##	13.1	1.50	4.0	3.0	system v	2	core	yes	yes	Y	Y	4G	4G	Y	256	288		2006	2008		clone of Knuth's MMIX	micro-coded
A	1	s1_core	S1 Core	stable	Fabrizio Fazzino etal	SPARC	64	32	kintex-7-3	James Brakef		54434	6	8	57	50	##	14.7	1.00	1.0	0.9	verilog	136	s1_top	yes	yes	N	N	4G	4G	Y		32		2007	2012	SPARC data sheets	reduced version of OpenSPARC T1	
A	1	microblaze		proprieta	Xilinx	uBlaze	32	32	kintex-7	Xilinx		546	6		1	320			1.03	1.0	603.7	not avail			yes	yes	opt		4G	4G	Y	86	32	3	2002		www.xilinx.com/tools	MicroBlaze MCS, smallest configuratio	70 configuration options, MMU optional
A	1	ARM_Cortex_A9		ASIC	ARM	ARM a9	32	16	arria V	altera		4500	A			1050			2.50	1.0	583.3	asic			yes	yes	Y		4G	4G	Y	80	16	10		2012	altera data sheets	uses pro-rated LC area	dual issue, includes fltg-pt & MMU & caches
A	1	nios2		proprietar	Altera	Nios II	32	32	stratix-5	Altera		895	A			310			1.13	1.0	389.7	not avail			yes	yes	opt		4G	4G	Y		32		2004		NIOS2 data sheets	fltg-pt, caches & MMU options	Nios II/f: fastest version
W	1	hive	hive	stable	Eric Wallin	4-8 stack	32	16	cyclone-5	James Brakef		628	A	3	3	217	##	13.1	1.00	1.0	345.0	verilog		core	yes		N				N	40	10	8	2013	2014		4-8 symetrical stacks, eight threads via	pipeline barrel
W	1	microcore		beta	Klaus Schleisiek	forth	32	8	kintex-7-3	James Brakef		644	6			149	##	14.7	1.00	1.0	231.3	vhdl	10	core	yes	asm	N	Y	2M	512K					2004		has several PDFs	indexing into return stack, auto inc/de	AKA uCore110
A	1	mips789	mips789	stable	Li Wei	MIPS	32	32	kintex-7-3	James Brakef		1432	6		1	171	##	14.7	1.00	1.0	119.1	verilog	10	mips_cor	yes	yes	N		4G	4G	Y		32		2007	2009	MIPS data sheets		
W	1	ensilica		proprieta	ensilica.com	eSi-3200	32		stratix-4	ensilica		1800	A			200			1.00	1.0	111.1	not avail			yes	yes			4G	4G			16	5			www.ensilica.com	verilog source included with license	10 addressing modes
A	1	ion	Ion MIPS compa	mature	Jose Ruiz	MIPS	32	32	kintex-7-3	James Brakef		1533	6			163	##	14.7	1.00	1.0	106.0	vhdl	12	mips_soc	yes	yes	N		4G	4G	Y		32		2011	2014		MIPS R3000 clone	
X	1	jam		stable	Johan Thelin etal	RISC	32	32	kintex-7-3	James Brakef		1369	6			143	##	14.7	1.00	1.0	104.2	vhdl	17	cpu	yes		N	Y	128K	128K			32	5	2002			serial multiply & divide	
A	1	ucore	Ucore	stable	Whitewill	MIPS	32	32	kintex-7-3	James Brakef		2469	6		1	231	##	14.7	1.00	1.0	93.5	verilog	25	ucore	yes	yes	N		4G	4G	Y		32	6	2005	2010	MIPS data sheets	MMU & caches	
W	1	altor32_lite	AltOr32	stable	Ultra Embedded	OpenRISC	32	32	arria-2	James Brakef		1809	A			161	##	13.1	1.00	1.0	88.8	system v	8	altor32		yes	N		4G	4G	Y				2012	2014	OpenRISC 1000	simplified OpenRISC 1000	LPMs & systemVerilog
A	1	openfire2	OpenFIRE	beta	Antonio Anton	uBlaze	32	32	kintex-7-3	James Brakef		1201	6	3	2	105	##	14.7	1.00	1.0	87.4	verilog	27	openfire_	yes	yes	N	N	4G	4G	Y		32		2007	2012	uBlaze data sheets	"FPGA Proven"	derived from Stephen Craven's OpenFire
A	1	storm_core	Storm Core (ARM	beta	Stephan Nolting	ARM7	32	32	kintex-7-3	James Brakef		2312	6	3		179	##	14.7	1.00	1.0	77.4	vhdl	16	CORE	yes	yes	N		4G	4G	Y		32	8	2011	2014		I & D caches not compiled	
A	1	aspida	ASPIDA DLX core	stable	Sotiriou	DLX	32	32	kintex-7-3	James Brakef		3586	6			257	##	14.7	1.00	1.0	71.7	verilog	10	DLX_top	yes	yes			4G	4G					2002	2009	Knuth DLX		compiled sync version
A	1	m1_core	M1 Core	beta	Fabrizo Fazzino, Albert	MIPS?	32	32	kintex-7-3	James Brakef		3456	6			233	##	14.7	1.00	1.0	67.3	verilog	9	m1_core		yes	N		4G	4G	Y		32		2007	2012		GCC target?	
X	1	risc0		beta	Niklaus Wirth	RISC	32	32	kintex-7-3	James Brakef		1186	6	4	6	110	##	14.7	0.67	1.0	61.9	verilog	8	RISC0	yes	yes	N		4G	4G					2011			minimalist Wirth, education tool	
A	1	secretblaze		beta	Lyonel Barthe	uBlaze	32	32	spartan-3-4	Lyonel Barthe		1563	4			91		12.1	1.00	1.0	58.2	vhdl	26	sb_core		yes			4G	4G	Y	86	32	5	2010	2012	www.lirmm.fr/ADAC/		
W	1	latticemicro32		stable	Yann Siommeau, Micha	RISC	32	32	kintex-7-3	James Brakef		2292	6	3	8	155	##	14.7	0.80	1.0	54.2	verilog	24	lm32_cpu	yes	yes	N		4G	4G	Y		32		2006	2012	en.wikipedia.org/wiki	optional data & inst caches	
X	1	eco32	SOC:ECO32	stable	Hellwing Geisse	RISC	32	32	kintex-7-3	James Brakef		2210	6		1	160		14.7	1.00	1.5	48.1	verilog	23	cpu	yes	yes	N		512M	256M	Y	61	32		2003	2014		MIPS like, slow mul & div	
X	1	qrisc32	qrisc32 wishbon	alpha	Viacheslav	RISC	32	32	arria-2	James Brakef		3075	A	4		144	##	13.1	1.00	1.0	46.9	system v	8	qrisc32	yes	yes	N		4G	4G	Y		32	4	2010	2011		for PhD thesis	
A	1	minimips	miniMIPS	stable	Poppy etal	MIPS	32	32	kintex-7-3	James Brakef		2939	6	8		118	##	14.7	1.00	1.0	40.1	vhdl	12	minimips	yes	yes	N		4G	4G	Y		32	5			MIPS I		
W	1	ba22		proprieta	CAST Inc	RISC	32	16x	spartan-6	CAST Inc		1800	6		32	72			1.00	1.0	40.0	not avail							4G	4G			32				www.cast-inc.com		
A	1	plasma	Plasma most MI	stable	Steve Rhoads	MIPS	32	32	kintex-7-3	James Brakef		2462	6		3	97	##	14.7	1.00	1.0	39.5	vhdl	22	plasma	yes	yes	N		4G	4G	Y		32		2001	2013	MIPS data sheets	wide outside use, opencores page has list of related publications	
W	1	risc5		beta	Niklaus Wirth	RISC	32	32	kintex-7-3	James Brakef		2441	6	4	1	92	##	14.7	1.00	1.0	37.8	verilog	8	RISC5	yes	yes	Y		4G	4G			16		2013			minimalist Wirth, part of Project Oberd	32x32 multiplier
A	1	mipsr2000	mipsr2000	stable	Lazaridis Dimitris	MIPS	32	32	kintex-7-3	James Brakef		1971	6	4	6	71	##	14.7	1.00	1.0	36.2	vhdl	35	Dm	yes	yes	N		4G	4G	Y		32	5	2012	2013	MIPS data sheets	course project	
W	1	nige_machine		stable	Andrew Read	forth	32	8	kintex-7-3	James Brakef		5033	6	8	33	123	##	14.7	1.00	1.0	24.5	vhdl	29	Board	yes	yes	N		16M	16M		512	512		2014			standalone Forth system	
W	1	minsoc	minsoc	stable	Raul Fajardo etal	OpenRISC	32	32	kintex-7-3	James Brakef		4945	6	4	8	107	##	14.7	1.00	1.0	21.7	verilog	88	or1200_t	yes	yes	Y	M	4G	4G	Y		32		2009	2013	www.minsoc.com	minimal OR1200, vendor neutral, has caches	
A	1	aquarius	aquarius	stable	Thorn Aitch	SuperH-2	32	16	kintex-7-3	James Brakef		3958	6	2		86	##	14.7	1.00	1.0	21.6	verilog	21	top	yes	yes	N		4G	4G	Y				2003	2009	SuperH data sheets		
A	1	mips32r1	MIPS32 Release	stable	Grant Ayers	MIPS	32	32	arria-2	James Brakef		3716	A	8		79	##	13.1	1.00	1.0	21.3	verilog	20	processor	yes	yes	N		4G	4G	Y		32		2012	2014	MIPS data sheets	Harvard arch	
W	1	zpu	ZPU the worlds s	stable	Oyvind Harboe	forth	32	8	spartan-6	Oyvind Harbo		1259	6			135			0.10	1.0	10.7	vhdl	23	zpu_core	yes	yes	N		4G	4G	Y	37			2008	2009	www.zylin.com	zpu4: 16 & 32 bit versions, code size 80% of ARM (thumb), low MIPs/MHz	
A	1	amber	Amber ARM-con	stable	Conor Santifort	ARM7	32	32	kintex-7-3	James Brakef		6409	6		2	82	##	14.7	0.75	1.0	9.6	verilog	25	a23_core	yes	yes	N		4G	4G	Y			3	2010	2013	ARM7 data sheets	no MMU, shared cache	2048 LUTs used as single port RAM
A	1	amber	Amber ARM-con	stable	Conor Santifort	ARM7	32	32	kintex-7-3	James Brakef		12450	6		4	98	##	14.7	1.05	1.0	8.2	verilog	25	a25_core	yes	yes	N	Y	4G	4G	Y			5	2010	2013	ARM7 data sheets	no MMU, data & inst caches	4096 LUTs used as single port RAM
X	1	edge	Edge Processor (	alpha	Hesham ALMatary	MIPS	32	32	spartan-6-3	James Brakef		5345	6	7	1	8	##	14.7	1.00	1.0	1.5	verilog	30	edge_cor	yes	yes	N	N	4G	4G	Y		32	5	2014		MIPS data sheets	MIPS1 clone	
A	1	ao486	ao486	beta	Aleksander Osman	x86	32	8x	cyclone-4-7	James Brakef		35872	4	4	34	44	##	13.1	1.00	1.0	1.2	verilog	85	ao486	yes	yes			4G	4G	Y				2014	2014	x86 data sheets	complete 486, SoC configuration	non-SoC, no MMU
A	1	pdp1	PDP-1 reimplem	alpha	Yann Vernier	PDP11	18	18	spartan-3a-	James Brakef		1390	4		6	138	##	14.7	0.50	10.0	5.0	vhdl		top	yes	yes	N	N	4K	4K		28			2011	2011	http://pdp-1.computa	PDP-1 descended from MIT TX-0	uses Minimal UART from opencores
X	1	iDEA		proprietar	Liu Cheah etal	RISC	16	32	virtex-6	Liu Cheah		190	6	1	1	534			0.67	1.0	1883.1	not avail									20	32	9		2011	A Lean FPGA Soft Pro	uses DSP slice in barrel mode for ALU	by Xilinx, no source
W	1	leros	Leros	stable	Martin Schoeberl	accum	16	16	spartan-6	Martin Schoe		112	6		1	182			0.67	1.0	1088.8	vhdl	5	leros	yes	yes	N	Y	256	64K			2	2	2008	2012	Leros: A Tiny Microco	short LUT inst ROM	256 word data RAM, PIC like
W	1	Lutiac		custom	David Galloway, David	2 reg	16	NA	stratix-4	David Gallow		140	A	4		198			0.67	1.0	947.6	vhdl & verilog								64	N	64	32	3		2010	Lutiac – Small Soft Pro	no inst RAM, instead microcode	no inst mem: small state machine, ~200 inst optimal
W	1	octavo		beta	Charles LaForest	reg	16	16	stratix-4	Charles LaFor		500	A	1		550			0.67	1.0	737.0	verilog	18	Octavo	yes	asm	N						14	16	10		2012	Octavo: an FPGA-Cen	8 core barrel, adjustable data width	~= performance across word sizes, no call/rtn inst
X	1	cpu16		beta	C. H. Ting	forth	16	5	kintex-7-3	James	case c	367	6			355	##	14.7	0.67	1.0	648.1	vhdl	1	cpu16	yes	asm	N		64K	64K		28			2000			part of eForth?	data width can be expanded
X	1	msl16		beta	Philip Leong, Tsang, Le	forth	16	4	kintex-7-3	James Brakef		303	6			256	##	14.7	0.67	1.0	566.4	vhdl	13	cpu	yes	asm	N		256			16			2001			CPLD prototype	
W	1	alwcpu	Alwcpu	alpha	Andreas Hilvarsson	RISC	16	16	kintex-7-3	James Brakef		298	6			237	##	14.7	0.67	1.0	533.3	vhdl	7	top	some		N		64K	64K	Y		16		2009	2009		lightweight CPU	
X	1	micro16b		beta	John Kent	accum	16	16	kintex-7	James Brakef		205	6			434	##	14.7	0.33	2.0	349.0	vhdl	1	u16bcpu	yes	asm	N	N	64K	4K	Y	8			2002	2008	members.optushome	very limited inst set	MIPS/clk adj'd, 2 clks/inst
W	1	J1		stable	James Bowman	forth	16	16	spartan-6	James Brakef		333	6		1	117	##	14.7	0.80	1.0	280.2	vhdl	1	j1	yes	forth	N		64K	64K		16		2	2006	2010	excamera.com/sphinx	uCode inst, dual port block RAM	32 deep data & return stacks
X	1	diogenes	diogenes	beta	Fekknhifer	RISC	16	16	kintex-7-3	James Brakef		807	6		1	297	##	14.7	0.67	1.0	246.3	vhdl	11	cpu	yes	yes	N			1K					2008	2009		"student RISC system"	
W	1	sayeh_proces	SAYEH educatior	stable	Alireza Haghdoost, Arm	RISC	16	16	kintex-7-3	James Brakef		479	6	1		164	##	14.7	0.67	1.0	229.7	verilog	13	Sayeh	yes		N		64K	64K			32		2008	2009	haghdoost.persiangig	simple RISC	
W	1	atlas_core	Atlas Processor (	beta	Stephan Nolting	RISC	16	16	kintex-7-3	James Brakef		648	6	1	0	168	##	14.7	0.80	1.0	207.6	vhdl	8	ATLAS_CP	yes	asm	N	Y	64K	64K	Y	80	8		2013	2014	opencore page	ARM thumb like inst set	non-MMU version
W	1	b16		stable	Bernd Paysan	forth	16	5	spartan-6-3	James Brakef		554	6			134	##	14.7	0.67	1.0	161.7	verilog	1	b16	yes	yes	N								2002	2011	bernd-paysan.de/b16	two versions: one/15 source files, derived from c18	
W	1	dragonfly		beta	LEOX team	MISC	16	16	kintex-7-3	James Brakef		788	6			164	##	14.7	0.67	1.0	139.3	vhdl	6	dgf_core	yes		N		256	2K					2001		www.leox.org	unusual, uses FIFOs	
A	1	ae18	ae18	beta	Shawn Tan	PIC18	16	24	arria-2	James Brakef		1084	A	1		207	##	13.1	0.67	1.0	128.2	verilog	1	ae18_core		yes	N	Y	4K	1M					2003	2009	PIC18 data sheets	not 100% compatable	negative edge reset "clock"
X	1	hpc-16	HPC-16	beta	Umair Siddiqui	RISC	16	16	kintex-7-3	James Brakef		875	6			136	##	14.7	0.67	1.0	104.2	vhdl	20	cpu	yes	asm	N		64K	64K			16		2005	2009			
W	1	dcpu16		beta	Marcus Persson , Shaw	RISC	16	16	kintex-7-3	James Brakef		662	6	1		318	##	14.7	0.67	4.0	80.4	vhdl & v	5	dcpu16_c	yes	asm	N	N	64K	64K	N	37	8		2009	2012	https://github.com/d	for the 0X10c game	4+ addressing modes, 4 & 5-bit reg /modefields
W	1	atlas_2K	Atlas Processor (	beta	Stephan Nolting	RISC	16	16	kintex-7-3	James Brakef		1512	6	1	5	149	##	14.7	0.80	1.0	79.1	vhdl	19	ATLAS_2K	yes	asm	N	Y	64K	64K	M	80	8		2013	2014	opencore page	ARM thumb like inst set	has MMU & full SOC features
X	1	oc54x	OpenCores54x D	beta	Richard Herveille	DSP	16	16	kintex-7-3	James Brakef		2225	6	1		180	##	14.7	0.67	1.0	54.1	verilog	10	oc54_cpu	yes	yes	Y	Y	64K	64K					2002	2009		40-bit accumulator, barrel shifter	
X	1	cole_c16		beta	Cole Design & Develop	RISC	16	16	spartan-6-3	James Brakef		554	6			298	##	14.7	0.67	7.0	51.4	vhdl	1	core	yes	asm	N		64K	64K	N	20	8		2002	2012		(7) clks per inst, complete SOC	for teaching
X	1	bobcat		beta	Stan Drey		16	24	kintex-7-3	James Brakef		1622	6	1		107	##	14.7	0.67	1.0	44.0	vhdl							64K	64K					1998			appears to be a DSP	
W	1	blue	16-bit CPU Blue	stable	Al Williams	accum	16	16	spartan-3-5	James	remov	1025	4			63	##	14.7	0.67	1.0	41.1	verilog	16	topbox	web		N		4K	4K	N	16	2		2009	2010		Caxton Foster's Blue derivative	http://www.youtube.com/watch?v=dt4zezZP8w8
W	1	jop	JOP a Java Optim	stable	Martin Schoeberl etal	forth	16	16	cyclone-1	Martin Schoe		2000	4			100		10	0.67	1.0	33.5	vhdl	11	core	yes	yes	N		256K	256K					2004	2014		opencores download is empty	https://github.com/jop-devel/jop
A	1	openmsp430	openMSP430	stable	Oliver Girard	msp430	16	16x	stratix-3-2	Oliver Girard		1147	A	1		98			0.67	2.0	28.5	verilog	30	openMSP	yes	yes	N	N	64K	64K	Y		16		2009	2014	msp430 data sheets	performance spreadsheet	
A	1	rtf8088	rtf8088	planning	Robert Finch	8086	16	8x	kintex-7-3	James Brakef		4514	6	4		174	##	14.7	0.67	1.0	25.8	verilog	57	rtf8088	yes	yes	N	N	1M	1M	Y				2012	2013	x86 data sheets		
A	1	pdp11-34verilog		stable	Brad Parker	PDP11	16	16x	arria-2	James Brakef		2532	A			126	##	13.1	0.67	2.0	16.7	verilog	24	pdp11	yes	yes	N	N	64K	64K			8		2009		PDP11 data sheets	boots & runs RT-11, EIS inst & MMU	www.heeltoe.com/download/pdp11/README.html
A	1	v1_coldfire		stable	IPextreme	68000	16	16x	cyclone-3	freescale		5000	4			80			0.89	1.0	14.2				yes	yes	N	N	4G	4G	Y		16		2008		68000 data sheets	free for Cyclone III	
A	1	next186	Next 80186 proc	stable	Nicolae Dumitrache	8086	16	8x	arria-2	James Brakef		1966	A	2		77	##	13.1	0.67	2.0	13.1	verilog	4	Next186_	yes	yes	N	N	1M	1M	Y				2012	2013	x86 data sheets	boots DOS	
W	1	xr16		stable	Jan Gray	RISC	16	16	kintex-7-3	James Brakef		371	6			7	##	14.7	0.67	1.0	13.0	verilog	12	xsoc	yes		N	N	64K	64K			16		1999	2001		handcrafted FPGA layout & instruction	source code written for simulation
A	1	ao68000	ao68000	beta	Aleksander Osman	68000	16	16x	arria-2	James Brakef		3479	A		6	169	##	13.1	0.67	3.0	10.8	verilog	1	ao68000	some	yes	N		4G	4G	Y				2010	2011	68000 data sheets	uses microcode, instruction prefetch buffer	
W	1	c16	16 Bit Microcont	stable	Jsauermann	C	16	8x	spartan-3-5	James Brakef		1850	4		16	57	##	14.7	0.33	1.0	10.1	vhdl	22	Board_cp	min	C,asm	N		64K	64K	Y		5		2003	2012		8080 derivative, optional UART, 8-bit memory port	

		_uP_cores_test folder	opencores name	status	author	style / clone	data size	inst size	FPGA	reporter	comment	LUTs ALM	LUT?	mults	blk ram	F max	##	date	tool ver	MIPS /clk	clks/ inst	KIPS /LUT	src code	# src files	top file	doc	tool chain	fltg pt	Ha vd	max data	max inst	byte adrs	# inst	# reg	pipe len	start year	last revis	reference	note worthy	comments
X	1	marca	McAdam's RISC (	stable	Wolfgang Puffitsch	RISC	16	16	arria-2	James Brakef		1763	A		22	157	##		13.1	0.67	6.0	10.0	vhdl	40	marca	yes		N		8K	16K		75	16	4	2007	2009		serial multiply & divide	clks/inst is approx
A	1	tg68	TG68 execute 68	stable	Tobias Gubener	68000	16	16x	kintex-7-3	James Brakef		2331	6			44	##		14.7	0.67	4.0	3.2	vhdl	2	TG68_fas	yes	yes	N	N	4G	4G	Y		16		2007	2012	68000 data sheets	for use with Minimig	
A	1	suska-III		beta	Wolfgang Forster	68000	16	16x	arria-2	James Brakef		7388	A			55	##		13.1	0.67	4.0	1.3	vhdl	11	wf68k00i	yes	yes	N	N	4G	4G	Y		16		2003	2013	68000 data sheets	for use as an Atari ST	http://www.experiment-s.de/en/
X	1	vtach	VTACH Bell Labs	mature	Al Williams		13	12	spartan-3-4	James Brakef		557	4			71	##		14.7	0.50	1.0	64.1	verilog	16	vtach			N		256	256	Y				2913	2013		ISE project only, BCD arithmetic	
X	1	usimplez	MicroSimplez	stable	Pablo Salvadeo etal	accum	12	12	stratix-2	Pablo Salvad		48	4			134			9.1	0.17	1.0	475.9	vhdl	3	usimplez_cpu			N		512	512		8			2011		http://www-gti.det.u	part of university course, simplez+i4 h	MIPS/Mhz reduced due to few inst
A	1	pdp8verilog		stable	Brad Parker	PDP8	12	12	kintex-7-3	James Brakef		505	6			366	##		14.7	0.50	2.0	181.3	verilog	18	pdp8	yes	yes	N	N	32K	32K			8		2005	2010	PDP8 data sheets	boots & runs TSS/8 & Basic	www.heeltoe.com/download/pdp8/README.html
A	1	pdp8	PDP-8 Processor	alpha	Joe Manojlovich, Rob D	PDP8	12	12	kintex-7-3	James Brakef		1219	6	1		183	##		14.7	0.50	2.0	37.5	vhdl	55	cpu	yes	yes	N	N	32K	32K			8		2012	2013	PDP8 data sheets	Boots OS/8, runs apps, several variants	
A	1	pdp8l	Minimal PDP8/L	beta	Ian Schofield	PDP8	12	12	cyclone-3	James Brakef		1088	4		48	63	##		14.7	0.50	2.0	14.4	vhdl	11	top	yes	yes	N	N	4K	4K					2013		PDP8 data sheets		
W	1	eric5		proprieta	enter-electronics.com	forth	9	8	cyclone-4-6	enter-electro		110	4	opt		60			0.42	1.0	229.1	not avail							512	1K			3-4		2007			25 MIPS: ERIC5xs, ERIC5Q	
A	1	picoblaze	picoblaze	stable	Ken Chapman	picoBlaze	8	18	kintex-7-3	James	ROM	178	6			182	##		14.7	0.33	2.0	168.9	vhdl	1	kcspm3	yes	asm	N		256	2K	Y				2003		picoblaze data sheets	2 clocks per inst	this is the original picoBlaze author
A	1	avr8	Reduced AVR Co	beta	Nick Kovach	AVR	8	16	kintex-7-3	James Brakef		174	6			418	##		14.7	0.33	1.0	792.2	verilog	1	rAVR	yes	yes	N		64K	64K	Y	17	4		2010	2010	AVR data sheets	not a full clone, doc is opencores page	
X	1	mcpu	MCPU A minima	stable	Tim Boscke	accum	8	8	spartan-6-3	James Brakef		41	6			384	##		14.7	0.08	1.0	749.0	vhdl	1	tb02cpu2	yes	asm	N		64	64	Y	4			2007	2014		fits into 32 macrocell CPLD	reduced MIPS/clk due to only 4 inst
X	1	lwrisc	ClaiRISC	stable	Li Wu	accum	8	12	arria-2	James Brakef		88	A		1	230	##		13.1	0.17	1.0	443.6	verilog	9	risc_core		asm	N	Y	256	2K	Y	16			2008	2009		simplified PIC, 4 reg rtn stack	absolute addressing only, lowered MIPS/clk
X	1	popcorn		stable	Jeung Joon Lee	accum	8	8x	kintex-7-3	James Brakef		267	6			347	##		14.7	0.33	1.0	428.4	verilog	4	pc	yes		N		64K	64K	Y	43			2000			small 8 bit uP	
A	1	risc16f84	risc16f84	stable	John Clayton	PIC16	8	14	kintex-7-3	James Brakef		331	6			333	##		14.7	0.33	1.0	332.3	verilog	1	risc16f84_	yes	yes	N	Y	256	4K	Y				2002	2013	PIC16 data sheets	derived from CQPIC by Sumio Morioka	
W	1	gumnut		stable	Peter Ashenden	RISC	8	18	kintex-7-3	James Brakef		420	6			275	##		14.7	0.33	1.0	216.2	vhdl	20	gumnut-r	yes		N		256	4K	Y		8		2007			see Digital Design: An Embedded Syste	does not seem complete
W	1	dfp	dfp	stable	Ron Chapman	forth	8	Y	kintex-7-3	James Brakef		297	6			192	##		14.7	0.33	1.0	213.2	vhdl	25	DataFlow	yes										2003	2009		8-bitter, generates a custom VHDL stack	machine, compiler is in Forth
A	1	picoblaze	picoblaze	stable	Ken Chapman	picoBlaze	8	18	spartan-3-4	James Brakef		178	4			182	##		14.7	0.33	2.0	168.9	vhdl	1	kcspm3	yes	asm	N		256	2K	Y				2003		picoblaze data sheets	2 clocks per inst	this is the original picoBlaze author
B	1	pic_coonan		alpha	Tom Coonan	PIC16	8	14	kintex-7-3	James Brakef		328	6		1	165	##		14.7	0.33	1.0	166.1	verilog	7	piccpu	yes	yes	N	Y	256	4K	Y				1999		PIC16 data sheets		
X	1	tisc	Tiny Instruction	beta	Vincent Crabtree	accum	8	8x	kintex-7-3	James Brakef		195	6			87	##		14.7	0.33	1.0	147.1	vhdl	1	TISC			N		256	1K	Y		2		2009	2009		minimal accumulator machine	
A	1	free_risc8		stable	Thomas Coonan	PIC16	8	14	kintex-7-3	James Brakef		355	6			142	##		14.7	0.33	1.0	132.2	verilog	8	cpu	yes	yes	N		256	4K	Y				2002	2011	PIC16 data sheets		
W	1	open8_urisc	Open8 uRISC	stable	Kirk Hays, Jshamlet	RISC	8	8	kintex-7-3	James Brakef		691	6	1		263	##		14.7	0.33	1.0	125.6	vhdl	9	Open8	yes	yes	N		64K	64K	Y		8		2006	2013		accum & 8 regs, clone of Vautomation u	RISC processor, in use
A	1	pacoBlaze		mature	Pablo Kocik	picoBlaze	8	18	spartan-3	Pablo Kocik		177	4		1	117				0.33	2.0	109.1	verilog	18	pacoblaze	yes	asm	N		256	2K	Y	57		2		2006	bleyer.org/pacoblaze	3 versions, behavioral coding	
X	1	myrisc1	myRISC1	stable	Muza Byte	RISC	8	8	cyclone-2	Muza	Altera	185	4		1	57				0.33	1.0	101.8	verilog		myRISC1	yes		N	Y	256	256	Y	16	4		2011	2011		Verilog source included in PDF file	LPM macros
A	1	navre	Navre AVR clone	stable	Sebastien Bourdeaudu	AVR	8	16	kintex-7-3	James Brakef		990	6			207	##		14.7	0.33	1.0	69.0	verilog	1	softusb_r	yes	yes	N		64K	64K	Y		32	2	2010	2013	AVR data sheets	AVR clone, part of www.milkymist.org	
W	1	latticemicro8		stable	Lattice Semiconductor	RISC	8	18	LFE2	Lattice Semic		265	4			104				0.33	2.0	64.4	vhdl	10	isp8_core	yes	yes	N		256	4K	Y		32		2005	2010	en.wikipedia.org/wiki	16 deep call stack, four configurations	
X	1	erp	Educational RISC	stable	Shahzadjk	RISC	8	16	spartan-3-5	James Brakef		366	4	1	1	70	##		14.7	0.33	1.0	63.5	verilog	1	ERPverilo	yes							15	6		2004	2009		two report PDFs & one Verilog file	
A	1	light8080	Lightweight 808	stable	Jose Ruiz, Moti Litoche	8080	8	8x	kintex-7-3	James Brakef		154	6		1	247			14.7	0.33	9.0	58.9	verilog	5	i80soc	yes	yes	N	N	64K	64K	Y				2007	2012	8080 data sheets	targeted to area, includes UART, interr	typically 9 clocks per inst, .04=.33/9
A	1	copyblaze	copyBlaze	stable	Abdallah Ellbrahimi	picoBlaze	8	18	kintex-7-3	James	missin	622	6			217	##		14.7	0.33	2.0	57.5	vhdl	16	cp_copyb	yes	asm	N		256	2K	Y				2011	2013	microBlaze data shee	wishbone extras	does not infer RAM for registers
A	1	minirisc	Mini-Risc core	stable	Rudolf Usselmann	PIC16	8	14	spartan-3	Rudolf Usselr		460	4			80				0.33	1.0	57.4	verilog	7	risc_core	yes	yes	N	Y	256	4K	Y				2001	2012	PIC16 data sheets		
A	1	avrtinyx61cor	avrtinyx61core	beta	Andreas Hilvarsson	AVR	8	16	kintex-7-3	James Brakef		1243	6			194	##		14.7	0.33	1.0	51.5	vhdl	1	mcu_core		yes	N		64K	128K	Y		32		2008	2009	AVR data sheets		
A	1	avr_hp	avr_hp	stable	Strauch Tobias	AVR	8	16	kintex-7-3	James	2 slot	1554	6			223	##		14.7	0.33	1.0	47.4	vhdl	10	avr_core_	some	yes	N		64K	128K	Y		32		2010	2010	AVR data sheets	hyper pipelined (eg barrel) AVR	
X	1	micro8a		beta	John Kent	accum	8	16	kintex-7	James Brakef		531	6			204	##		14.7	0.33	3.0	42.3	vhdl	11	Micro8	yes		N	N	2K	2K	Y				2002	2002	members.optushome	derived from Tim Boscke's mcpu, not perfected	
A	1	t65	T65 CPU	stable	Daniel Wallner	6502	8	8x	kintex-7-3	James Brakef		575	6			291	##		14.7	0.33	4.0	41.7	vhdl	7	T65	yes	yes	N	N	64K	64K	Y				2002	2010	6502 data sheets	6502, 65C02 & 65C816; wide use	
W	1	natalius_8bit	Natalius 8 bit RIS	beta	Fabio Guzman	RISC	8	16	kintex-7-3	James Brakef		232	6		1	175	##		14.7	0.11	3.0	27.7	verilog	12	natalius_	yes	asm	N	Y	256	2K	Y	29	8		2012	2012		return stack & register file	3 clocks/inst
A	1	free6502		stable	David Kessner	6502	8	8x	kintex-7-3	James Brakef		646	6			193	##		14.7	0.33	4.0	24.6	vhdl	5	free6502	yes	yes	N	N	64K	64K	Y				1999	2000	6502 data sheets	microcoded	
A	1	m16c5x	M16C5x	mature	Michael Morris	PIC16	8	14	spartan-3-4	Michael Mor		1265	4		3	81				0.33	1.0	21.1	verilog	3	m16C5x	yes	yes	N	Y	256	4K	Y				2013	2014	PIC16 data sheets	SOC LUT count	was P16C5X, name could be in flux
B	1	68hc05	68hc05	stable	Ulrich Riedel	6805	8	8x	kintex-7-3	James Brakef		1225	6			300	##		14.7	0.33	4.0	20.2	vhdl	1	6805		yes	N	N	64K	64K	Y				2007	2009	6805 data sheets		
A	1	system05	SOC:system05	beta	John Kent	6805	8	8x	kintex-7-3	James Brakef		834	6			204	##		14.7	0.33	4.0	20.2	vhdl	10	System05	yes	yes	N	N	64K	64K	Y				2003	2009	6805 data sheets		
A	1	avr_core	avr_core	stable	Rusian Lepetenok	AVR	8	16	kintex-7-3	James Brakef		2135	6			127	##		14.7	0.33	1.0	19.7	verilog	15	avr_core	yes	yes	N		64K	128K	Y		32		2002	2012	AVR data sheets	VHDL core included	
A	1	ag_6502	ag_6502 soft cor	beta	Oleg Odintsov	6502	8	8x	kintex-7-3	James Brakef		824	6	0	0	176	##		14.7	0.33	4.0	17.7	verilog	2	ag_6502		yes	N	N	64K	64K	Y				2012	2012	6502 data sheets	verilog code generation, "phase level accurate"	
A	1	tv80	TV80	mature	Guy Hutchison, Howar	Z80	8	8x	kintex-7-3	James Brakef		1207	6			182	##		14.7	0.33	3.0	16.6	verilog	6	tv80n	yes	yes	N	N	64K	64K	Y				2004	2012	z80 data sheets	derived from Daniel Wallner's T80, ASIC	implementations
A	1	t80	T80 cpu	stable	Daniel Wallner	Z80	8	8x	kintex-7-3	James	Z80 m	1389	6			163	##		14.7	0.33	3.0	12.9	vhdl	5	T80a	yes	yes	N	N	64K	64K	Y				2002	2011	z80 data sheets	Z80 & 8080 inst sets, several usage	
A	1	dalton_8051		stable	Tony Givargis	8051	8	8x	kintex-7-3	James Brakef		2725	6	1	1	105	##		14.7	0.33	1.0	12.7	vhdl	7	i8051_all	yes	yes	N	N	64K	64K	Y				1999	2003	8051 data sheets	ASIC	www.cs.ucr.edu/~dalton/
A	1	zet86	Zet The x86 (IA-3	alpha	Zeus Marmolejo	8086	8	8x	kintex-7-3	James Brakef		3642	6	1		68	##		14.7	0.67	1.0	12.5	verilog	32	fpga_zet	yes	yes	N	N	1M	1M	Y				2008	2014	x86 data sheets	equivalent to 80186, boots MS-DOS	zet.aluzina.org/index.php/Zet_processor
A	1	nextz80	NextZ80	stable	Nicolae Dumitrache	Z80	8	8x	kintex-7-3	James Brakef		1064	6			106	##		14.7	0.33	3.0	10.9	verilog	3	NextZ80C	yes	yes	N	N	64K	64K	Y				2011	2014	z80 data sheets		
A	1	6809_6309	6809_6309_com	beta	Alejandro Paz Schmidt	6809	8	8x	kintex-7-3	James Brakef		2207	6			212	##		14.7	0.33	3.0	10.6	verilog	5	MC6809_cpu	yes	yes	N	N	64K	64K	Y				2012	2013	6809 data sheets	includes 6309 op-codes, xilinx & lattice	projects
A	1	system11		alpha	John Kent, David Burne	68HC11	8	8x	kintex-7-3	James Brakef		1218	6			153	##		14.7	0.33	4.0	10.3	vhdl	17	cpu11	yes	yes	N	N	64K	64K	Y				2003	2009	6811 data sheets	known bugs & untested instructions	
A	1	m65c02	M65C02	mature	Michael Morris	6502	8	8x	spartan-3	Michael Mor		661	4	0	3	74				0.33	4.0	9.2	verilog	13	M65C02	yes	yes	N	N	64K	64K	Y				2013	2014	6502 data sheets		
A	1	system09	SOC:system09	stable	John Kent	6809	8	8x	kintex-7-3	James Brakef		1945	6			154	##		14.7	0.33	3.0	8.7	vhdl	40	cpu09l	yes	yes	N	N	64K	64K	Y				2003	2012	6809 data sheets	from John Kent web page	
A	1	light52	Lightweight 805	beta	Jose Ruiz	8051	8	8x	kintex-7-3	James Brakef		1027	6	1	1	148	##		14.7	0.33	6.0	7.9	vhdl	8	light52_c	yes	yes	N	N	64K	64K	Y				2012	2013	8051 data sheets	targeted to balanced	~ 6 clocks/inst
A	1	w11	PDP-11/70 CPU (	alpha	Walter Mueller	PDP11	8	16x	spartan-6	Walter Muell		3418	6			80				0.67	2.0	7.8	vhdl	26	pdp11	yes	yes	N	N	4M	4M	Y		8		2010	2013	PDP11 data sheets	Boots UNIX, has MMU & cache, retro project	
A	1	wb_z80	Wishbone High F	stable	Brewster Porcella	Z80	8	8x	kintex-7-3	James Brakef		2025	6			144	##		14.7	0.33	3.0	7.8	verilog	4	z80_core	yes	yes	N	N	64K	64K	Y				2004	2012	z80 data sheets	derived from Guy Hutchison TV80	
A	1	cpu6502_true	cpu6502_tc	stable	Jens Gutschmidt	6502	8	8x	kintex-7-3	James Brakef		1678	6			159	##		14.7	0.33	4.0	7.8	vhdl	7	r6502_tc		yes	N	N	64K	64K	Y				2008	2010	6502 data sheets		
A	1	t48	T48 uController	stable	Arnim Laeuger	MCS-48	8	8x	cyclone-1	Arnim Laeuge		738	4		1	59				0.33	4.0	6.6	vhdl	70	t48_core	yes	asm	N		256	1K					2004	2009	MCS-48 data sheets	used in several projects	
A	1	t51	T51 mcu	stable	Andreas Voggeneder	8051	8	8x	kintex-7-3	James Brakef		1942	6	1		147	##		14.7	0.33	4.0	6.2	vhdl	17	T8032	yes	yes	N	N	64K	64K	Y				2002	2010	8032 data sheets	8052 & 8032	8032 SoC
A	1	turbo8051	turbo 8051	beta	Dinesh Annayya	8051	8	8x	kintex-7-3	James Brakef		1985	6	1		127	##		14.7	0.33	4.0	5.3	verilog	74	oc8051_t	yes	yes	N	N	64K	64K	Y				2011	2013	8051 data sheets	includes perpherials	
A	1	hc11core		stable	Green Mountain Comp	68HC11	8	8x	kintex-7-3	James Brakef		2190	6			127	##		14.7	0.33	4.0	4.8	vhdl	1	hc11rtl	yes	yes	?	N	64K	64K	N	53	8	2	2000		6811 data sheets	restricted use license, with corrections	http://www.gmvhdl.com/hc11core.html
A	1	df6805		proprietar	Hitech Global	6805	8	8x	stratix-1	Hitech Globa		1690	4			83				0.33	4.0	4.1	not avail			yes	yes	N	N	64K	64K	Y						6805 data sheets		www.hitechglobal.com/IPCores/DF6805.htm
A	1	cpu8080	8080 Compativle	stable	Scott Moore	8080	8	8x	spartan-6-3	James Brakef		1269	6			129	##		14.7	0.33	9.0	3.7	verilog	1	m8080	yes	yes	N	N	64K	64K	Y				2006	2009	8080 data sheets	includes VGA display generator, three	variants
B	1	68hc08	68hc08	stable	Ulrich Riedel	6808	8	8x	kintex-7-3	James Brakef		2290	6			101	##		14.7	0.33	4.0	3.6	vhdl	1	x68ur08		yes	N	N	64K	64K	Y				2007	2009	6808 data sheets		
A	1	lattice6502	Lattice 6502	beta	Ian Chapman	6502	8	8x	kintex-7-3	James Brakef		4942	6			214	##		14.7	0.33	4.0	3.6	vhdl	3	ghdl_pro	yes	yes	N	N	64K	64K	Y				2010	2010	6502 data sheets	targeted to LCMXO2280	huge LUT count
A	1	z80soc	Z80 System on C	stable	Ronivon Costa	Z80	8	8x	spartan-3e-	James Brakef		2474	4	2	19	78	##		14.7	0.33	3.0	3.4	vhdl	19	top_s3e	yes	yes	N	N	64K	64K	Y				2008	2010	z80 data sheets	based on Daniel Wallner's T80	
A	1	cpu86		beta	ht-lab.com	8086	8	8x	kintex-7-3	James Brakef		3421	6	1		127	##		14.7	0.17	2.0	3.1	vhdl	23	cpu86_to	yes	yes	N	N	1M	1M	Y				2002	2010	x86 data sheets	8088 clone	www.ht-lab.com
A	1	mc8051		stable	Helmut Mayrhofer	8051	8	8x	kintex-7-3	James Brakef		3022	6	1		83	##		14.7	0.33	4.0	2.3	vhdl	49	mc8051c	yes	yes	N	N	256	64K	Y				1999	2013	www.oreganosystem	fast 8051, version available with floating-point by David Lundgren	
A	1	hd63701	HD63701 compa	planning	Tsuyoshi Hasegawa	6801	8	8x	spartan-6-3	James Brakef		1412	6	1	3	31	##		14.7	0.33	4.0	1.8	verilog	6	HD63701_CORE			N	N	64K	64K	Y				2014			Used in Atari game console, 6801 clone?	
A	1	system68	System68	stable	John Kent, David Burne	6801	8	8x	spartan-3-5	James Brakef		2235	4		4	46	##		14.7	0.33	4.0	1.7	vhdl	21	cpu68	yes	yes	N	N	64K	64K	Y				2003	2009	6801 data sheets		
A	1	k68	K68	alpha	Shawn Tan	68000	8	16x	kintex-7-3	James Brakef		2392	6			24	##		14.7	0.67	4.0	1.7	verilog	15	k68_cpu	yes	yes	N	N	4K	4G	Y		16		2003	2009	68000 data sheets	68K binary compatible	
W	1	jane_nn		stable	Suresh Devanathan	RISC	4	8	kintex-7-3	James Brakef		723	6			178	##		14.7	0.33	1.0	81.4	vhdl	3	Processor	yes							27	16		2002			neural network microprocessor, specialized registers	
	1	mcs-4	4004 CPU & MCS	alpha	Reece Pollack	4004	4	4	kintex-7-3	James Brakef		228	6			376	##		14.7	0.16	4.0	66.0	verilog	7	i4004			N		4K	4K	N				2012	2012	4004 data sheets	4004 was multi-chip	clks/inst is approx
A	1	t400	T400 uController	stable	Arnim Laeuger	COP400	4	8x	cyclone-1	Arnim Laeuge		583	4		2	59				0.17	4.0	4.3	vhdl	53	t400_cor	yes	asm	N		256	1K					2006	2009	COP400 data sheets	several variants	

		_uP_cores_test folder	opencores name	status	author	style / clone	data size	inst size	FPGA	reporter	comment	LUTs ALM	LUT?	mults	blk ram	F max	date	tool ver	MIPS /clk	clks/ inst	KIPS /LUT	src code	# src files	top file	doc	tool chain	fltg pt	Ha vd	max data	max inst	byte adrs	# inst	# reg	pipe len	start year	last revis	reference	note worthy	comments
W	1	lem1_9	lem1_9	stable	James Brakefield	accum	1	9	kintex-7	James	Brakef	40	6		1	358	##	14.5	0.04	1.0	357.5	vhdl	3	lem1_9m	yes	asm	N	Y	64	2K	N	8	64	1	2003	2009		very small, 2 pipe stage is faster with r	"logic emulation machine"

79 ## 34 # usable(beta, stable or mature): "A"(clones) & "W"(originals) 9 ## ## ## # adrs

3 24 "B" or "X" of limited interest **171 unique usable designs**

Web page DMIPS per clock cycle per core en.wikipedia.org/wiki/Instructions_p community.freescale. www.eembc.org/coremark/index.php

MIPS/MHz Pro-rating for data size:

1-bit 0.04
8-bit 0.33
16-bit 0.67
32-bit 1.00

Under the assumption that the core is capable of one instuction per clock

Silicon Area equivalents

LUTS/DSP48 16:1
LUTS/Block RAM 32:1

Following has DMIPS per clock for many microprocessors
http://en.wikipedia.org/wiki/Instructions_per_second

uP	MIPS		CoreMarks /MHz	MHz		guessed average clocks/inst
4004	0.10					
6502	0.50		0.02	0.06		4
8051	0.01	DMIPS	0.08	0.24		1, 4 or 6
8080	0.17			0.25		9
68K	0.10			0.15		4
ARM Cortex A9	2.50	DMIPS		2.90	1000	
ARM Cortex M0	0.90	DMIPS		1.50	70	
ARM Cortex M3	1.25	DMIPS		2.17	25	
ARM7	0.90		0.74	2.04	600	
AVR	1.00		0.21	0.53	8	
AVR32				1.62	60	
BA21				2.44	400	
Coldfire				2.80	400	
Coldfire				0.77	150	Virtex-5 2
HCS08			0.04	0.12		4
HC11						4
LEON3/Spartan-6				1.96	100	
MC6809	1.24		0.07	1.86		3
MicroBlaze 3-stage	1.03			1.50		
MicroBlaze 5-stage	1.38			1.90	125	
MIPS32	1.51			2.28		
MSP430			0.40	1.20		2
MSP430				1.10	25	2
Nios II	0.64	DMIPS		0.93	200	
Nios II -e	0.15	DMIPS		0.25		
Nios II -f	1.13	DMIPS		1.60	200	
PIC16	0.25					
PIC18				0.04	40	
PIC24			0.72	1.86	40	
PIC32				3.45	80	
Super H-2				1.44	180	
VAX780	1.00	DMIPS		1.50		DMIPS # is by definition
Z80	1.60		0.01	0.03		3
eSi-1600				1.98		

Column Titles	Details
"A"	A: 1st choice clone, B: 2nd choice clone, W: 1st choice original, X: 2nd choice original
"B"	used to indicate best KIPS/LUT for a given design, usually using fast FPGA family
_uP_cores_test folder	if opencores design is their folder name, otherwise my folder name
opencores name	
status	ASIC, planning, alpha, beta, stable, mature, proprietary
author	First Name, Last Name
style / clone	part number or "forth", RISC, accumulator, etc
data size	data memory word size
inst size	instruction size
FPGA	FPGA family for compile, place, route & timing, usually using fastest part grade
reporter	First Name, Last Name
comments	compile, place, route & timing problems
LUTs ALM	4-LUT, 6-LUT, Altera ALM, Actel Tile
LUT?	total number of LUTs or ALMs used including route-thrus & otherwise unavailable
mults	total number of multipliers/DSPs used; 9x9 multiplier counts divided by two and rounded up
blk RAM	total # of block RAMs used, Xilinx half block RAM counts divided by two and rounded up, Altera count is percent used times # avail
Fmax	maximum primary clock speed from compile, place, route & timing run
date	date of compile, place & route; serves to identify source version
tool ver	Altera, Xilinx, Lattice Semiconductor or MicroSemi tool version number
MIPS /clk	prorated DMIPS per clock, reduced for data word sizes under 32-bits, greater than one for multiple issue processors
clks/ inst	number of clocks per instruction, typically 1.0 for modern pipelined processors, subjective for older uP
KIPS /LUT	figure of merit, does not include effects of memory capacity, floating point or instruction set quality
src code	VHDL or Verilog or System Verilog or schematic or gates
# src files	number of source files for compile, place, route & timing
top file	top file for compile, place, route & timing run
doc	is documentation provided
tool chain	is there a compiler or assembler provided or available
fltg pt	does the compile, place, route & timing run include floating point
Ha vd	separate instruction and data memory(s), there can be more than one data memory, M for MMU & caches
max data	maximum data address
max inst	maximum instruction address
byte adrs	is byte addressing provided
# inst	number of unique instructions, somewhat subjective
# reg	number of registers in register file
pipe len	number of pipeline stages
start year	year of first design activity
last revis	last year for revisions
reference	web address or generic information (for clones)
note worthy	anything special about the design
comments	catchall