

Opencore and other soft core processors

| uP_cores_t est folder | opencore name | status | author | style / clone | data size | inst size | FPGA | repor ter | com ment | LUTs ALUT | LUT: m | blks ram | F max | Date | tool ver | MIPS /clk | clks/ inst | KIPS /LUT | src code | # src files | top file | doc | tool chain | flt pt | Ha vd | max data | max inst | byte adrs | # inst | # reg | pipe len | start year | last revis | reference | note worthy | comments | | | |
|-----------------------|----------------|------------------|-----------------------|--------------------------|-----------|-----------|------------|---------------|---------------|-----------|--------|----------|-------|------|----------|-----------|------------|-----------|-----------|-------------|----------|------------|------------|--------|-------|----------|----------|-----------|--------|-------|----------|------------|--|--|--|--|---|-------------------------|--|
| A 1 | cray1 | alpha | Christopher Fenton | cray1 | 64 | 16 | kintex-7-3 | James Brakef | 13463 | 6 | 19 | 10 | 127 | ## | 14.7 | 6.00 | 1.0 | 56.6 | verilog | 46 | cray_sys | yes | yes | Y | N | 4M | 4M | N | | 512 | 2010 | | CRAY data sheets | homebrew Cray1 | www.chrisfenton.com/homebrew-cray-1a/ | | | | |
| W 1 | fpgamix | stable | Tommy Thorn | RISC | 64 | 32 | aria-2 | James Brakef | 11605 | A | 8 | 10 | 94 | ## | 13.1 | 1.50 | 4.0 | 3.0 | system v | 2 | core | yes | yes | Y | Y | 4G | 4G | Y | 256 | 288 | 2006 | 2008 | | clone of Knuth's MMIX | micro-coded | | | | |
| A 1 | s1_core | S1 Core | Fabrizio Fazzino etal | SPARC | 64 | 32 | kintex-7-3 | James Brakef | 54434 | 6 | 8 | 57 | 50 | ## | 14.7 | 1.00 | 1.0 | 0.9 | verilog | 136 | s1_top | yes | yes | N | N | 4G | 4G | Y | 32 | | 2007 | 2012 | SPARC data sheets | reduced version of OpenSPARC T1 | | | | | |
| A 1 | microblaze | proprieta | Xilinx | uBlaze | 32 | 32 | kintex-7 | Xilinx | 546 | 6 | | 1 | 320 | | | 1.03 | 1.0 | 603.7 | not avail | | | yes | yes | opt | | 4G | 4G | Y | 86 | 32 | 3 | 2002 | | www.xilinx.com/tools | MicroBlaze MCS, smallest configuration | 70 configuration options, MMU optional | | | |
| A 1 | ARM_Cortex_A9 | ASIC | ARM | ARM a9 | 32 | 16 | aria-7 | altera | 4500 | A | | | 1050 | | | 2.50 | 1.0 | 583.3 | asic | | | yes | yes | Y | Y | 4G | 4G | Y | 80 | 16 | 10 | | 2012 | | altera data sheets | uses pro-rated LC area | dual issue, includes fltg-pt & MMU & caches | | |
| A 1 | nios2 | proprieta | Altera | Nios II | 32 | 32 | stratix-5 | Altera | 895 | A | | | 310 | | | 1.13 | 1.0 | 389.7 | not avail | | | yes | yes | opt | | 4G | 4G | Y | 32 | | 2004 | | Nios2 data sheets | flt-pt, caches & MMU options | Nios II/f: fastest version | | | | |
| W 1 | hive | stable | Eric Wallin | 4-8 sthck | 32 | 16 | yclone-5 | James Brakef | 628 | A | 3 | 3 | 217 | ## | 13.1 | 1.00 | 1.0 | 345.0 | verilog | | core | yes | yes | N | | | | N | 40 | 10 | 8 | 2013 | 2014 | | 4-8 symmetrical stacks, eight threads via pipeline barrel | | | | |
| W 1 | microcore | beta | Klaus Schleisiek | forth | 32 | 8 | kintex-7-3 | James Brakef | 644 | 6 | | | 149 | ## | 14.7 | 1.00 | 1.0 | 231.3 | vhdl | 10 | core | yes | asm | N | Y | 2M | 512K | | | | 2004 | | | has several PDFs | indexing into return stack, auto inc/de | AKA uCore110 | | | |
| A 1 | mips789 | mips789 | stable | Li Wei | MIPS | 32 | 32 | kintex-7-3 | James Brakef | 1432 | 6 | | 1 | 171 | ## | 14.7 | 1.00 | 1.0 | 119.1 | verilog | 10 | mips_cor | yes | yes | N | | 4G | 4G | Y | 32 | | 2007 | 2009 | MIPS data sheets | | | | | |
| W 1 | ensilica | proprieta | ensilica.com | eSi-3200 | 32 | | stratix-4 | ensilica | 1800 | A | | | 200 | | | 1.00 | 1.0 | 111.1 | not avail | | | yes | yes | | | 4G | 4G | | 16 | 5 | | | | www.ensilica.com | verilog source included with license | 10 addressing modes | | | |
| A 1 | ion | ion MIPS compa | mature | Jose Ruiz | MIPS | 32 | 32 | kintex-7-3 | James Brakef | 1533 | 6 | | 163 | ## | 14.7 | 1.00 | 1.0 | 106.0 | vhdl | 12 | mips_soc | yes | yes | N | | 4G | 4G | Y | 32 | | 2011 | 2014 | | | | | MIPS R3000 clone | | |
| X 1 | jam | stable | Johan Thelin etal | RISC | 32 | 32 | kintex-7-3 | James Brakef | 1369 | 6 | | | 143 | ## | 14.7 | 1.00 | 1.0 | 104.2 | vhdl | 17 | cpu | yes | yes | N | Y | 128K | 128K | | 32 | 5 | 2002 | | | | | | serial multiply & divide | | |
| A 1 | ucore | Ucore | stable | Whitewill | MIPS | 32 | 32 | kintex-7-3 | James Brakef | 2469 | 6 | | 1 | 231 | ## | 14.7 | 1.00 | 1.0 | 93.5 | verilog | 25 | ucore | yes | yes | N | | 4G | 4G | Y | 32 | 6 | 2005 | 2010 | | MIPS data sheets | MMU & caches | | | |
| W 1 | altor32_lite | AltOr32 | stable | Ultra Embedded | OpenRISC | 32 | 32 | aria-2 | James Brakef | 1809 | A | | | 161 | ## | 13.1 | 1.00 | 1.0 | 88.8 | system v | 8 | altor32 | yes | yes | N | | 4G | 4G | Y | 32 | | 2012 | 2014 | OpenRISC 1000 | simplified OpenRISC 1000 | LPMS & systemVerilog | | | |
| A 1 | openfire2 | OpenFIRE | beta | Antonio Anton | uBlaze | 32 | 32 | kintex-7-3 | James Brakef | 1201 | 6 | 3 | 2 | 105 | ## | 14.7 | 1.00 | 1.0 | 87.4 | verilog | 27 | openfire2 | yes | yes | N | N | 4G | 4G | Y | 32 | | 2007 | 2012 | uBlaze data sheets | "FPGA Proven" | derived from Stephen Craven's OpenFire | | | |
| A 1 | storm_core | Storm Core (ARN | beta | Stephan Nolting | ARM7 | 32 | 32 | kintex-7-3 | James Brakef | 2312 | 6 | 3 | | 179 | ## | 14.7 | 1.00 | 1.0 | 77.4 | vhdl | 16 | CORE | yes | yes | N | | 4G | 4G | Y | 32 | 8 | 2011 | 2014 | | | | I & D caches not compiled | | |
| A 1 | aspida | ASPIDA DLX core | stable | Sotiriou | DLX | 32 | 32 | kintex-7-3 | James Brakef | 3586 | 6 | | | 257 | ## | 14.7 | 1.00 | 1.0 | 71.7 | verilog | 10 | DLX_top | yes | yes | | | 4G | 4G | | | | 2002 | 2009 | | Knuth DLX | compiled sync version | | | |
| A 1 | m1_core | M1 Core | beta | Fabrizio Fazzino, Albert | MIPS? | 32 | 32 | kintex-7-3 | James Brakef | 3456 | 6 | | | 233 | ## | 14.7 | 1.00 | 1.0 | 67.3 | verilog | 9 | m1_core | yes | yes | N | | 4G | 4G | Y | 32 | | 2007 | 2012 | | | | GCC target? | | |
| X 1 | risco | beta | Niklaus Wirth | RISC | 32 | 32 | kintex-7-3 | James Brakef | 1186 | 6 | 4 | 6 | 110 | ## | 14.7 | 0.67 | 1.0 | 61.9 | verilog | 8 | RISCO | yes | yes | N | | 4G | 4G | | | | 2011 | | | | | | minimalist Wirth, education tool | | |
| A 1 | secretblaze | beta | Lyonel Barthe | uBlaze | 32 | 32 | spartan-3 | Lyonel Barthe | 1563 | 4 | | | 91 | | | 12.1 | 1.00 | 1.0 | 58.2 | vhdl | 26 | sb_core | yes | yes | | | 4G | 4G | Y | 86 | 32 | 5 | 2010 | 2012 | www.lirmm.fr/ADAC/ | | | | |
| W 1 | latticemicro32 | stable | Yann Siommeau, Micha | RISC | 32 | 32 | kintex-7-3 | James Brakef | 2292 | 6 | 3 | 8 | 155 | ## | 14.7 | 0.80 | 1.0 | 54.2 | verilog | 24 | lm32_cpu | yes | yes | N | | 4G | 4G | Y | 32 | | 2006 | 2012 | | | en.wikipedia.org/wiki | optional data & inst caches | | | |
| X 1 | eco32 | SOC:ECO32 | stable | Hellwing Geisse | RISC | 32 | 32 | kintex-7-3 | James Brakef | 2210 | 6 | | 1 | 160 | | 14.7 | 1.00 | 1.5 | 48.1 | verilog | 23 | cpu | yes | yes | N | | 512M | 256M | Y | 61 | 32 | 2003 | 2014 | | | | MIPS like, slow mul & div | | |
| X 1 | qris32 | qris32 wsbhonn | alpha | Vlachias | RISC | 32 | 32 | aria-2 | James Brakef | 3075 | A | 4 | | 144 | ## | 13.1 | 1.00 | 1.0 | 46.9 | system v | 8 | qris32 | yes | yes | N | | 4G | 4G | Y | 32 | 4 | 2010 | 2011 | | | | for PhD thesis | | |
| A 1 | minimips | miniMIPS | stable | Poppy etal | MIPS | 32 | 32 | kintex-7-3 | James Brakef | 2939 | 6 | 8 | | 118 | ## | 14.7 | 1.00 | 1.0 | 40.1 | vhdl | 12 | minimips | yes | yes | N | | 4G | 4G | Y | 32 | 5 | | | | | MIPS I | | | |
| W 1 | ba22 | proprieta | CAST Inc | RISC | 32 | 16x | spartan-6 | CAST Inc | 1800 | 6 | | 32 | 72 | | | 1.00 | 1.0 | 40.0 | not avail | | | yes | yes | | | 4G | 4G | | | | | | | www.cast-inc.com | | | | | |
| A 1 | plasma | Plasma most Mi | stable | Steve Rhoads | MIPS | 32 | 32 | kintex-7-3 | James Brakef | 2462 | 6 | | 3 | 97 | ## | 14.7 | 1.00 | 1.0 | 39.5 | vhdl | 22 | plasma | yes | yes | N | | 4G | 4G | Y | 32 | | 2001 | 2013 | MIPS data sheets | wide outside use, opencore page has list of related publications | | | | |
| W 1 | risC5 | beta | Niklaus Wirth | RISC | 32 | 32 | kintex-7-3 | James Brakef | 2441 | 6 | 4 | 1 | 92 | ## | 14.7 | 1.00 | 1.0 | 37.8 | verilog | 8 | RISC5 | yes | yes | Y | | 4G | 4G | | 16 | | 2013 | | | | | | minimalist Wirth, part of Project Oberon | 32x32 multiplier | |
| A 1 | mipsr2000 | mipsr2000 | stable | Lazaridis Dimitris | MIPS | 32 | 32 | kintex-7-3 | James Brakef | 1971 | 6 | 4 | 6 | 71 | ## | 14.7 | 1.00 | 1.0 | 36.2 | vhdl | 35 | Dm | yes | yes | N | | 4G | 4G | Y | 32 | 5 | 2012 | 2013 | | MIPS data sheets | course project | | | |
| W 1 | nige_machine | stable | Andrew Read | forth | 32 | 8 | kintex-7-3 | James Brakef | 5033 | 6 | 8 | 33 | 123 | ## | 14.7 | 1.00 | 1.0 | 24.5 | vhdl | 29 | Board | yes | yes | N | | 16M | 16M | | 512 | 512 | | 2014 | | | | | | standalone Forth system | |
| W 1 | minsoc | minsoc | stable | Raul Fajardo etal | OpenRISC | 32 | 32 | kintex-7-3 | James Brakef | 4945 | 6 | 4 | 8 | 107 | ## | 14.7 | 1.00 | 1.0 | 21.7 | verilog | 88 | or1200_top | yes | yes | Y | M | 4G | 4G | Y | 32 | | 2009 | 2013 | www.minsoc.com | minimal OR1200, vendor neutral, has caches | | | | |
| A 1 | aquarius | aquarius | stable | Thorn Atch | SuperH-2 | 32 | 16 | kintex-7-3 | James Brakef | 3958 | 6 | 2 | | 86 | ## | 14.7 | 1.00 | 1.0 | 21.6 | verilog | 21 | top | yes | yes | N | | 4G | 4G | Y | | | 2003 | 2009 | SuperH data sheets | | | | | |
| A 1 | mips32r1 | MIPS32 Release | stable | Graat Ayers | MIPS | 32 | 32 | aria-2 | James Brakef | 3716 | A | 8 | | 79 | ## | 13.1 | 1.00 | 1.0 | 21.3 | verilog | 20 | processor | yes | yes | N | | 4G | 4G | Y | 32 | | 2012 | 2014 | MIPS data sheets | Harvard arch | | | | |
| W 1 | zpu | ZPU the worlds s | stable | Oyvind Harboe | forth | 32 | 8 | spartan-6 | Oyvind Harboe | 1259 | 6 | | | 135 | | 0.10 | 1.0 | 10.7 | vhdl | 23 | zpu_core | yes | yes | N | | 4G | 4G | Y | 37 | | 2008 | 2009 | www.zylin.com | zpu4: 16 & 32 bit versions, code size 80% of ARM (thumb), low MIPS/MHz | | | | | |
| A 1 | amber | Amber ARM-com | stable | Conor Santifort | ARM7 | 32 | 32 | kintex-7-3 | James Brakef | 6409 | 6 | | 2 | 82 | ## | 14.7 | 0.75 | 1.0 | 9.6 | verilog | 25 | a23_core | yes | yes | N | | 4G | 4G | Y | 3 | 2010 | 2013 | ARM7 data sheets | no MMU, shared cache | 2048 LUTs used as single port RAM | | | | |
| A 1 | amber | Amber ARM-com | stable | Conor Santifort | ARM7 | 32 | 32 | kintex-7-3 | James Brakef | 12450 | 6 | | 4 | 98 | ## | 14.7 | 1.05 | 1.0 | 8.2 | verilog | 25 | a25_core | yes | yes | N | Y | 4G | 4G | Y | 5 | 2010 | 2013 | ARM7 data sheets | no MMU, data & inst caches | 4096 LUTs used as single port RAM | | | | |
| X 1 | edge | Edge Processor (| alpha | Hesham ALMATary | MIPS | 32 | 32 | spartan-6-3 | James Brakef | 5345 | 6 | 7 | 1 | 8 | ## | 14.7 | 1.00 | 1.0 | 1.5 | verilog | 30 | edge_cor | yes | yes | N | N | 4G | 4G | Y | 32 | 5 | 2014 | | MIPS data sheets | MIPS1 clone | | | | |
| A 1 | ao486 | ao486 | beta | Aleksander Osman | x86 | 32 | 8x | yclone-4-7 | James Brakef | 35872 | 4 | 4 | 34 | 44 | ## | 13.1 | 1.00 | 1.0 | 1.2 | verilog | 85 | ao486 | yes | yes | | | 4G | 4G | Y | | | 2014 | 2014 | x86 data sheets | complete 486, SoC configuration | non-SoC, no MMU | | | |
| A 1 | pdp1 | PDP-1 reimplem | alpha | Yann Vernier | x86 | 18 | 18 | spartan-3a | James Brakef | 1390 | 4 | | 6 | 138 | ## | 14.7 | 0.50 | 10.0 | 5.0 | vhdl | | top | yes | yes | N | N | 4K | 4K | | 28 | | 2011 | 2011 | http://pdp-1.computer | PDP-1 descended from MIT TX-0 | uses Minimal UART from opencores | | | |
| X 1 | IDEA | proprieta | Liu Cheah etal | RISC | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| | up_cores_t | opencores | status | author | style/clone | data size | inst size | FPGA | reporter | comment | LUTs | LUT? | mults | blk ram | F max | date | tool ver | MIPS /clk | clks/inst | KIPS /LUT | src code | # src files | top file | doc | tool chain | ftg pt | Ha vd | max data | max inst | byte adrs | # inst | # reg | pipe len | start year | last revis | reference | note worthy | comments | |
|---|------------|----------------|---------------------|-----------|-------------------------|-----------|-----------|------|-------------|----------------|------|------|-------|---------|-------|------|----------|-----------|-----------|-----------|----------|-------------|--------------|------|------------|--------|-------|----------|----------|-----------|--------|-------|----------|------------|------------|--|---|--|---------------------------------------|
| X | 1 | marca | McAdam's RISC | stable | Wolfgang Puffitsch | RISC | 16 | 16 | aria-2 | James Brakef | 1763 | A | | 22 | 157 | ## | 13.1 | 0.67 | 6.0 | 10.0 | vhdl | 40 | marca | yes | asm | N | 8K | 16K | | 75 | 16 | 4 | 2007 | 2009 | | serial multiply & divide | clks/inst is approx | | |
| A | 1 | tg68 | TG68 execute 68 | stable | Tobias Gubener | 68000 | 16 | 16x | kintex-7.3 | James Brakef | 2331 | 6 | | | 44 | ## | 14.7 | 0.67 | 4.0 | 3.2 | vhdl | 2 | TG68_fas | yes | yes | N | N | 4G | 4G | Y | | 16 | | 2007 | 2012 | 68000 data sheets | for use with Minimig | | |
| A | 1 | suska-III | | beta | Wolfgang Forster | 68000 | 16 | 16x | aria-2 | James Brakef | 7388 | A | | | 55 | ## | 13.1 | 0.67 | 4.0 | 1.3 | vhdl | 11 | wf68k00i | yes | yes | N | N | 4G | 4G | Y | | 16 | | 2003 | 2013 | 68000 data sheets | for use as an Atari ST | http://www.experiment-s.de/en/ | |
| X | 1 | vtach | VTACH Bell Labs | mature | Al Williams | | 13 | 12 | spartan-3-4 | James Brakef | 557 | 4 | | | 71 | ## | 14.7 | 0.50 | 1.0 | 64.1 | verilog | 16 | vtach | | | N | | 256 | 256 | Y | | | | 2007 | 2013 | | ISE project only, BCD arithmetic | | |
| X | 1 | usimplez | MicroSimplez | stable | Pablo Salvadeo etal | accum | 12 | 12 | stratix-2 | Pablo Salvadeo | 48 | 4 | | | 134 | ## | 9.1 | 0.17 | 1.0 | 475.9 | vhdl | 3 | usimplez_cpu | | | N | | 512 | 512 | | 8 | | | 2011 | | http://www.gti-det.u | part of university course, simplez+4h | MIPS/Mhz reduced due to few inst | |
| A | 1 | pdp8verilog | | stable | Brad Parker | PDP8 | 12 | 12 | kintex-7.3 | James Brakef | 505 | 6 | | | 366 | ## | 14.7 | 0.50 | 2.0 | 181.3 | verilog | 18 | pdp8 | yes | yes | N | N | 32K | 32K | | | 8 | | 2005 | 2010 | PDP8 data sheets | boots & runs TSS/8 & Basic | www.heeltoe.com/download/pdp8/README.html | |
| A | 1 | pdp8 | PDP-8 Processor | alpha | Joe Manojlovick, Rob D | PDP8 | 12 | 12 | kintex-7.3 | James Brakef | 1219 | 6 | 1 | | 183 | ## | 14.7 | 0.50 | 2.0 | 37.5 | vhdl | 55 | cpu | yes | yes | N | N | 32K | 32K | | | 8 | | 2012 | 2013 | PDP8 data sheets | Boots OS/8, runs apps, several variants | | |
| A | 1 | pdp8l | Minimal PDP8/L | beta | Ian Schofield | PDP8 | 12 | 12 | cyclone-3 | James Brakef | 1088 | 4 | | 48 | 63 | ## | 14.7 | 0.50 | 2.0 | 14.4 | vhdl | 11 | top | yes | yes | N | N | 4K | 4K | | | | | 2013 | | | PDP8 data sheets | | |
| W | 1 | eric5 | | proprieta | enter-electronics.com | forth | 9 | 8 | cyclone-4-6 | enter-electro | 110 | 4 | opt | | 60 | | | 0.42 | 1.0 | 229.1 | | | | | | | 512 | 1K | | | 3-4 | | 2007 | | | 25 MIPS: ERIC5xs, ERIC5Q | | | |
| A | 1 | picoblaze | picoblaze | stable | Ken Chapman | picoblaze | 8 | 18 | kintex-7.3 | James ROM | 178 | 6 | | | 182 | ## | 14.7 | 0.33 | 2.0 | 168.9 | vhdl | 1 | kcpm3 | yes | asm | N | | 256 | 2K | Y | | | | 2003 | | | picoblaze data sheets | 2 clocks per inst | this is the original picoblaze author |
| A | 1 | avr8 | Reduced AVR Co | beta | Nick Kovach | AVR | 8 | 16 | kintex-7.3 | James Brakef | 174 | 6 | | | 418 | ## | 14.7 | 0.33 | 1.0 | 792.2 | verilog | 1 | rAVR | yes | yes | N | N | 64K | 64K | Y | 17 | 4 | | 2010 | 2010 | | AVR data sheets | not a full clone, doc is opencores page | |
| X | 1 | mcpu | MCPU A minima | stable | Tim Boscke | accum | 8 | 8 | spartan-6-3 | James Brakef | 41 | 6 | | | 384 | ## | 14.7 | 0.08 | 1.0 | 749.0 | vhdl | 1 | tb02cpu2u | yes | asm | N | N | 64 | 64 | Y | 4 | | | 2007 | 2014 | | fits into 32 macrocell CPLD | reduced MIPS/clock due to only 4 inst | |
| X | 1 | lwrrisc | ClairRISC | stable | Li Wu | accum | 8 | 12 | aria-2 | James Brakef | 88 | A | | 1 | 230 | ## | 13.1 | 0.17 | 1.0 | 443.6 | verilog | 9 | risc_core | yes | asm | N | Y | 256 | 2K | Y | 16 | | | 2008 | 2009 | | simplified PIC, 4 reg rtn stack | absolute addressing only, lowered MIPS/clock | |
| X | 1 | popcorn | | stable | Jeung Joon Lee | accum | 8 | 8x | kintex-7.3 | James Brakef | 267 | 6 | | | 347 | ## | 14.7 | 0.33 | 1.0 | 428.4 | verilog | 4 | pc | yes | yes | N | N | 64K | 64K | Y | 43 | | | 2000 | | | small 8 bit uP | | |
| A | 1 | risc16f84 | risc16f84 | stable | John Clayton | PIC16 | 8 | 14 | kintex-7.3 | James Brakef | 331 | 6 | | | 333 | ## | 14.7 | 0.33 | 1.0 | 332.3 | verilog | 1 | risc16f84 | yes | yes | N | Y | 256 | 4K | Y | | | | 2002 | 2013 | | PIC16 data sheets | derived from CQPIC by Sumio Morioka | |
| W | 1 | gunnut | | stable | Peter Ashenden | RISC | 8 | 18 | kintex-7.3 | James Brakef | 420 | 6 | | | 275 | ## | 14.7 | 0.33 | 1.0 | 216.2 | vhdl | 20 | gunnut-r | yes | asm | N | | 256 | 4K | Y | | 8 | | 2007 | | | see Digital Design: An Embedded System does not seem complete | | |
| W | 1 | dfp | dfp | stable | Ron Chapman | forth | 8 | Y | kintex-7.3 | James Brakef | 297 | 6 | | | 192 | ## | 14.7 | 0.33 | 1.0 | 213.2 | vhdl | 25 | DataFlow | yes | yes | N | | | | | | | | 2003 | 2009 | | 8-bitter, generates a custom VHDL state machine, compiler is in Forth | | |
| A | 1 | picoblaze | picoblaze | stable | Ken Chapman | picoblaze | 8 | 18 | spartan-3-4 | James Brakef | 178 | 4 | | | 182 | ## | 14.7 | 0.33 | 2.0 | 168.9 | vhdl | 1 | kcpm3 | yes | asm | N | | 256 | 2K | Y | | | | 2003 | | | picoblaze data sheets | 2 clocks per inst | this is the original picoblaze author |
| B | 1 | pic_coonan | | alpha | Tom Coonan | PIC16 | 8 | 14 | kintex-7.3 | James Brakef | 328 | 6 | 1 | | 165 | ## | 14.7 | 0.33 | 1.0 | 166.1 | verilog | 7 | piccpu | yes | yes | N | Y | 256 | 4K | Y | | | | 1999 | | | PIC16 data sheets | | |
| X | 1 | tisc | Tiny Instruction | beta | Vincent Crabtree | accum | 8 | 8x | kintex-7.3 | James Brakef | 195 | 6 | | | 87 | ## | 14.7 | 0.33 | 1.0 | 147.1 | vhdl | 1 | TISC | | | N | | 256 | 1K | Y | | 2 | | 2009 | 2009 | | minimal accumulator machine | | |
| A | 1 | free_risc8 | | stable | Thomas Coonan | PIC16 | 8 | 14 | kintex-7.3 | James Brakef | 355 | 6 | | | 142 | ## | 14.7 | 0.33 | 1.0 | 132.2 | verilog | 8 | cpu | yes | yes | N | | 256 | 4K | Y | | | | 2002 | 2011 | | PIC16 data sheets | | |
| W | 1 | open8_urisc | Open8 uRISC | stable | Kirk Hays, Jshamlet | RISC | 8 | 8 | kintex-7.3 | James Brakef | 691 | 6 | 1 | | 263 | ## | 14.7 | 0.33 | 1.0 | 125.6 | vhdl | 9 | Open8 | yes | yes | N | | 64K | 64K | Y | | 8 | | 2006 | 2013 | | accum & 8 regs, clone of Vautomation uRISC processor, in use | | |
| A | 1 | pacoblaze | | mature | Pablo Kocik | picoblaze | 8 | 18 | spartan-3 | Pablo Kocik | 177 | 4 | | 1 | 117 | ## | 14.7 | 0.33 | 2.0 | 109.1 | verilog | 18 | pacoblaze | yes | asm | N | | 256 | 2K | Y | 57 | 2 | | 2006 | | bleyer.org/pacoblaze | 3 versions, behavioral coding | | |
| X | 1 | myrisc1 | myRISC1 | stable | Muza Byte | RISC | 8 | 8 | cyclone-2 | Muza [Alter | 185 | 4 | | 1 | 57 | ## | 14.7 | 0.33 | 1.0 | 101.8 | verilog | 1 | myRISC1 | yes | asm | N | Y | 256 | 256 | Y | 16 | 4 | | 2011 | 2011 | | Verilog source included in PDF file | LPM macros | |
| A | 1 | navre | Navre AVR clone | stable | Sebastien Bourdeaudou | AVR | 8 | 16 | kintex-7.3 | James Brakef | 990 | 6 | | | 207 | ## | 14.7 | 0.33 | 1.0 | 69.0 | verilog | 1 | softusb_n | yes | yes | N | | 64K | 64K | Y | | 32 | 2 | 2010 | 2013 | | AVR data sheets | AVR clone, part of www.milkymist.org | |
| W | 1 | latticemicro8 | | stable | Lattice Semiconductor | RISC | 8 | 18 | LFE2 | Lattice Semic | 265 | 4 | | | 104 | ## | 14.7 | 0.33 | 2.0 | 64.4 | vhdl | 10 | isp8_core | yes | yes | N | | 256 | 4K | Y | | 32 | | 2005 | 2010 | | en.wikipedia.org/wiki | 16 deep call stack, four configurations | |
| X | 1 | erp | Educational RISC | stable | Lhazzadzik | RISC | 8 | 16 | spartan-3-5 | James Brakef | 366 | 4 | 1 | 1 | 70 | ## | 14.7 | 0.33 | 1.0 | 63.5 | verilog | 1 | ERPVerilog | yes | | | | | | | 15 | 6 | | 2004 | 2009 | | two report PDFs & one Verilog file | | |
| A | 1 | light8080 | Lightweight 8080 | stable | Jose Ruiz, Moti Litoche | 8080 | 8 | 8x | kintex-7.3 | James Brakef | 154 | 6 | | 1 | 247 | ## | 14.7 | 0.33 | 9.0 | 58.9 | verilog | 5 | i80soc | yes | yes | N | N | 64K | 64K | Y | | | | 2007 | 2012 | | 8080 data sheets | targeted to area, includes UART, interrupt | typically 9 clocks per inst, .04=33/9 |
| A | 1 | copyblaze | copyBlaze | stable | Abdallah Ellbrahimi | picoblaze | 8 | 18 | kintex-7.3 | James missir | 622 | 6 | | | 217 | ## | 14.7 | 0.33 | 2.0 | 57.5 | vhdl | 16 | cp_copybl | yes | asm | N | | 256 | 2K | Y | | | | 2011 | 2013 | | microBlaze data sheet | wishbone extras | does not infer RAM for registers |
| A | 1 | minirisc | Mini-Risc core | stable | Rudolf Usselmann | PIC16 | 8 | 14 | spartan-3 | Rudolf Usselr | 460 | 4 | | | 80 | ## | 14.7 | 0.33 | 1.0 | 57.4 | verilog | 7 | risc_core | yes | yes | N | Y | 256 | 4K | Y | | | | 2001 | 2012 | | PIC16 data sheets | | |
| A | 1 | avrtinyx64core | avrtinyx64core | beta | Andreas Hilvarsson | AVR | 8 | 16 | kintex-7.3 | James Brakef | 1243 | 6 | | | 194 | ## | 14.7 | 0.33 | 1.0 | 51.5 | vhdl | 1 | mcu_core | yes | yes | N | | 64K | 128K | Y | | 32 | | 2008 | 2009 | | AVR data sheets | | |
| A | 1 | avr_hp | avr_hp | stable | Strauch Tobias | AVR | 8 | 16 | kintex-7.3 | James [2 slot | 1554 | 6 | | | 223 | ## | 14.7 | 0.33 | 1.0 | 47.4 | vhdl | 10 | avr_core | some | yes | N | | 64K | 128K | Y | | 32 | | 2010 | 2010 | | AVR data sheets | hyper pipelined (eg barrel) AVR | |
| X | 1 | micro8a | | beta | John Kent | accum | 8 | 16 | kintex-7 | James Brakef | 531 | 6 | | | 204 | ## | 14.7 | 0.33 | 3.0 | 42.3 | vhdl | 11 | Micro8 | yes | asm | N | N | 2K | 2K | Y | | | | 2002 | 2002 | | members.optushome | derived from Tim Boscke's mcpu, not perfected | |
| A | 1 | t65 | T65 CPU | stable | Daniel Wallner | 6502 | 8 | 8x | kintex-7.3 | James Brakef | 575 | 6 | | | 291 | ## | 14.7 | 0.33 | 4.0 | 41.7 | vhdl | 7 | T65 | yes | yes | N | | 64K | 64K | Y | | | | 2002 | 2010 | | 6502 data sheets | 6502, 65C02 & 65C816; wide use | |
| W | 1 | natalius_8bit | Natalius 8 bit RISC | beta | Fabio Guzman | RISC | 8 | 16 | kintex-7.3 | James Brakef | 232 | 6 | 1 | 1 | 175 | ## | 14.7 | 0.11 | 3.0 | 27.7 | verilog | 12 | natalius_ | yes | asm | N | Y | 256 | 2K | Y | 29 | 8 | | 2012 | 2012 | | | return stack & register file | 3 clocks/inst |
| A | 1 | free6502 | | stable | David Kessner | 6502 | 8 | 8x | kintex-7.3 | James Brakef | 646 | 6 | | | 193 | ## | 14.7 | 0.33 | 4.0 | 24.6 | vhdl | 5 | free6502 | yes | yes | N | N | 64K | 64K | Y | | | | 1999 | 2000 | | 6502 data sheets | microcoded | |
| A | 1 | m16c5x | M16C5x | mature | Michael Morris | PIC16 | 8 | 14 | spartan-3-4 | Michael Mor | 1265 | 4 | 3 | 81 | ## | 14.7 | 0.33 | 1.0 | 21.1 | verilog | 3 | m16c5x | yes | yes | N | Y | 256 | 4K | Y | | | | 2013 | 2014 | | PIC16 data sheets | SOC LUT count | was P16C5X, name could be in flux | |
| B | 1 | 68hc05 | 68hc05 | stable | Ulrich Riedel | 6805 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| up_cores_test folder | opencores name | status | author | style / clone | data size | inst size | FPGA | reporter | comment | LUTs ALUT | LUT? | mults | blk ram | F max | date | tool ver | MIPS /clk | clks/ inst | KIPS /LUT | src code | # src files | top file | doc | tool chain | ftg pt | Ha vd | max data | max inst | byte adrs | # inst | # reg | pipe len | start year | last revis | reference | note worthy | comments |
|----------------------|----------------|--------|------------------|---------------|-----------|-----------|----------|--------------|---------|-----------|------|-------|---------|-------|------|----------|-----------|------------|-----------|----------|-------------|----------|-----|------------|--------|-------|----------|----------|-----------|--------|-------|----------|------------|------------|-----------|---|---------------------------|
| W 1 | lem1_9 | stable | James Brakefield | accum | 1 | 9 | kintex-7 | James Brakef | | 40 | 6 | | 1 | 358 | ## | 14.5 | 0.04 | 1.0 | 357.5 | vhdl | 3 | lem1_9m | yes | asm | N | Y | 64 | 2K | N | 8 | 64 | 1 | 2003 | 2009 | | very small, 2 pipe stage is faster with r | "logic emulation machine" |

79 ## 34 # usable(beta, stable or mature): "A"(clones) & "W"(originals) 9 ## ##
 3 24 "B" or "X" of limited interest 171 unique usable designs

Web page DMIPS per clock cycle per core en.wikipedia.org/wiki/Instructions_per_second community.freescale.com www.eembc.org/coremark/index.php

MIPS/MHz Pro-rating for data size:

| | | | |
|--------|------|---------------------------------|------|
| 1-bit | 0.04 | | |
| 8-bit | 0.33 | Silicon Area equivalents | |
| 16-bit | 0.67 | LUTs/DSP48 | 16:1 |
| 32-bit | 1.00 | LUTs/Block RAM | 32:1 |

Under the assumption that the core is capable of one instruction per clock

Following has DMIPS per clock for many microprocessors

http://en.wikipedia.org/wiki/Instructions_per_second

| uP | MIPS | /MHz | MHz | guessed average clocks/inst |
|--------------------|------------|------|------|-----------------------------|
| 4004 | 0.10 | | | |
| 6502 | 0.50 | 0.02 | 0.06 | 4 |
| 8051 | 0.01 DMIPS | 0.08 | 0.24 | 1, 4 or 6 |
| 8080 | 0.17 | | 0.25 | 9 |
| 68K | 0.10 | | 0.15 | 4 |
| ARM Cortex A9 | 2.50 DMIPS | 2.90 | 1000 | |
| ARM Cortex M0 | 0.90 DMIPS | 1.50 | 70 | |
| ARM Cortex M3 | 1.25 DMIPS | 2.17 | 25 | |
| ARM7 | 0.90 | 0.74 | 2.04 | 600 |
| AVR | 1.00 | 0.21 | 0.53 | 8 |
| AVR32 | | | 1.62 | 60 |
| BA21 | | | 2.44 | 400 |
| Coldfire | | | 2.80 | 400 |
| Coldfire | | | 0.77 | 150 |
| HCS08 | | 0.04 | 0.12 | 4 |
| HC11 | | | | 4 |
| LEON3/Spartan-6 | | | 1.96 | 100 |
| MC6809 | 1.24 | 0.07 | 1.86 | 3 |
| MicroBlaze 3-stage | 1.03 | | 1.50 | |
| MicroBlaze 5-stage | 1.38 | | 1.90 | 125 |
| MIPS32 | 1.51 | | 2.28 | |
| MSP430 | | 0.40 | 1.20 | 2 |
| MSP430 | | | 1.10 | 25 |
| Nios II | 0.64 DMIPS | | 0.93 | 200 |
| Nios II -e | 0.15 DMIPS | | 0.25 | |
| Nios II -f | 1.13 DMIPS | | 1.60 | 200 |
| PIC16 | 0.25 | | | |
| PIC18 | | | 0.04 | 40 |
| PIC24 | | 0.72 | 1.86 | 40 |
| PIC32 | | | 3.45 | 80 |
| Super H-2 | | | 1.44 | 180 |
| VAX780 | 1.00 DMIPS | | 1.50 | DMIPS # is by definition |
| Z80 | 1.60 | 0.01 | 0.03 | 3 |
| eSi-1600 | | | 1.98 | |

| Column Titles | Details |
|----------------------|--|
| "A" | A: 1st choice clone, B: 2nd choice clone, W: 1st choice original, X: 2nd choice original |
| "B" | used to indicate best KIPS/LUT for a given design, usually using fast FPGA family |
| up_cores_test folder | if opencores design is their folder name, otherwise my folder name |
| opencores name | |
| status | ASIC, planning, alpha, beta, stable, mature, proprietary |
| author | First Name, Last Name |
| style / clone | part number or "forth", RISC, accumulator, etc |
| data size | data memory word size |
| inst size | instruction size |
| FPGA | FPGA family for compile, place, route & timing, usually using fastest part grade |
| reporter | First Name, Last Name |
| comments | compile, place, route & timing problems |
| LUTs ALM | 4-LUT, 6-LUT, Altera ALM, Actel Tile |
| LUT? | total number of LUTs or ALMs used including route-thrus & otherwise unavailable |
| mults | total number of multipliers/DSPs used; 9x9 multiplier counts divided by two and rounded up |
| blk RAM | total # of block RAMs used, Xilinx half block RAM counts divided by two and rounded up, Altera count is percent used times # avail |
| Fmax | maximum primary clock speed from compile, place, route & timing run |
| date | date of compile, place & route; serves to identify source version |
| tool ver | Altera, Xilinx, Lattice Semiconductor or MicroSemi tool version number |
| MIPS /clk | prorated DMIPS per clock, reduced for data word sizes under 32-bits, greater than one for multiple issue processors |
| clks/ inst | number of clocks per instruction, typically 1.0 for modern pipelined processors, subjective for older uP |
| KIPS /LUT | figure of merit, does not include effects of memory capacity, floating point or instruction set quality |
| src code | VHDL or Verilog or System Verilog or schematic or gates |
| # src files | number of source files for compile, place, route & timing |
| top file | top file for compile, place, route & timing run |
| doc | is documentation provided |
| tool chain | is there a compiler or assembler provided or available |
| ftg pt | does the compile, place, route & timing run include floating point |
| Ha vd | separate instruction and data memory(s), there can be more than one data memory, M for MMU & caches |
| max data | maximum data address |
| max inst | maximum instruction address |
| byte adrs | is byte addressing provided |
| # inst | number of unique instructions, somewhat subjective |
| # reg | number of registers in register file |
| pipe len | number of pipeline stages |
| start year | year of first design activity |
| last revis | last year for revisions |
| reference | web address or generic information (for clones) |
| note worthy | anything special about the design |
| comments | catchall |