_uP_cores_test folder	opencores name	status	author	style / clone	data size	inst size	FPGA	reporter	comments	LUTs ALUT	LUT?	mults	blk ram	F max	date	tool ver	MIPS /clk	clks/ inst	KIPS /LUT	src code	# src fi	top file	doc	tool chain	fltg pt	Ha vd	max data	ma x	byte adrs	# inst	# reg	pipe len	start year	last revis	reference	note worthy	comments
ag_6502	ag_6502 soft cor	beta	Oleg Odintsov	6502	8	8x	spartan-3e-	Oleg Odintsov		978	4			50			0.33	4.0	4.2	verilog	2	ag_6502		yes	N	N	64K	64K	Y				2012	2012	6502 data sheets	verilog code generation, "phase level accurate"	
ag_6502	ag_6502 soft cor	beta	Oleg Odintsov	6502	8	8x	kintex-7-3	James Brakefiel		807	6			80	##	14.7	0.33	4.0	8.2	verilog	2	ag_6502		yes	N	N	64K	64K	Y				2012	2012	6502 data sheets	verilog code generation, "phase level accurate"	
ag_6502	ag_6502 soft cor	beta	Oleg Odintsov	6502	8	8x	kintex-7-3	James Brakefiel		824	6			176	##	14.7	0.33	4.0	17.7	verilog	2	ag_6502		yes	N	N	64K	64K	Y				2012	2012	6502 data sheets	verilog code generation, "phase level accurate"	
cpu6502_tru	cpu6502_tc	stable	Jens Gutschmidt	6502	8	8x	kintex-7-3	James Brakefiel		1678	6			159	##	14.7	0.33	4.0	7.8	vhdl	7	r6502_tc		yes	N	N	64K	64K	Y				2008	2010	6502 data sheets		
cpu65c02_tri	cpu65c02_tc	stable	Jens Gutschmidt	6502	8	8x	spartan-6-3	James Bra	latch	4794	6			47	##	14.7	0.33	4.0	0.8	vhdl	8	core		yes	N	N	64K	64K	Y				2008	2013	6502 data sheets		
free6502		stable	David Kessner	6502	8	8x	spartan-6-3	James Brakefiel		663	6			89	##	14.7	0.33	4.0	11.1	vhdl	5	free6502	yes	yes	N	N	64K	64K	Y				1999	2000	6502 data sheets	microcoded	
free6502		stable	David Kessner	6502	8	8x	kintex-7-3	James Brakefiel		646	6			193	##	14.7	0.33	4.0	24.6	vhdl	5	free6502	yes	yes	N	N	64K	64K	Y				1999	2000	6502 data sheets	microcoded	
lattice6502	Lattice 6502	beta	Ian Chapman	6502	8	8x	kintex-7-3	James Brakefiel		4942	6			214	##	14.7	0.33	4.0	3.6	vhdl	3	ghdl_proce	yes	yes	N	N	64K	64K	Y				2010	2010	6502 data sheets	targeted to LCMXO2280	huge LUT count
m65c02	M65C02	mature	Michael Morris	6502	8	8x	spartan-3	Michael Morris		661	4		3	74			0.33	4.0	9.2	verilog	13	M65C02	yes	yes	N	N	64K	64K	Y				2013	2014	6502 data sheets		
m65c02	M65C02	mature	Michael Morris	6502	8	8x	spartan-3-5	James Brakefield			4		3		##	14.7	0.33	4.0		verilog	13	M65C02	yes	yes	N	N	64K	64K	Y				2013	2014	6502 data sheets		
m65c02	M65C02	mature	Michael Morris	6502	8	8x	spartan-6-3	James Brakefiel		466	6		3	118	##	14.7	0.33	4.0	20.8	verilog	13	M65C02	yes	yes	N	N	64K	64K	Y				2013	2014	6502 data sheets		
m65c02	M65C02	mature	Michael Morris	6502	8	8x	kintex-7-3	James Brakefiel		661	6		3		##	14.7	0.33	4.0		verilog	13	M65C02	yes	yes	N	N	64K	64K	Y				2013	2014	6502 data sheets		
t65	T65 CPU	stable	Daniel Wallner	6502	8	8x	cyclone-2	James Brakefiel		829	4			84	##	q11.1s	0.33	4.0	8.4	vhdl	7	T65	yes	yes	N	N	64K	64K	Y				2002	2010	6502 data sheets	6502, 65C02 & 65C816; wide use	
t65	T65 CPU	stable	Daniel Wallner	6502	8	8x	cyclone-4	James Brakefiel		831	4			110	##	q13.1	0.33	4.0	10.9	vhdl	7	T65	yes	yes	N	N	64K	64K	Y				2002	2010	6502 data sheets	6502, 65C02 & 65C816; wide use	
t65	T65 CPU	stable	Daniel Wallner	6502	8	8x	arria-2	James Brakefiel		617	A			190	##	q13.1	0.33	4.0	25.4	vhdl	7	T65	yes	yes	N	N	64K	64K	Y				2002	2010	6502 data sheets	6502, 65C02 & 65C816; wide use	
t65	T65 CPU	stable	Daniel Wallner	6502	8	8x	spartan-3-5	James Brakefiel		923	4			83	##	14.7	0.33	4.0	7.5	vhdl	7	T65	yes	yes	N	N	64K	64K	Y				2002	2010	6502 data sheets	6502, 65C02 & 65C816; wide use	
t65	T65 CPU	stable	Daniel Wallner	6502	8	8x	spartan-6-3	James Brakefiel		725	6			128	##	14.7	0.33	4.0	14.5	vhdl	7	T65	yes	yes	N	N	64K	64K	Y				2002	2010	6502 data sheets	6502, 65C02 & 65C816; wide use	
t65	T65 CPU	stable	Daniel Wallner	6502	8	8x	kintex-7-3	James Brakefiel		575	6			291	##	14.7	0.33	4.0	41.7	vhdl	7	T65	yes	yes	N	N	64K	64K	Y				2002	2010	6502 data sheets	6502, 65C02 & 65C816; wide use	
t6507lp	T6507LP	beta	Gabriel Oshiro, Samuel	6502	8	8x	spartan-6-3	James Bra	errors							14.7		4.0		verilog	22	t6507lp	yes	yes	N	N	64K	64K	Y				2009	2010	6502 data sheets	for use in ATARI 2600	
m65		stable	Naohiko Shimizu	6502	8	8x	arria-2	James Brakefiel		483	A			110	##	q13.1	0.33	4.0	18.8	sfl & TDF	8	m65cpu	yes	yes	N	N	4K	4K	Y				2001	2002	6502 data sheets		
hd63701	HD63701 compa	planning	Tsuyoshi Hasegawa	6801	8	8x	spartan-3-5	James Brakefiel		1937	4	1	3	20	##	14.7	0.33	4.0	0.9	verilog	6	HD63701_CORE			N	N	64K	64K	Y				2014			Used in Atari game console, 6801 clone?	
hd63701	HD63701 compa	planning	Tsuyoshi Hasegawa	6801	8	8x	spartan-6-3	James Brakefiel		1412	6	1	3	31	##	14.7	0.33	4.0	1.8	verilog	6	HD63701_CORE			N	N	64K	64K	Y				2014			Used in Atari game console, 6801 clone?	
system68	System68	stable	John Kent, David Burne	6801	8	8x	spartan-3-5	James Brakefiel		2235	4		4	46	##	14.7	0.33	4.0	1.7	vhdl	21	cpu68	yes	yes	N	N	64K	64K	Y				2003	2009	6801 data sheets		
system6801	Wishbone Syste	stable	Michael L. Hasenfratz	6801	8	8x	cyclone-3	James Brakefiel		1507	4		3	73	##	14.7	0.33	4.0	4.0	vhdl	15	wb_cyclon	yes	yes	N	N	64K	64K	Y				2003	2009	6801 data sheets	based on John Kent's 6801	tested on Apex20K, Cyclone & Stra
df6805		proprietar	Hitech Global	6805	8	8x	stratix-1	Hitech Global		1690	4			83			0.33	4.0	4.1	not avail			yes	yes	N	N	64K	64K	Y						6805 data sheets		www.hitechglobal.com/IPCores/D
system05	SOC:system05	beta	John Kent	6805	8	8x	kintex-7-3	James Brakefiel		834	6			204	##	14.7	0.33	4.0	20.2	vhdl	10	System05	yes	yes	N	N	64K	64K	Y				2003	2009	6805 data sheets		
68hc05	68hc05	stable	Ulrich Riedel	6805	8	8x	kintex-7-3	James Brakefiel		1225	6			300	##	14.7	0.33	4.0	20.2	vhdl	1	6805		yes	N	N	64K	64K	Y				2007	2009	6805 data sheets		
68hc08	68hc08	stable	Ulrich Riedel	6808	8	8x	kintex-7-3	James Brakefiel		2290	6			101	##	14.7	0.33	4.0	3.6	vhdl	1	x68ur08		yes	N	N	64K	64K	Y				2007	2009	6808 data sheets		
6809_6309	6809_6309_com	beta	Alejandro Paz Schmidt	6809	8	8x	spartan-6-3	James Brakefiel		2061	6			109	##	14.7	0.33	3.0	5.8	verilog	5	MC6809_cpu	yes	yes	N	N	64K	64K	Y				2012	2013	6809 data sheets	includes 6309 op-codes, xilinx & lattice projects	
6809_6309	6809_6309_com	beta	Alejandro Paz Schmidt	6809	8	8x	kintex-7-3	James Brakefiel		2207	6			212	##	14.7	0.33	3.0	10.6	verilog	5	MC6809_cpu	yes	yes	N	N	64K	64K	Y				2012	2013	6809 data sheets	includes 6309 op-codes, xilinx & lattice projects	
system09	SOC:system09	stable	John Kent	6809	8	8x	spartan-6-3	James Brakefiel		2127	6			64	##	14.7	0.33	3.0	3.3	vhdl	40	cpu09l	yes	yes	N	N	64K	64K	Y				2003	2012	6809 data sheets	from John Kent web page	
system09	SOC:system09	stable	John Kent	6809	8	8x	kintex-7-3	James Brakefiel		1945	6			154	##	14.7	0.33	3.0	8.7	vhdl	40	cpu09l	yes	yes	N	N	64K	64K	Y				2003	2012	6809 data sheets	from John Kent web page	
mc6809e		beta	Flint Weller	6809	8	8x	kintex-7-3	James Bra	gate level pri		6					14.7	0.33	3.0		vhdl	26	core_6809	yes	yes	N	N	64K	64K	Y				1999		6809 data sheets	course work, ASIC orientation	
altium/TSK51A		proprietar	Altium	8051	8	8x	cyclone-2	Altium		2135	4		1	50			0.33	6.0	1.3	not avail			yes	yes	N	N	64K	64K	Y				2004		CR0140.PDF	asm, C, C++, schem, VHDL & Verilog	default clock speed is 50MHz
altium/TSK51A		proprietar	Altium	8051	8	8x	spartan-3-5	Altium		1890	4		1	50			0.33	6.0	1.5	not avail			yes	yes	N	N	64K	64K	Y				2004		CR0140.PDF	asm, C, C++, schem, VHDL & Verilog	default clock speed is 50MHz
dalton_8051		stable	Tony Givargis	8051	8	8x	kintex-7-3	James Brakefiel		2725	6	1	1	105	##	14.7	0.33	1.0	12.7	vhdl	7	i8051_all	yes	yes	N	N	64K	64K	Y				1999	2003	8051 data sheets	ASIC	www.cs.ucr.edu/~dalton/
light52	Lightweight 805	beta	Jose Ruiz	8051	8	8x	cyclone-2-7	Jose Ruiz		1339	4	1	29	62			0.33	6.0	2.5	vhdl	8	light52_cp	yes	yes	N	N	64K	64K	Y				2012	2013	8051 data sheets	targeted to area	0.0187 DMIPS/MHz, i8051 is 0.009
light52	Lightweight 805	beta	Jose Ruiz	8051	8	8x	spartan-3-4	Jose Ruiz		1424	4	1	10	35			0.33	6.0	1.4	vhdl	8	light52_cp	yes	yes	N	N	64K	64K	Y				2012	2013	8051 data sheets	targeted to area	~ 6 clocks/inst
light52	Lightweight 805	beta	Jose Ruiz	8051	8	8x	kintex-7-3	James Brakefiel		1027	6	1	1	148	##	14.7	0.33	6.0	7.9	vhdl	8	light52_cp	yes	yes	N	N	64K	64K	Y				2012	2013	8051 data sheets	targeted to balanced	~ 6 clocks/inst
mc8051		stable	Helmut Mayrhofer	8051	8	8x	kintex-7-3	James Brakefiel		3022	6	1		83	##	14.7	0.33	4.0	2.3	vhdl	49	mc8051co	yes	yes	N	N	256	64K	Y				1999	2013	www.oreganosystems.	fast 8051, version available with floating-point by David Lundgren	
t51	T51 mcu	stable	Andreas Voggeneder	8051	8	8x	kintex-7-3	James Brakefiel		1942	6	1		147	##	14.7	0.33	4.0	6.2	vhdl	17	T8032	yes	yes	N	N	64K	64K	Y				2002	2010	8032 data sheets	8052 & 8032	8032 SoC
t51	T51 mcu	stable	Andreas Voggeneder	8051	8	8x	kintex-7-3	James Brakefiel		1921	6	1	2	127	##	14.7	0.33	4.0	5.5	vhdl	17	T8052	yes	yes	N	N	64K	64K	Y				2002	2010	8052 data sheets	8052 & 8032	8052 SoC
t51	T51 mcu	stable	Andreas Voggeneder	8051	8	8x	arria-2	James Bra	proba	3049	6	1		111	##	q13.1	0.33	4.0	3.0	vhdl	17	T8032	yes	yes	N	N	64K	64K	Y				2002	2010	8032 data sheets	8052 & 8032	8032 SoC
t51	T51 mcu	stable	Andreas Voggeneder	8051	8	8x	arria-2	James Bra	proba	4704	6	1	1	89	##	q13.1	0.33	4.0	1.6	vhdl	17	T8052	yes	yes	N	N	64K	64K	Y				2002	2010	8052 data sheets	8052 & 8032	8052 SoC
turbo8051	turbo 8051	beta	Dinesh Annayya	8051	8	8x	cyclone-2	Dinesh Annayya		5072	4			39			0.33	4.0	0.6	verilog	74	oc8051_to	yes	yes	N	N	64K	64K	Y				2011	2013	8051 data sheets	includes perpherials	
turbo8051	turbo 8051	beta	Dinesh Annayya	8051	8	8x	kintex-7-3	James Brakefiel		1985	6	1		127	##	14.7	0.33	4.0	5.3	verilog	74	oc8051_to	yes	yes	N	N	64K	64K	Y				2011	2013	8051 data sheets	includes perpherials	
cpu8080	8080 Compativle	stable	Scott Moore	8080	8	8x	spartan-6-3	James Brakefiel		1269	6			129	##	14.7	0.33	9.0	3.7	verilog	1	m8080	yes	yes	N	N	64K	64K	Y				2006	2009	8080 data sheets	includes VGA display generator, three variants	
light8080	Lightweight 808	stable	Jose Ruiz, Moti Litoche	8080	8	8x	spartan-2-5	Jose Ruiz		203	4		4	60		q9.1	0.33	9.0	10.8	vhdl	5	light8080	yes	yes	N	N	64K	64K	Y				2007	2012	8080 data sheets	targeted to speed, bare core	typically 9 clocks per inst, .04=.33/
light8080	Lightweight 808	stable	Jose Ruiz, Moti Litoche	8080	8	8x	cyclone-2-7	Jose Ruiz		413	4		4	80		q9.0	0.33	9.0	7.1	vhdl	5	light8080	yes	yes	N	N	64K	64K	Y				2007	2012	8080 data sheets	targeted to balanced, bare core	typically 9 clocks per inst, .04=.33/
light8080	Lightweight 808	stable	Jose Ruiz, Moti Litoche	8080	8	8x	spartan-3-5	Jose Ruiz		209	4		1	100		q9.1	0.33	9.0	17.5	vhdl	5	light8080	yes	yes	N	N	64K	64K	Y				2007	2012	8080 data sheets	targeted to speed, bare core	typically 9 clocks per inst, .04=.33/
light8080	Lightweight 808	stable	Jose Ruiz, Moti Litoche	8080	8	8x	kintex-7-3	James Brakefiel		154	6		1	247		14.7	0.33	9.0	58.9	verilog	5	i80soc	yes	yes	N	N	64K	64K	Y				2007	2012	8080 data sheets	targeted to area, includes UART, inte	typically 9 clocks per inst, .04=.33/
light8080	Lightweight 808	stable	Jose Ruiz, Moti Litoche	8080	8	8x	spartan-6	James Brakefiel		148	6		3	172	##	14.7	0.33	9.0	42.7	verilog	5	light8080	yes	yes	N	N	64K	64K	Y				2007	2012	8080 data sheets	targeted to area, bare core	typically 9 clocks per inst, .04=.33/
light8080	Lightweight 808	stable	Jose Ruiz, Moti Litoche	8080	8	8x	kintex-7-3	James Brakefiel		154	6		1	247	##	14.7	0.33	9.0	58.9	verilog	5	light8080	yes	yes	N	N	64K	64K	Y				2007	2012	8080 data sheets	targeted to area, bare core	typically 9 clocks per inst, .04=.33/
light8080	Lightweight 808	stable	Jose Ruiz, Moti Litoche	8080	8	8x	spartan-6	James Brakefiel		150	6		3	142	##	14.7	0.33	9.0	34.6	vhdl	5	light8080	yes	yes	N	N	64K	64K	Y				2007	2012	8080 data sheets	targeted to area, bare core	typically 9 clocks per inst, .04=.33/
t80	T80 cpu	stable	Daniel Wallner	8080	8	8x	spartan-6-3	James Bra	8080	958	6			95	##	14.7	0.33	9.0	3.6	vhdl	5	T8080se	yes	yes	N	N	64K	64K	Y				2002	2011	8080 data sheets	Z80, 8080 & gameboy int sets, several usages	
gl85		stable	Alex Miczo	8085	8	8x	kintex-7-3	James Bra	gate level des		6					14.7	0.33	4.0		vhdl	1	i8085	yes	yes	N	N	64K	64K	Y				1993		8085 data sheets	also a TTL implementation in VHDL	
cpu86		beta	ht-lab.com	8086	8	8x	kintex-7-3	James Brakefiel		3421	6	1		127	##	14.7	0.17	2.0	3.1	vhdl	23	cpu86_top	yes	yes	N	N	1M	1M	Y				2002	2010	x86 data sheets	8088 clone	www.ht-lab.com
next186	Next 80186 proc	stable	Nicolae Dumitrache	8086	16	8x	cyclone-2	James Brakefiel		2865	4	1		39	##	q11.1s	0.67	2.0	4.6	verilog	4	Next186_C	yes	yes	N	N	1M	1M	Y				2012	2013	x86 data sheets	boots DOS	did not infer multiplier
next186	Next 80186 proc	stable	Nicolae Dumitrache	8086	16	8x	cyclone-4	James Brakefiel		3252	4			48	##	q13.1	0.67	2.0	4.9	verilog	4	Next186_C	yes	yes	N	N	1M	1M	Y				2012	2013	x86 data sheets	boots DOS	did not infer multiplier
next186	Next 80186 proc	stable	Nicolae Dumitrache	8086	16	8x	cyclone-5	James Brakefiel		2710	A	1		44	##	q13.1	0.67	2.0	5.4	verilog	4	Next186_C	yes	yes	N	N	1M	1M	Y				2012	2013	x86 data sheets	boots DOS	
next186	Next 80186 proc	stable	Nicolae Dumitrache	8086	16	8x	arria-2	James Brakefiel		1966	A	2		77	##	q13.1	0.67	2.0	13.1	verilog	4	Next186_C	yes	yes	N	N	1M	1M	Y				2012	2013	x86 data sheets	boots DOS	
next186	Next 80186 proc	stable	Nicolae Dumitrache	8086	16	8x	spartan-3-5	James Brakefiel		2763	4	1		34	##	14.7	0.67	2.0	4.2	verilog	4	Next186_C	yes	yes	N	N	1M	1M	Y				2012	2013	x86 data sheets	boots DOS	
next186	Next 80186 proc	stable	Nicolae Dumitrache	8086	16	8x	spartan-6-3	James Brakefiel		2716	6	1		44	##	14.7	0.67	2.0	5.4	verilog	4	Next186_C	yes	yes	N	N	1M	1M	Y				2012	2013	x86 data sheets	boots DOS	
next186	Next 80186 proc	stable	Nicolae Dumitrache	8086	16	8x	kintex-7-3	James Brakefiel		2500	6	1		94	##	14.7	0.67	2.0	12.6	verilog	4	Next186_C	yes	yes	N	N	1M	1M	Y				2012	2013	x86 data sheets	boots DOS	
zet86	Zet The x86 (IA-	alpha	Zeus Marmolejo	8086	16	8x	kintex-7-3	James Brakefiel		3642	6	1		68	##	14.7	0.67	2.0	6.2	verilog	32	fpga_zet_t	yes	yes	N	N	1M	1M	Y				2008	2014	x86 data sheets	equivalent to 80186, boots MS-DOS	zet.aluzina.org/index.php/Zet_pro
rtf8088	rtf8088	planning	Robert Finch	8086	8x	8x	kintex-7-3	James Brakefiel		4514	6	4		174	##	14.7	0.67	3.0	8.6	verilog	57	rtf8088	yes	yes	N	N	1M	1M	Y				2012	2013	x86 data sheets	8-bit memory data, e.g. 8088	
ao68000	ao68000	beta	Aleksander Osman	68000	16	16x	arria-2	James Brakefiel		3479	A		6	169	##	q13.1	0.67	3.0	10.8	verilog	1	ao68000	som	yes	N		4G	4G	Y				2010	2011	68000 data sheets	uses microcode, instruction prefetch buffer	
k68	K68	alpha	Shawn Tan	68000	8	16x	kintex-7-3	James Brakefiel		2392	6			24	##	14.7	0.67	4.0	1.7	verilog	15	k68_cpu	yes	yes	N	N	4K	4G	Y		16		2003	2009	68000 data sheets	68K binary compatible	
suska-III		beta	Wolfgang Forster	68000	16	16x	arria-2	James Brakefiel		7388	A			55	##	q13.1	0.67	4.0	1.3	vhdl	11	wf68k00ip	yes	yes	N	N	4G	4G	Y		16		2003	2013	68000 data sheets	for use as an Atari ST	http://www.experiment-s.de/en/
tg68	TG68 execute 68	stable	Tobias Gubener	68000	16	16x	kintex-7-3	James Brakefiel		2331	6			44	##	14.7	0.67	4.0	3.2	vhdl	2	TG68_fast	yes	yes	N	N	4G	4G	Y		16		2007	2012	68000 data sheets	for use with Minimig	
v1_coldfire		stable	IPextreme	68000	16	16x	cyclone-3	freescale		5000	4			80			0.89	1.0	14.2				yes	yes	N	N	4G	4G	Y		16		2008		68000 data sheets	free for Cyclone III	http://www.ip-extreme.com/IP/co
aoocs	aoOCS - Wishbo	beta	Aleksander Osman	68000	16	16x	cyclone-3	James Bra	pin constrain		4					q13.1	0.67	4.0		verilog	22	aoOCS	som	yes	N		4G	4G	Y				2010	2011	68000 data sheets	uses ao68000 core, Amiga chip set emulation (blitter, copper), Minimig	
rtf68ksys	rtf68kSys	alpha	Robert Finch	68000	16	16x	spartan-3e-	James Bra	need	13639	4	12	17		##	14.7	0.67	4.0		verilog	49	rtf68kSys	yes	yes	N	N	4G	4G	Y		16		2011	2011	68000 data sheets	based on Tobias Gubener's TG68	
agcnorm	Apollo Guidance	beta	Dave Roberts	?	16	16												1.0		vhdl	5	AGC	some		N		32M	32M					2010	2012		Apollo Guidance Computer via NOR gate emulation	
gup	HC11 Compatibl	stable	Kevin Phillipson	68HC11	8	8x	arria-2	James Brakefiel		925	A	1	1	127	##	q13.1	0.33	4.0	11.3	vhdl	25	gator_upro	yes	yes	N	N	64K	64K	Y				2008	2009	6811 data sheets	68HC11 compatible	top level is schematic
hc11core		stable	Green Mountain Comp	68HC11	8	8x	arria-2	James Brakefiel		1962	A			116	##	q13.1	0.33	4.0	4.9	vhdl	1	hc11rtl	yes	yes	?	N	64K	64K	N	53	8	2	2000		6811 data sheets	restricted use license, with correctio	http://www.gmvhdl.com/hc11cor
hc11core		stable	Green Mountain Comp	68HC11	8	8x	kintex-7-3	James Brakefiel		2190	6			127	##	14.7	0.33	4.0	4.8	vhdl	1	hc11rtl	yes	yes	?	N	64K	64K	N	53	8	2	2000		6811 data sheets	restricted use license, with correctio	http://www.gmvhdl.com/hc11cor
system11		alpha	John Kent, David Burne	68HC11	8	8x	kintex-7-3	James Brakefiel		1218	6			153	##	14.7	0.33	4.0	10.3	vhdl	17	cpu11	yes	yes	N	N	64K	64K	Y				2003	2009	6811 data sheets	known bugs & untested instructions	
ARM_Cortex_A9		ASIC	ARM	ARM a9	32	16	arria V	altera		4500	A			1050			2.50	1.0	583.3	asic			yes	yes	Y		4G	4G	Y	80	16	10		2012	altera data sheets	uses pro-rated LC area	dual issue, includes fltg-pt & MMU
ARM_Cortex_A9		ASIC	ARM	ARM a9	32	16	cyclone V	altera		4500	A			925			2.50	1.0	513.9	asic			yes	yes	Y		4G	4G	Y	80	16	10		2012	altera data sheets	uses pro-rated LC area	dual issue, includes fltg-pt & MMU
ARM_Cortex_A9		ASIC	ARM	ARM a9	32	16	zynq	xilinx		4500	6			1000			2.50	1.0	555.6	asic			yes	yes	Y		4G	4G	Y	80	16	10		2012	xilinx plan ahead: an A9	uses pro-rated LC area	dual issue, includes fltg-pt & MMU
amber	*Amber ARM-con*	stable	Conor Santifort	ARM7	32	32	spartan-6-3	James Brakefiel		6901	6		4	40	##	14.7	0.75	1.0	4.3	verilog	25	a23_core	yes	yes	N		4G	4G	Y			3	2010	2013	ARM7 data sheets	no MMU, shared cache	2048 LUTs used as single port RAM
amber	*Amber ARM-con*	stable	Conor Santifort	ARM7	32	32	kintex-7-3	James Brakefiel		6409	6		2	82	##	14.7	0.75	1.0	9.6	verilog	25	a23_core	yes	yes	N		4G	4G	Y			3	2010	2013	ARM7 data sheets	no MMU, shared cache	2048 LUTs used as single port RAM
amber	*Amber ARM-con*	stable	Conor Santifort	ARM7	32	32	spartan-6-3	James Brakefiel		12834	6		8	40	##	14.7	1.05	1.0	3.3	verilog	25	a25_core	yes	yes	N	Y	4G	4G	Y			5	2010	2013	ARM7 data sheets	no MMU, data & inst caches	4096 LUTs used as single port RAM
amber	*Amber ARM-con*	stable	Conor Santifort	ARM7	32	32	kintex-7-3	James Brakefiel		12450	6		4	98	##	14.7	1.05	1.0	8.2	verilog	25	a25_core	yes	yes	N	Y	4G	4G	Y			5	2010	2013	ARM7 data sheets	no MMU, data & inst caches	4096 LUTs used as single port RAM
amber	*Amber ARM-con*	stable	Conor Santifort	ARM7	32	32	kintex-7-3	James Brakefiel		7926	6		320	92	##	v14.1	1.05	1.0	12.2	verilog	25	a25_core	yes	yes	N	Y	4G	4G	Y			5	2010	2013	ARM7 data sheets	no MMU, data & inst caches	2454 LUTs used as single port RAM
arm4u	ARM4U	stable	Joanathan Masur, Xavi	ARM7	32	32	cyclone-2	James Brakefiel		2084	4	3	12	43	##	q11.1s	0.75	1.0	15.4	vhdl	12	cpu	yes	ues	N		4G	4G	Y	80	16	5	2013	2014	ARM7 data sheets	university project	altera memory
arm4u	ARM4U	stable	Joanathan Masur, Xavi	ARM7	32	32	cyclone-4-6	James Brakefiel		2809	4		8	43	##	q13.1	0.75	1.0	11.5	vhdl	12	cpu	yes	ues	N		4G	4G	Y	80	16	5	2013	2014	ARM7 data sheets	university project	altera memory

arm4u	ARM4U	stable	Joanathan Masur, Xavi	ARM7	32	32	aria-2	James Brakefiel	1668	A	4	8	66	##	q13.1	0.75	1.0	29.5	vhdl	12	cpu	yes	ues	N		4G	4G	Y	80	16	5	2013	2014	ARM7 data sheets	university project	altera memory
storm_core	Storm Core (ARM	beta	Stephan Nolting	ARM7	32	32	cyclone-2-6	Stephan Nolting	11469	4	3	75	179			1.00	1.0	15.6	vhdl	16	STORM_TC	yes	yes	N	M	4G	4G	Y		32	8	2011	2014		I & D caches	
storm_core	Storm Core (ARM	beta	Stephan Nolting	ARM7	32	32	cyclone-4-6	Stephan Nolting	11518	4	3	67	157			1.00	1.0	13.7	vhdl	16	STORM_TC	yes	yes	N	M	4G	4G	Y		32	8	2011	2014		I & D caches	
storm_core	Storm Core (ARM	beta	Stephan Nolting	ARM7	32	32	kintex-7-3	James Brakefiel	2312	6	3		179	##	14.7	1.00	1.0	77.4	vhdl	16	CORE	yes	yes	N		4G	4G	Y		32	8	2011	2014		I & D caches not compiled	
storm_core	Storm Core (ARM	beta	Stephan Nolting	ARM7	32	32	kintex-7-3	James Brakefiel	3514	6	3	4	157	##	14.7	1.00	1.0	44.8	vhdl	16	STORM_TC	yes	yes	N	M	4G	4G	Y		32	8	2011	2014		I & D caches	
oks8	oks8	alpha	Kongzilee	ARM7	32	32	kintex-7-3	James Brakefiel	bad coding pr	6				##	14.7	0.67	1.0		verilog	8	oks8	yes	yes	N		64K	64K	Y				2006	2009		clone of KS86C4204/C4208/P4208, SAM87RI instruction set	
avr_core	avr_core	stable	Rusian Lepetenok	AVR	8	16	kintex-7-3	James Brakefiel	2135	6			127	##	14.7	0.33	1.0	19.7	verilog	15	avr_core	yes	yes	N		64K	128K	Y		32		2002	2012	AVR data sheets	VHDL core included	
avr_hp	avr_hp	stable	Strauch Tobias	AVR	8	16	kintex-7-3	James Brakefiel	1 slot	6			127	##	14.7	0.33	1.0	35.0	vhdl	9	avr_core	som	yes	N		64K	128K	Y		32		2010	2010	AVR data sheets	hyper pipelined (eg barrel) AVR	
avr_hp	avr_hp	stable	Strauch Tobias	AVR	8	16	kintex-7-3	James Brakefiel	2 slot	6			223	##	14.7	0.33	1.0	47.4	vhdl	10	avr_core_c	som	yes	N		64K	128K	Y		32		2010	2010	AVR data sheets	hyper pipelined (eg barrel) AVR	
avr_hp	avr_hp	stable	Strauch Tobias	AVR	8	16	kintex-7-3	James Brakefiel	3 slot	6			243	##	14.7	0.33	1.0	44.2	vhdl	10	avr_core_c	som	yes	N		64K	128K	Y		32		2010	2010	AVR data sheets	hyper pipelined (eg barrel) AVR	
avr_hp	avr_hp	stable	Strauch Tobias	AVR	8	16	kintex-7-3	James Brakefiel	4 slot	6			278	##	14.7	0.33	1.0	44.7	vhdl	10	avr_core_c	som	yes	N		64K	128K	Y		32		2010	2010	AVR data sheets	hyper pipelined (eg barrel) AVR	
avr8	Reduced AVR Co	beta	Nick Kovach	AVR	8	16	kintex-7-3	James Brakefiel	174	6			418	##	14.7	0.33	1.0	792.2	verilog	1	rAVR	yes	yes	N		64K	64K	Y	17	4		2010	2010	AVR data sheets	not a full clone, doc is opencores page	
avrtinyx61co	avrtinyx61core	beta	Andreas Hilvarsson	AVR	8	16	kintex-7-3	James Brakefiel	1243	6			194	##	14.7	0.33	1.0	51.5	vhdl	1	mcu_core		yes	N		64K	128K	Y		32		2008	2009	AVR data sheets		
ax8	AX8 MCU	stable	Daniel Wallner	AVR	8	16	spartan-6-3	James Brakefiel	missing ROM	6					14.7	0.33	1.0		vhdl	14	A90S1200			N		64K	128K	Y		32		2002	2009	AVR data sheets	both A90S1200 & A90S2313	80K LUTs as ROM
navre	Navre AVR clone	stable	Sebastien Bourdeaudu	AVR	8	16	cyclone-2	James Brakefiel	1567	4			74	##	q11.1s	0.33	1.0	15.6	verilog	1	softusb_na	yes	yes	N		64K	64K	Y		32	2	2010	2013	AVR data sheets	AVR clone, part of www.milkymist.org	
navre	Navre AVR clone	stable	Sebastien Bourdeaudu	AVR	8	16	cyclone-4-6	James Brakefiel	1561	4			102	##	q13.1	0.33	1.0	21.5	verilog	1	softusb_na	yes	yes	N		64K	64K	Y		32	2	2010	2013	AVR data sheets	AVR clone, part of www.milkymist.org	
navre	Navre AVR clone	stable	Sebastien Bourdeaudu	AVR	8	16	cyclone-5	James Brakefiel	1566	A			103	##	q13.1	0.33	1.0	21.8	verilog	1	softusb_na	yes	yes	N		64K	64K	Y		32	2	2010	2013	AVR data sheets	AVR clone, part of www.milkymist.org	
navre	Navre AVR clone	stable	Sebastien Bourdeaudu	AVR	8	16	arria-2	James Brakefiel	1126	A			154	##	q13.1	0.33	1.0	45.1	verilog	1	softusb_na	yes	yes	N		64K	64K	Y		32	2	2010	2013	AVR data sheets	AVR clone, part of www.milkymist.org	
navre	Navre AVR clone	stable	Sebastien Bourdeaudu	AVR	8	16	spartan-3-5	James Brakefiel	internal error	4				##	14.7	0.33	1.0		verilog	1	softusb_na	yes	yes	N		64K	64K	Y		32	2	2010	2013	AVR data sheets	AVR clone, part of www.milkymist.org	
navre	Navre AVR clone	stable	Sebastien Bourdeaudu	AVR	8	16	spartan-6-3	James Brakefiel	1038	6			116	##	14.7	0.33	1.0	36.9	verilog	1	softusb_na	yes	yes	N		64K	64K	Y		32	2	2010	2013	AVR data sheets	AVR clone, part of www.milkymist.org	
navre	Navre AVR clone	stable	Sebastien Bourdeaudu	AVR	8	16	kintex-7-3	James Brakefiel	990	6			207	##	14.7	0.33	1.0	69.0	verilog	1	softusb_na	yes	yes	N		64K	64K	Y		32	2	2010	2013	AVR data sheets	AVR clone, part of www.milkymist.org	
navre	Navre AVR clone	stable	Sebastien Bourdeaudu	AVR	8	16	ecp-3-6	James Brakefiel	1338	4			40	##	3.1	0.33	1.0	9.8	verilog	1	softusb_na	yes	yes	N		64K	64K	Y		32	2	2010	2013	AVR data sheets	AVR clone, part of www.milkymist.org	
riscmcu	RISC Microcontr	stable	Yapzihe	AVR	8	16	arria-2	James Brakefiel	LPM paramet	6					14.7	0.33	1.0		vhdl	15	v_riscmcu	yes	yes	N		128	512	Y	92	16		2002	2009	AVR data sheets		
t400	*T400 uControlle*	stable	Arnim Laeuger	COP400	4	8x	cyclone-1	Arnim Laeuger	583	4		2	59			0.17	4.0	4.3	vhdl	53	t400_core	yes	asm	N		256	1K					2006	2009	COP400 data sheets	several variants	
t400	*T400 uControlle*	stable	Arnim Laeuger	COP400	4	8x	spartan-2	Arnim Laeuger	643	4		2	60			0.17	4.0	4.0	vhdl	53	t400_core	yes	asm	N		256	1K					2006	2009	COP400 data sheets	several variants	
cray1		alpha	Christopher Fenton	cray1	64	16	kintex-7-3	James Brakefiel	13463	6	19	10	127	##	14.7	6.00	1.0	56.6	verilog	46	cray_sys_t	yes	yes	Y	N	4M	4M	N		512		2010		CRAY data sheets	homebrew Cray1	www.chrisfenton.com/homebrew
cray1		alpha	Christopher Fenton	cray1	64	16	kintex-7-3	James Brakefiel	missing black	6				##	v14.1	6.00	1.0		verilog	46	cray_sys_t	yes	yes	Y	N	4M	4M	N		512		2010		CRAY data sheets	homebrew Cray1	www.chrisfenton.com/homebrew
aspida	ASPIDA DLX core	stable	Sotiriou	DLX	32	32	kintex-7-3	James Brakefiel	3586	6			257	##	14.7	1.00	1.0	71.7	verilog	10	DLX_top	yes	yes			4G	4G					2002	2009	Knuth DLX		compiled sync version
oc54x	OpenCores54x D	beta	Richard Herveille	DSP	16	16	kintex-7-3	James Brakefiel	2225	6	1		180	##	14.7	0.67	1.0	54.1	verilog	10	oc54_cpu	yes	yes	N	Y	64K	64K					2002	2009		40-bit accumulator, barrel shifter	C54x clone
t48	*T48 uControlle*	stable	Arnim Laeuger	MCS-48	8	8x	cyclone-1	Arnim Laeuger	738	4		1	59			0.33	4.0	6.6	vhdl	70	t48_core	yes	asm	N		256	1K					2004	2009	MCS-48 data sheets	used in several projects	
t48	*T48 uControlle*	stable	Arnim Laeuger	MCS-48	8	8x	spartan-2	Arnim Laeuger	771	4		1	30			0.33	4.0	3.2	vhdl	70	t48_core	yes	asm	N		256	1K					2004	2009	MCS-48 data sheets	used in several projects	
ion	Ion MIPS compa	mature	Jose Ruiz	MIPS	32	32	cyclone-2	Jose Ruiz	2349	4			50		q11.1	1.00	1.0	21.3	vhdl	12	mips_soc	yes	yes	N		4G	4G	Y		32		2011	2014	en.wikipedia.org/wiki/I	MIPS R3000 clone	originally MIPS-I moving to MIPS3
ion	Ion MIPS compa	mature	Jose Ruiz	MIPS	32	32	spartan-3	Jose Ruiz	3173	4			51		14.3	1.00	1.0	16.1	vhdl	12	mips_soc	yes	yes	N		4G	4G	Y		32		2011	2014	en.wikipedia.org/wiki/I	MIPS R3000 clone	originally MIPS-I moving to MIPS3
ion	Ion MIPS compa	mature	Jose Ruiz	MIPS	32	32	virtex-5	Jose Ruiz	2017	6			104		14.3	1.00	1.0	51.6	vhdl	12	mips_soc	yes	yes	N		4G	4G	Y		32		2011	2014	en.wikipedia.org/wiki/I	MIPS R3000 clone	originally MIPS-I moving to MIPS3
ion	Ion MIPS compa	mature	Jose Ruiz	MIPS	32	32	kintex-7-3	James Brakefiel	1533	6			163	##	14.7	1.00	1.0	106.0	vhdl	12	mips_soc	yes	yes	N		4G	4G	Y		32		2011	2014	en.wikipedia.org/wiki/I	MIPS R3000 clone	originally MIPS-I moving to MIPS3
minimips	miniMIPS	stable	Poppy etal	MIPS	32	32	kintex-7-3	James Brakefiel	2939	6	8		118	##	14.7	1.00	1.0	40.1	vhdl	12	minimips	yes	yes	N		4G	4G	Y		32	5			MIPS I		
mips_fault_t	Mips-FaultTolera	stable	Lazaridis	MIPS	32	32											1.0		vhdl			yes	yes	N		4G	4G	Y		32		2013		MIPS data sheets	arithmetic includes fault detection	
mips32r1	MIPS32 Release	stable	Grant Ayers	MIPS	32	32	cyclone-4	James Brakefiel	9556	4			48	##	q13.1	1.00	1.0	5.0	verilog	20	processor	yes	yes	N		4G	4G	Y		32		2012	2014	MIPS data sheets	Harvard arch	did not infer multipliers
mips32r1	MIPS32 Release	stable	Grant Ayers	MIPS	32	32	arria-2	James Brakefiel	3716	A	8		79	##	q13.1	1.00	1.0	21.3	verilog	20	processor	yes	yes	N		4G	4G	Y		32		2012	2014	MIPS data sheets	Harvard arch	
mips32r1	MIPS32 Release	stable	Grant Ayers	MIPS	32	32	spartan-3-5	James Brakefiel	6322	4	8		38	##	14.7	1.00	1.0	6.0	verilog	20	processor	yes	yes	N		4G	4G	Y		32		2012	2014	MIPS data sheets	Harvard arch	
mips32r1	MIPS32 Release	stable	Grant Ayers	MIPS	32	32	spartan-6-3	James Brakefiel	4823	6	8		43	##	14.7	1.00	1.0	8.8	verilog	20	processor	yes	yes	N		4G	4G	Y		32		2012	2014	MIPS data sheets	Harvard arch	
mips32r1	MIPS32 Release	stable	Grant Ayers	MIPS	32	32	kintex-7-3	James Brakefiel	4822	6	8		90	##	14.7	1.00	1.0	18.6	verilog	20	processor	yes	yes	N		4G	4G	Y		32		2012	2014	MIPS data sheets	Harvard arch	
mips789	mips789	stable	Li Wei	MIPS	32	32	kintex-7-3	James Brakefiel	1432	6		1	171	##	14.7	1.00	1.0	119.1	verilog	10	mips_core	yes	yes	N		4G	4G	Y		32		2007	2009	MIPS data sheets		
mips789	mips789	stable	Li Wei	MIPS	32	32	kintex-7-3	James Brakefiel	1432	6		1	171	##	14.7	1.00	1.0	119.1	verilog	10	mips_core	yes	yes	N		4G	4G	Y		32		2007	2009	MIPS data sheets		
mipsr2000	mipsr2000	stable	Lazaridis Dimitris	MIPS	32	32	kintex-7-3	James Brakefiel	1971	6	4	6	71	##	14.7	1.00	1.0	36.2	vhdl	35	Dm	yes	yes	N		4G	4G	Y		32	5	2012	2013	MIPS data sheets	course project	
plasma	Plasma most MI	stable	Steve Rhoads	MIPS	32	32	kintex-7-3	James Brakefiel	2462	6		3	97	##	14.7	1.00	1.0	39.5	vhdl	22	plasma	yes	yes	N		4G	4G	Y		32		2001	2013	MIPS data sheets	wide outside use, opencores page has list of related publications	
ucore	Ucore	stable	Whitewill	MIPS	32	32	kintex-7-3	James Brakefiel	2469	6		1	231	##	14.7	1.00	1.0	93.5	verilog	25	ucore	yes	yes	N		4G	4G	Y		32	6	2005	2010	MIPS data sheets	MMU & caches	
yacc	YACC Yet Anothe	stable	Tak Sugawara	MIPS	32	32	arria-2	James Brakefiel	map errors	A				##	q13.1	1.00	1.0		verilog	10	yacc2	yes	yes	N		4G	4G	Y		32	5	2005	2009	MIPS data sheets	derived from, but independent of plasma, xilinx & altera implemntatior	
yacc	YACC Yet Anothe	stable	Tak Sugawara	MIPS	32	32	kintex-7-3	James Brakefiel	map c	2220	6	6		##	14.7	1.00	1.0		verilog	10	yacc2	yes	yes	N		4G	4G	Y		32	5	2005	2009	MIPS data sheets	derived from, but independent of plasma, xilinx & altera implemntatior	
yellowstar	Yellow Star	stable	Charles Brej	MIPS	32	32			missing declarations										verilog	1	processor	yes	yes	N		4G	4G	Y		32		2001	2013	MIPS data sheets	MIPS R3000 clone, gate level dsgn	brej.org/yellow_star/
m1_core	M1 Core	beta	Fabrizo Fazzino, Albert	MIPS?	32	32	cyclone-2	James Brakefiel	3752	4			70	##	q11.1s	1.00	1.0	18.8	verilog	9	m1_core		yes	N		4G	4G	Y		32		2007	2012		GCC target?	
m1_core	M1 Core	beta	Fabrizo Fazzino, Albert	MIPS?	32	32	cyclone-4	James Brakefiel	3795	4			94	##	q13.1	1.00	1.0	24.8	verilog	9	m1_core		yes	N		4G	4G	Y		32		2007	2012		GCC target?	
m1_core	M1 Core	beta	Fabrizo Fazzino, Albert	MIPS?	32	32	arria-2	James Brakefiel	2101	A			190	##	q13.1	1.00	1.0	90.6	verilog	9	m1_core		yes	N		4G	4G	Y		32		2007	2012		GCC target?	
m1_core	M1 Core	beta	Fabrizo Fazzino, Albert	MIPS?	32	32	spartan-3-5	James Brakefiel	4688	4			70	##	14.7	1.00	1.0	14.9	verilog	9	m1_core		yes	N		4G	4G	Y		32		2007	2012		GCC target?	
m1_core	M1 Core	beta	Fabrizo Fazzino, Albert	MIPS?	32	32	spartan-6-3	James Brakefiel	3483	6			131	##	14.7	1.00	1.0	37.5	verilog	9	m1_core		yes	N		4G	4G	Y		32		2007	2012		GCC target?	
m1_core	M1 Core	beta	Fabrizo Fazzino, Albert	MIPS?	32	32	kintex-7-3	James Brakefiel	3456	6			233	##	14.7	1.00	1.0	67.3	verilog	9	m1_core		yes	N		4G	4G	Y		32		2007	2012		GCC target?	
fpgammix		stable	Tommy Thorn	MMIX	64	32	arria-2	James Brakefiel	11605	A	8	10	94	##	q13.1	1.50	4.0	3.0	system ve	2	core	yes	yes	Y	Y	4G	4G	Y	256	288		2006	2008		clone of Knuth's MMIX	micro-coded
openmsp430	*openMSP430*	stable	Oliver Girard	msp430	16	16x	cyclone-4-6	Oliver Girard	1750	4	1		52			0.67	2.0	9.9	verilog	30	openMSP4	yes	yes	N	N	64K	64K	Y		16		2009	2014	msp430 data sheets	performance spreadsheet	
openmsp430	*openMSP430*	stable	Oliver Girard	msp430	16	16x	stratix-3-2	Oliver Girard	1147	A	1		98			0.67	2.0	28.5	verilog	30	openMSP4	yes	yes	N	N	64K	64K	Y		16		2009	2014	msp430 data sheets	performance spreadsheet	
openmsp430	*openMSP430*	stable	Oliver Girard	msp430	16	16x	spartan-6-4	Oliver Girard	1424	6	1		68			0.67	2.0	15.9	verilog	30	openMSP4	yes	yes	N	N	64K	64K	Y		16		2009	2014	msp430 data sheets	performance spreadsheet	
openmsp430	*openMSP430*	stable	Oliver Girard	msp430	16	16x	virtex-6-3	Oliver Girard	1387	6	1		116			0.67	2.0	27.9	verilog	30	openMSP4	yes	yes	N	N	64K	64K	Y		16		2009	2014	msp430 data sheets	performance spreadsheet	
nios2		proprietar	Altera	Nios II	32	32	cyclone-4-6	Altera		2065	4			160			1.13	1.0	87.2	not avail			yes	yes	opt		4G	4G	Y		32		2004		NIOS2 data sheets	fltg-pt, caches & MMU options	Nios II/f: fastest version
nios2		proprietar	Altera	Nios II	32	32	arria-2	Altera		1355	A			170			1.13	1.0	141.1	not avail			yes	yes	opt		4G	4G	Y		32		2004		NIOS2 data sheets	fltg-pt, caches & MMU options	Nios II/f: fastest version
nios2		proprietar	Altera	Nios II	32	32	cyclone-5	Altera		1050	A			160			1.13	1.0	171.4	not avail			yes	yes	opt		4G	4G	Y		32		2004		NIOS2 data sheets	fltg-pt, caches & MMU options	Nios II/f: fastest version
nios2		proprietar	Altera	Nios II	32	32	arria-5	Altera		1355	A			280			1.13	1.0	232.5	not avail			yes	yes	opt		4G	4G	Y		32		2004		NIOS2 data sheets	fltg-pt, caches & MMU options	Nios II/f: fastest version
nios2		proprietar	Altera	Nios II	32	32	stratix-5	Altera		895	A			310			1.13	1.0	389.7	not avail			yes	yes	opt		4G	4G	Y		32		2004		NIOS2 data sheets	fltg-pt, caches & MMU options	Nios II/f: fastest version
nios2		proprietar	Altera	Nios II	32	32	cyclone-4-6	Altera		1915	4			130			0.64	1.0	43.2	not avail			yes	yes	opt		4G	4G	Y		32		2004		NIOS2 data sheets	fltg-pt, caches & MMU options	Nios II: balanced version
nios2		proprietar	Altera	Nios II	32	32	arria-2	Altera		1045	A			170			0.64	1.0	103.4	not avail			yes	yes	opt		4G	4G	Y		32		2004		NIOS2 data sheets	fltg-pt, caches & MMU options	Nios II: balanced version
nios2		proprietar	Altera	Nios II	32	32	cyclone-5	Altera		1570	A			140			0.64	1.0	56.7	not avail			yes	yes	opt		4G	4G	Y		32		2004		NIOS2 data sheets	fltg-pt, caches & MMU options	Nios II: balanced version
nios2		proprietar	Altera	Nios II	32	32	arria-5	Altera		1045	A			250			0.64	1.0	152.1	not avail			yes	yes	opt		4G	4G	Y		32		2004		NIOS2 data sheets	fltg-pt, caches & MMU options	Nios II: balanced version
nios2		proprietar	Altera	Nios II	32	32	stratix-5	Altera		1300	A			300			0.64	1.0	146.7	not avail			yes	yes	opt		4G	4G	Y		32		2004		NIOS2 data sheets	fltg-pt, caches & MMU options	Nios II: balanced version
nios2		proprietar	Altera	Nios II	32	32	cyclone-4-6	Altera		1080	4			170			0.15	1.0	23.6	not avail			yes	yes	N		4G	4G	Y		32		2004		NIOS2 data sheets	serial arithmetic	Nios II/e: minimum LUTs version
nios2		proprietar	Altera	Nios II	32	32	arria-2	Altera		730	A			300			0.15	1.0	61.6	not avail			yes	yes	N		4G	4G	Y		32		2004		NIOS2 data sheets	serial arithmetic	Nios II/e: minimum LUTs version
nios2		proprietar	Altera	Nios II	32	32	cyclone-5	Altera		840	A			200			0.15	1.0	35.7	not avail			yes	yes	N		4G	4G	Y		32		2004		NIOS2 data sheets	serial arithmetic	Nios II/e: minimum LUTs version
nios2		proprietar	Altera	Nios II	32	32	arria-5	Altera		730	A			320			0.15	1.0	65.8	not avail			yes	yes	N		4G	4G	Y		32		2004		NIOS2 data sheets	serial arithmetic	Nios II/e: minimum LUTs version
nios2		proprietar	Altera	Nios II	32	32	stratix-5	Altera		445	A			340			0.15	1.0	114.6	not avail			yes	yes	N		4G	4G	Y		32		2004		NIOS2 data sheets	serial arithmetic	Nios II/e: minimum LUTs version
pdp1	PDP-1 reimplem	alpha	Yann Vernier	PDP1	18	18	spartan-3a	James Brakefiel	1390	4		6	138	##	14.7	0.50	10.0	5.0	vhdl		top	yes	yes	N	N	4K	4K		28			2011	2011	http://pdp-1.computer	PDP-1 descended from MIT TX-0	uses Minimal UART from opencor
pdp11-34verilog		stable	Brad Parker	PDP11	16	16x	cyclone-2	James Brakefiel	3340	4			50	##	q11.1s	0.67	2.0	5.0	verilog	24	pdp11	yes	yes	N	N	64K	64K			8		2009		PDP11 data sheets	boots & runs RT-11, EIS inst & MMU	www.heeltoe.com/download/pdp
pdp11-34verilog		stable	Brad Parker	PDP11	16	16x	cyclone-4	James Brakefiel	3439	4			64	##	q13.1	0.67	2.0	6.2	verilog	24	pdp11	yes	yes	N	N	64K	64K			8		2009		PDP11 data sheets	boots & runs RT-11, EIS inst & MMU	www.heeltoe.com/download/pdp
pdp11-34verilog		stable	Brad Parker	PDP11	16	16x	arria-2	James Brakefiel	2532	A			126	##	q13.1	0.67	2.0	16.7	verilog	24	pdp11	yes	yes	N	N	64K	64K			8		2009		PDP11 data sheets	boots & runs RT-11, EIS inst & MMU	www.heeltoe.com/download/pdp
pdp11-34verilog		stable	Brad Parker	PDP11	16	16x	spartan-3-5	James Brakefiel	3842	4			56	##	14.7	0.67	2.0	4.8	verilog	24	pdp11	yes	yes	N	N	64K	64K			8		2009		PDP11 data sheets	boots & runs RT-11, EIS inst & MMU	www.heeltoe.com/download/pdp
pdp11-34verilog		stable	Brad Parker	PDP11	16	16x	spartan-6-3	James Brakefiel	2966	6			64	##	14.7	0.67	2.0	7.3	verilog	24	pdp11	yes	yes	N	N	64K	64K			8		2009		PDP11 data sheets	boots & runs RT-11, EIS inst & MMU	www.heeltoe.com/download/pdp
pdp11-34verilog		stable	Brad Parker	PDP11	16	16x	kintex-7-3	James Brakefiel	3089	6			153	##	14.7	0.67	2.0	16.6	verilog	24	pdp11	yes	yes	N	N	64K	64K			8		2009		PDP11 data sheets	boots & runs RT-11, EIS inst & MMU	www.heeltoe.com/download/pdp
pdp2011		stable	Sytse van Slooten	PDP11	16	16x	arria-2	James Brakefiel	4888	A	2	1	162	##	q13.1	0.67	2.0	11.1	vhdl	3	cpu	yes	yes	Y	N	64K	64K			8		2008	2014	PDP11 data sheets	SoC, build files for A&X boards	http://pdp2011.sytse.net/wordpr
pdp2011		stable	Sytse van Slooten	PDP11	16	16x	arria-2	James Brakefiel	13221	A	2	14	35	##	q13.1	0.67	2.0	0.9	vhdl	32	unibus	yes	yes	Y	N	4M	4M			8		2008	2014	PDP11 data sheets	SoC, build files for A&X boards	http://pdp2011.sytse.net/wordpr
pdp2011		stable	Sytse van Slooten	PDP11	16	16x	kintex-7-3	James Brakefiel	5060	6	1		205	##	14.7	0.67	2.0	13.6	vhdl	3	cpu	yes	yes	Y	N	64K	64K			8		2008	2014	PDP11 data sheets	SoC, build files for A&X boards	http://pdp2011.sytse.net/wordpr
pdp2011		stable	Sytse van Slooten	PDP11	16	16x	kintex-7-3	James Brakefiel	13495	6	1	3	6	##	14.7	0.67	2.0	0.2	vhdl	32	unibus	yes	yes	Y	N	4M	4M			8		2008	2014	PDP11 data sheets	SoC, build files for A&X boards	http://pdp2011.sytse.net/wordpr
pdp2011		stable	Sytse van Slooten	PDP11	16	16x	kintex-7-3	James Brakefiel	13327	6	1		45	##	v14.1	0.67	2.0	1.1	vhdl	32	unibus	yes	yes	Y	N	4M	4M			8		2008	2014	PDP11 data sheets	SoC, build files for A&X boards	http://pdp2011.sytse.net/wordpr
w11	PDP-11/70 CPU (	alpha	Walter Mueller	PDP11	8	16x	spartan-6	Walter Mueller	3418	6			80			0.67	2.0	7.8	vhdl	26	pdp11	yes	yes	N	N	4M	4M	Y		8		2010	2013	PDP11 data sheets	Boots UNIX, has MMU & cache, retro project	
w11	PDP-11/70 CPU (	alpha	Walter Mueller	PDP11	8	16x	kintex-7-3	James Brakefiel	1760	6	1	1	147	##	14.7	0.67	2.0	28.0	vhdl	118	pdp11_cor	yes	yes	N	N	4M	4M	Y		8		2010	2013	PDP11 data sheets	Boots UNIX, has MMU & cache, retro project	
w11	PDP-11/70 CPU (	alpha	Walter Mueller	PDP11	8	16x	kintex-7-3	James Brakefiel	3174	6	1	3	131	##	14.7	0.67	2.0	13.9	vhdl	133	sys_w11a_	yes	yes	N	N	4M	4M	Y		8		2010	2013	PDP11 data sheets	Boots UNIX, has MMU & cache, retro project	

pdp8	PDP-8 Processor	alpha	Joe Manojlovick, Rob D	PDP8	12	12	spartan-6-3	James Brakefiel		1332	6	1		81	##	14.7	0.50	2.0	15.1	vhdl	55	cpu	yes	yes	N	N	32K	32K			8		2012	2013	PDP8 data sheets	Boots OS/8, runs apps, several variants	
pdp8	PDP-8 Processor	alpha	Joe Manojlovick, Rob D	PDP8	12	12	kintex-7-3	James Brakefiel		1219	6	1		183	##	14.7	0.50	2.0	37.5	vhdl	55	cpu	yes	yes	N	N	32K	32K			8		2012	2013	PDP8 data sheets	Boots OS/8, runs apps, several variants	
pdp8l	Minimal PDP8/L	beta	Ian Schofield	PDP8	12	12	cyclone-3	James Brakefiel		1088	4		48	63	##	q13.1	0.50	2.0	14.4	vhdl	11	top	yes	yes	N	N	4K	4K					2013		PDP8 data sheets		
pdp8verilog		stable	Brad Parker	PDP8	12	12	spartan-6-3	James Brakefiel		509	6			162	##	14.7	0.50	2.0	79.5	verilog	18	pdp8	yes	yes	N	N	32K	32K			8		2005	2010	PDP8 data sheets	boots & runs TSS/8 & Basic	www.heeltoe.com/download/pdp
pdp8verilog		stable	Brad Parker	PDP8	12	12	kintex-7-3	James Brakefiel		505	6			366	##	14.7	0.50	2.0	181.3	verilog	18	pdp8	yes	yes	N	N	32K	32K			8		2005	2010	PDP8 data sheets	boots & runs TSS/8 & Basic	www.heeltoe.com/download/pdp
pdp8verilog		stable	Brad Parker	PDP8	12	12	kintex-7-3	James Brakefiel		1117	6			251	##	14.7	0.50	2.0	56.1	verilog	18	top	yes	yes	N	N	32K	32K			8		2005	2010	PDP8 data sheets	boots & runs TSS/8 & Basic	www.heeltoe.com/download/pdp
synpic12		stable	Miguel Angel Ajo Pelay	PIC12	8	12	cyclone-2-6	James Br	ROM	1436	4		1	76	##	q11.1s	0.33	1.0	17.5	vhdl	7	synpic12	yes	yes	N	N	256	2K	Y				2011	2011	PIC12 data sheets	CHDL to verilog	http://projects.nbee.es/display/IP
synpic12		stable	Miguel Angel Ajo Pelay	PIC12	8	12	cyclone-4-6	James Br	ROM	1417	4		1	96	##	q13.1	0.33	1.0	22.4	vhdl	7	synpic12	yes	yes	N	N	256	2K	Y				2011	2011	PIC12 data sheets	CHDL to verilog	http://projects.nbee.es/display/IP
synpic12		stable	Miguel Angel Ajo Pelay	PIC12	8	12	arria-2	James Br	ROM	1098	A			154	##	q13.1	0.33	1.0	46.2	vhdl	7	synpic12	yes	yes	N	N	256	2K	Y				2011	2011	PIC12 data sheets	CHDL to verilog	http://projects.nbee.es/display/IP
synpic12		stable	Miguel Angel Ajo Pelay	PIC12	8	12	spartan-3-5	James Brakefiel		805	4		1	58	##	14.7	0.33	1.0	23.8	vhdl	7	synpic12	yes	yes	N	N	256	2K	Y				2011	2011	PIC12 data sheets	CHDL to verilog	http://projects.nbee.es/display/IP
synpic12		stable	Miguel Angel Ajo Pelay	PIC12	8	12	spartan-6-3	James Brakefiel		517	6		1	89	##	14.7	0.33	1.0	57.0	vhdl	7	synpic12	yes	yes	N	N	256	2K	Y				2011	2011	PIC12 data sheets	CHDL to verilog	http://projects.nbee.es/display/IP
synpic12		stable	Miguel Angel Ajo Pelay	PIC12	8	12	kintex-7-3	James Brakefiel		474	6		1	197	##	14.7	0.33	1.0	136.8	vhdl	7	synpic12	yes	yes	N	N	256	2K	Y				2011	2011	PIC12 data sheets	CHDL to verilog	http://projects.nbee.es/display/IP
altium/TSK165x		proprietar	Altium	PIC16	8	12	cyclone-2	Altium		428	4			50			0.33	1.0	38.6	not avail			yes	yes	N	Y	256	4K	Y				2004		CR0140.PDF	asm, C, C++, schem, VHDL & Verilog	default clock speed is 50MHz
altium/TSK165x		proprietar	Altium	PIC16	8	12	spartan-3-5	Altium		416	4			50			0.33	1.0	39.7	not avail			yes	yes	N	Y	256	4K	Y				2004		CR0140.PDF	asm, C, C++, schem, VHDL & Verilog	default clock speed is 50MHz
free_risc8		stable	Thomas Coonan	PIC16	8	14	kintex-7-3	James Brakefiel		355	6			142	##	14.7	0.33	1.0	132.2	verilog	8	cpu	yes	yes	N		256	4K	Y				2002	2011	PIC16 data sheets		
m16c5x	SoC:M16C5x	mature	Michael Morris	PIC16	8	14	spartan-3-4	Michael Morris		1265	4		3	60	##		0.33	1.0	15.7	verilog	3	m16C5x	yes	yes	N	Y	256	4K	Y				2013	2014	PIC16 data sheets	SOC LUT count	core at P16C5X
minirisc	Mini-Risc core	stable	Rudolf Usselmann	PIC16	8	14	spartan-3	Rudolf Usselma		460	4			80			0.33	1.0	57.4	verilog	7	risc_core_t	yes	yes	N	Y	256	4K	Y				2001	2012	PIC16 data sheets		
p16c5x	P16C5x	mature	Michael Morris	PIC16	8	14	cyclone-2	James Brakefiel		1216	4			87	##	q11.1s	0.33	1.0	23.7	verilog	3	P16C5x	yes	yes	N	Y	256	4K	Y				2013	2014	PIC16 data sheets		
p16c5x	P16C5x	mature	Michael Morris	PIC16	8	14	cyclone-4	James Brakefiel		1201	4			102	##	q13.1	0.33	1.0	27.9	verilog	3	P16C5x	yes	yes	N	Y	256	4K	Y				2013	2014	PIC16 data sheets		
p16c5x	P16C5x	mature	Michael Morris	PIC16	8	14	arria-2	James Brakefiel		649	A			176	##	q13.1	0.33	1.0	89.7	verilog	3	P16C5x	yes	yes	N	Y	256	4K	Y				2013	2014	PIC16 data sheets		
p16c5x	P16C5x	mature	Michael Morris	PIC16	8	14	spartan-3-5	James Brakefiel		487	4			90	##	14.7	0.33	1.0	60.7	verilog	3	P16C5x	yes	yes	N	Y	256	4K	Y				2013	2014	PIC16 data sheets		
p16c5x	P16C5x	mature	Michael Morris	PIC16	8	14	spartan-6-3	James Brakefiel		352	6			133	##	14.7	0.33	1.0	124.2	verilog	3	P16C5x	yes	yes	N	Y	256	4K	Y				2013	2014	PIC16 data sheets		
p16c5x	P16C5x	mature	Michael Morris	PIC16	8	14	kintex-7-3	James Brakefiel		378	6			252	##	14.7	0.33	1.0	220.2	verilog	3	P16C5x	yes	yes	N	Y	256	4K	Y				2013	2014	PIC16 data sheets		
ppx16	PPX16 mcu	stable	Daniel Wallner	PIC16	8	14	spartan-6-3	James Br	missing ROM BB							14.7		1.0		vhdl	10	P16C55, P1	yes	yes	N	Y	256	4K	Y				2002	2009	PIC16 data sheets	both 16C55 & 16F84	
recore54		beta	ht-lab.com	PIC16	8	14	kintex-7-3	James Br	Cannot find <		6					14.7	0.33	1.0		vhdl	20	rcore54_sy	yes	yes	N	Y	256	4K	Y				1999		PIC16 data sheets	PIC16 clone	www.ht-lab.com
risc16f84	risc16f84	stable	John Clayton	PIC16	8	14	kintex-7-3	James Brakefiel		331	6			333	##	14.7	0.33	1.0	332.3	verilog	1	risc16f84_	yes	yes	N	Y	256	4K	Y				2002	2013	PIC16 data sheets	derived from CQPIC by Sumio Morioka	
risc5x	RISC5x	stable	MikeJ	PIC16	8	14	kintex-7-3	James Br	RLOC constra		6					14.7	0.33	1.0		vhdl	15	cpu	yes	yes	N	Y	256	4K	Y				2002	2011	PIC16 data sheets	makes extensive use of xilinx primitives	
cqpic		stable	Sumio Morioka	PIC16	8	14	arria-2	James Br	ROM parame		A				##	q13.1	0.67	1.0		vhdl & ve	5	CQPIC	yes	yes	N	Y	256	4K	Y				1999	2004	PIC16 data sheets	LPM macros	http://www002.upp.so-net.ne.jp/
pic_coonan		alpha	Tom Coonan	PIC16	8	14	kintex-7-3	James Brakefiel		328	6		1	165	##	14.7	0.33	1.0	166.1	verilog	7	piccpu	yes	yes	N	Y	256	4K	Y				1999		PIC16 data sheets		
ae18	ae18	beta	Shawn Tan	PIC18	16	24	cyclone-2	James Brakefiel		1395	4	1	1	133	##	q11.1s	0.67	1.0	63.7	verilog	1	ae18_core		yes	N	Y	4K	1M					2003	2009	PIC18 data sheets	not 100% compatable	negative edge reset "clock"
ae18	ae18	beta	Shawn Tan	PIC18	16	24	cyclone-4-6	James Brakefiel		1505	4		1	144	##	q13.1	0.67	1.0	64.2	verilog	1	ae18_core		yes	N	Y	4K	1M					2003	2009	PIC18 data sheets	not 100% compatable	negative edge reset "clock"
ae18	ae18	beta	Shawn Tan	PIC18	16	24	arria-2	James Brakefiel		1084	A	1		207	##	q13.1	0.67	1.0	128.2	verilog	1	ae18_core		yes	N	Y	4K	1M					2003	2009	PIC18 data sheets	not 100% compatable	negative edge reset "clock"
ae18	ae18	beta	Shawn Tan	PIC18	16	24	spartan-6-3	James Brakefiel		1176	6	1		81	##	14.7	0.67	1.0	46.2	verilog	1	ae18_core		yes	N	Y	4K	1M					2003	2009	PIC18 data sheets	not 100% compatable	negative edge reset "clock"
ae18	ae18	beta	Shawn Tan	PIC18	16	24	virtex-6-3	James Brakefiel		1133	6	1		117	##	14.7	0.67	1.0	69.1	verilog	1	ae18_core		yes	N	Y	4K	1M					2003	2009	PIC18 data sheets	not 100% compatable	negative edge reset "clock"
ae18	ae18	beta	Shawn Tan	PIC18	16	24	kintex-7-3	James Brakefiel		1131	6	1		68	##	14.7	0.67	1.0	40.5	verilog	1	ae18_core		yes	N	Y	4K	1M					2003	2009	PIC18 data sheets	not 100% compatable	negative edge reset "clock"
copyblaze	copyBlaze	stable	Abdallah Ellbrahimi	picoBlaze	8	18	cyclone-2	James Br	missir	1348	4			77	##	q11.1s	0.33	2.0	9.5	vhdl	16	cp_copybl	yes	asm	N		256	2K	Y				2011	2013	microBlaze data sheets	wishbone extras	
copyblaze	copyBlaze	stable	Abdallah Ellbrahimi	picoBlaze	8	18	cyclone-4-6	James Br	missir	1345	4			104	##	q13.1	0.33	2.0	12.7	vhdl	16	cp_copybl	yes	asm	N		256	2K	Y				2011	2013	microBlaze data sheets	wishbone extras	
copyblaze	copyBlaze	stable	Abdallah Ellbrahimi	picoBlaze	8	18	arria-2	James Br	missir	604	A			167	##	q13.1	0.33	2.0	45.6	vhdl	16	cp_copybl	yes	asm	N		256	2K	Y				2011	2013	microBlaze data sheets	wishbone extras	
copyblaze	copyBlaze	stable	Abdallah Ellbrahimi	picoBlaze	8	18	spartan-3e-	James Br	missir	875	4			79	##	14.7	0.33	2.0	14.9	vhdl	16	cp_copybl	yes	asm	N		256	2K	Y				2011	2013	microBlaze data sheets	wishbone extras	
copyblaze	copyBlaze	stable	Abdallah Ellbrahimi	picoBlaze	8	18	spartan-6-3	James Br	missir	619	6			86	##	14.7	0.33	2.0	22.8	vhdl	16	cp_copybl	yes	asm	N		256	2K	Y				2011	2013	microBlaze data sheets	wishbone extras	
copyblaze	copyBlaze	stable	Abdallah Ellbrahimi	picoBlaze	8	18	kintex-7-3	James Br	missir	622	6			217	##	14.7	0.33	2.0	57.5	vhdl	16	cp_copybl	yes	asm	N		256	2K	Y				2011	2013	microBlaze data sheets	wishbone extras	
pacoBlaze		mature	Pablo Kocik	picoBlaze	8	18	spartan-3	Pablo Kocik		177	4		1	117			0.33	2.0	109.1	verilog	18	pacoblaze	yes	asm	N		256	2K	Y	57		2		2006	bleyer.org/pacoblaze	3 versions, behavioral coding	
picoblaze	picoblaze	stable	Ken Chapman	picoBlaze	8	18	spartan-3-4	James Brakefiel		178	4			182	##	14.7	0.33	2.0	168.9	vhdl	1	kcspm3	yes	asm	N		256	2K	Y				2003		picoblaze data sheets	2 clocks per inst	this is the original picoBlaze autho
picoblaze	picoblaze	stable	Ken Chapman	picoBlaze	8	18	kintex-7-3	James Br	ROM parame		6				##	14.7	0.33	2.0		vhdl	1	kcspm3	yes	asm	N		256	2K	Y				2003		picoblaze data sheets	2 clocks per inst	this is the original picoBlaze autho
mips_16	Educational 16-b	stable	Doyya Doyya	RISC	16	16	kintex-7-3	James Br	collapsed in c		6					14.7	1.00	1.0		verilog	12	mips_16_c	yes		N		64K	64K		13	8	5	2012	2012			
leon		stable	Jiri Gaisler, Jan Anderss	SPARC	32	32				3500								1.0		vhdl	100s	leon3x	yes	yes	Y		4G	4G			64		2003	2013	SPARC data sheets	customized for ~50 FPGA boards, configurable	
s1_core	S1 Core	stable	Fabrizio Fazzino etal	SPARC	64	32	kintex-7-3	James Brakefiel		54434	6	8	57	50	##	14.7	2.00	1.0	1.8	verilog	136	s1_top	yes	yes	Y	N	4G	4G	Y		32		2007	2012	SPARC data sheets	reduced version of OpenSPARC T1	ISE run
s1_core	S1 Core	stable	Fabrizio Fazzino etal	SPARC	64	32	kintex-7-3	James Brakefiel		52845	6	8	59	56	##	v14.1	2.00	1.0	2.1	verilog	136	s1_top	yes	yes	Y	N	4G	4G	Y		32		2007	2012	SPARC data sheets	reduced version of OpenSPARC T1	Vivado run
aquarius	aquarius	stable	Thorn Aitch	SuperH-2	32	16	cyclone-2	James Brakefiel		5237	4	2	32	33	##	q11.1s	1.00	1.0	6.3	verilog	21	top	yes	yes	N		4G	4G	Y				2003	2009	SuperH data sheets		
aquarius	aquarius	stable	Thorn Aitch	SuperH-2	32	16	cyclone-4-6	James Brakefiel		6034	4		32	43	##	q13.1	1.00	1.0	7.2	verilog	21	top	yes	yes	N		4G	4G	Y				2003	2009	SuperH data sheets		
aquarius	aquarius	stable	Thorn Aitch	SuperH-2	32	16	arria-2	James Brakefiel		3209	A	4	32	70	##	q13.1	1.00	1.0	22.0	verilog	21	top	yes	yes	N		4G	4G	Y				2003	2009	SuperH data sheets		
aquarius	aquarius	stable	Thorn Aitch	SuperH-2	32	16	spartan-3-5	James Brakefiel		5618	4	2	32	31	##	14.7	1.00	1.0	5.5	verilog	21	top	yes	yes	N		4G	4G	Y				2003	2009	SuperH data sheets		
aquarius	aquarius	stable	Thorn Aitch	SuperH-2	32	16	spartan-6-3	James Brakefiel		4180	6	2	12	49	##	14.7	1.00	1.0	11.8	verilog	21	top	yes	yes	N		4G	4G	Y				2003	2009	SuperH data sheets		
aquarius	aquarius	stable	Thorn Aitch	SuperH-2	32	16	kintex-7-3	James Brakefiel		4071	6	2	10	97	##	14.7	1.00	1.0	23.7	verilog	21	top	yes	yes	N		4G	4G	Y				2003	2009	SuperH data sheets		
aeMB	aeMB	beta	Shawn Tan	uBlaze	32	32	cyclone-2	James Brakefiel		1605	4	3	4	74	##	q11.1s	1.00	1.0	46.2	verilog	7	aeMB_core	yes	yes	N		4G	4G	Y				2004	2009	xilinx documentation	not 100% compatable	
aeMB	aeMB	beta	Shawn Tan	uBlaze	32	32	cyclone-4-6	James Brakefiel		2286	4		4	68	##	q13.1	1.00	1.0	29.5	verilog	7	aeMB_core	yes	yes	N		4G	4G	Y				2004	2009	xilinx documentation	not 100% compatable	
aeMB	aeMB	beta	Shawn Tan	uBlaze	32	32	arria-2	James Brakefiel		1078	A	4	4	104	##	q13.1	1.00	1.0	96.1	verilog	7	aeMB_core	yes	yes	N		4G	4G	Y				2004	2009	xilinx documentation	not 100% compatable	
aeMB	aeMB	beta	Shawn Tan	uBlaze	32	32	spartan-3e-	James Brakefiel		1514	4	3	3	54	##	i14.7	1.00	1.0	35.5	verilog	7	aeMB_core	yes	yes	N		4G	4G	Y				2004	2009	xilinx documentation	not 100% compatable	
aeMB	aeMB	beta	Shawn Tan	uBlaze	32	32	spartan-6-3	James Brakefiel		1053	6	3		71	##	i14.7	1.00	1.0	67.3	verilog	7	aeMB_core	yes	yes	N		4G	4G	Y				2004	2009	xilinx documentation	not 100% compatable	
aeMB	aeMB	beta	Shawn Tan	uBlaze	32	32	kintex-7-3	James Brakefiel		1018	6	3		131	##	14.7	1.00	1.0	128.5	verilog	7	aeMB_core	yes	yes	N		4G	4G	Y				2004	2009	xilinx documentation	not 100% compatable	
mblite	MB-Lite	beta	Tamar Kranenburg	uBlaze	32	32	cyclone-2	James Brakefiel		1250	4		3	88	##	q11.1s	1.00	1.0	70.8	vhdl	18	core_wb	yes	yes	N		4G	4G	Y	86	32		2009	2012	microBlaze data sheets	not all instructions implemented	
mblite	MB-Lite	beta	Tamar Kranenburg	uBlaze	32	32	cyclone-4	James Brakefiel		1255	4		3	115	##	q13.1	1.00	1.0	91.4	vhdl	18	core_wb	yes	yes	N		4G	4G	Y	86	32		2009	2012	microBlaze data sheets	not all instructions implemented	
mblite	MB-Lite	beta	Tamar Kranenburg	uBlaze	32	32	arria-2	James Brakefiel		784	A		3	183	##	q13.1	1.00	1.0	232.9	vhdl	18	core_wb	yes	yes	N		4G	4G	Y	86	32		2009	2012	microBlaze data sheets	not all instructions implemented	
mblite	MB-Lite	beta	Tamar Kranenburg	uBlaze	32	32	spartan-3-5	James Brakefiel		1367	4		3	80	##	14.7	1.00	1.0	58.9	vhdl	18	core_wb	yes	yes	N		4G	4G	Y	86	32		2009	2012	microBlaze data sheets	not all instructions implemented	moved everything to work library
mblite	MB-Lite	beta	Tamar Kranenburg	uBlaze	32	32	spartan-6-3	James Brakefiel		911	6		2	114	##	14.7	1.00	1.0	125.3	vhdl	18	core_wb	yes	yes	N		4G	4G	Y	86	32		2009	2012	microBlaze data sheets	not all instructions implemented	moved everything to work library
mblite	MB-Lite	beta	Tamar Kranenburg	uBlaze	32	32	kintex-7-3	James Brakefiel		941	6		2	227	##	14.7	1.00	1.0	240.9	vhdl	18	core_wb	yes	yes	N		4G	4G	Y	86	32		2009	2012	microBlaze data sheets	not all instructions implemented	moved everything to work library
microblaze		proprietar	Xilinx	uBlaze	32	32	kintex-7	Xilinx		1201	6		32	408			1.30	1.0	441.4	not avail			yes	yes	opt		4G	4G	Y	86	32	5	2002		www.xilinx.com/tools/	performance optimized	70 configuration options, MMU op
microblaze		proprietar	Xilinx	uBlaze	32	32	kintex-7	Xilinx		546	6		1	320			1.03	1.0	603.7	not avail			yes	yes	opt		4G	4G	Y	86	32	3	2002		www.xilinx.com/tools/	MicroBlaze MCS, smallest configurat	70 configuration options, MMU op
myblaze	myBlaze	mature	Jian Luo	uBlaze	32	32												1.0		myhdl			yes	yes	N		4G	4G	Y		32		2010	2010	microBlaze data sheets	clone, python code generators	
openfire2	OpenFIRE	beta	Antonio Anton	uBlaze	32	32	spartan-3-5	James Brakefiel		1352	4	3	6	39	##	14.7	1.00	1.0	28.8	verilog	27	openfire_s	yes	yes	N	N	4G	4G	Y		32		2007	2012	uBlaze data sheets	"FPGA Proven"	derived from Stephen Craven's Op
openfire2	OpenFIRE	beta	Antonio Anton	uBlaze	32	32	kintex-7-3	James Brakefiel		1201	6	3	2	105	##	14.7	1.00	1.0	87.4	verilog	27	openfire_s	yes	yes	N	N	4G	4G	Y		32		2007	2012	uBlaze data sheets	"FPGA Proven"	derived from Stephen Craven's Op
secretblaze		beta	Lyonel Barthe	uBlaze	32	32	spartan-3-4	Lyonel Barthe		1563	4			91		i12.1	1.00	1.0	58.2	vhdl	26	sb_core		yes			4G	4G	Y	86	32	5	2010	2012	www.lirmm.fr/ADAC/		
ao486	ao486	beta	Aleksander Osman	x86	32	8x	cyclone-4-7	Aleksander Osm		91256	4	22	106	39		q13.1	1.00	1.0	0.4	verilog	85	soc	yes	yes			4G	4G	Y				2014	2014	x86 data sheets	complete 486, SoC configuration	running on Terasic DE2-115 board
ao486	ao486	beta	Aleksander Osman	x86	32	8x	cyclone-4-7	James Brakefiel		36094	4	4	47	46	##	q13.1	1.00	1.0	1.3	verilog	85	ao486	yes	yes			4G	4G	Y				2014	2014	x86 data sheets	complete 486, SoC configuration	non-SoC, no MMU
ao486	ao486	beta	Aleksander Osman	x86	32	8x	arria-2	James Br	syntax errors		A				##	q13.1	1.00	1.0		system ve	85	ao486	yes	yes			4G	4G	Y				2014	2014	x86 data sheets	complete 486, SoC configuration	non-SoC, no MMU
ao486	ao486	beta	Aleksander Osman	x86	32	8x	kintex-7-3	James Br	syntax errors		6				##	14.7	1.00	1.0		system ve	85	ao486	yes	yes			4G	4G	Y				2014	2014	x86 data sheets	complete 486, SoC configuration	non-SoC, no MMU
altium/TSK80x		proprietar	Altium	Z80	8	8x	cyclone-2	Altium		2568	4			50			0.33	3.0	2.1	not avail			yes	yes	N	N	64K	64K	Y				2004		CR0140.PDF	asm, C, C++, schem, VHDL & Verilog	default clock speed is 50MHz
altium/TSK80x		proprietar	Altium	Z80	8	8x	spartan-3-5	Altium		2558	4			50			0.33	3.0	2.2	not avail			yes	yes	N	N	64K	64K	Y				2004		CR0140.PDF	asm, C, C++, schem, VHDL & Verilog	default clock speed is 50MHz
nextz80	NextZ80	stable	Nicolae Dumitrache	Z80	8	8x	kintex-7-3	James Brakefiel		1064	6			106	##	14.7	0.33	3.0	10.9	verilog	3	NextZ80CP	yes	yes	N	N	64K	64K	Y				2011	2014	z80 data sheets		
socz80		stable	Will Sowerbutts	Z80	8	8x	spartan-6-3	James Br	const	2568	6		15	93	##	14.7	0.33	3.0	4.0	vhdl	25	top_level	yes	yes	N	N	64K	64K	Y				2013	2014	z80 data sheets	based on Daniel Wallner's T80, for Pa	http://sowerbutts.com/socz80/
socz80		stable	Will Sowerbutts	Z80	8	8x	kintex-7-3	James Br	source uses S		6		8		##	14.7	0.33	3.0		vhdl	25	top_level	yes	yes	N	N	64K	64K	Y				2013	2014	z80 data sheets	based on Daniel Wallner's T80, for Pa	http://sowerbutts.com/socz80/
t80	T80 cpu	stable	Daniel Wallner	Z80	8	8x	spartan-3-5	James Br	Z80 m	1991	4			54	##	14.7	0.33	3.0	3.0	vhdl	5	T80a	yes	yes	N	N	64K	64K	Y				2002	2011	z80 data sheets	Z80, 8080 & gameboy inst sets, several usages	
t80	T80 cpu	stable	Daniel Wallner	Z80	8	8x	spartan-6-3	James Br	Z80 m	1462	6			83	##	14.7	0.33	3.0	6.2	vhdl	5	T80a	yes	yes	N	N	64K	64K	Y				2002	2011	z80 data sheets	Z80, 8080 & gameboy inst sets, several usages	
t80	T80 cpu	stable	Daniel Wallner	Z80	8	8x	kintex-7-3	James Br	Z80 m	1389	6			163	##	14.7	0.33	3.0	12.9	vhdl	5	T80a	yes	yes	N	N	64K	64K	Y				2002	2011	z80 data sheets	Z80, 8080 & gameboy inst sets, several usages	
tv80	TV80	mature	Guy Hutchison, Howar	Z80	8	8x	cyclone-2	James Brakefiel		2148	4			63	##	q11.1s	0.33	3.0	3.2	verilog	6	tv80n	yes	yes	N	N	64K	64K	Y				2004	2012	z80 data sheets	derived from Daniel Wallner's T80, ASIC implementations	
tv80	TV80	mature	Guy Hutchison, Howar	Z80	8	8x	cyclone-4	James Brakefiel		2193	4			86	##	q13.1	0.33	3.0	4.3	verilog	6	tv80n	yes	yes	N	N	64K	64K	Y				2004	2012	z80 data sheets	derived from Daniel Wallner's T80, ASIC implementations	
tv80	TV80	mature	Guy Hutchison, Howar	Z80	8	8x	arria-2	James Brakefiel		1413	A			139	##	q13.1	0.33	3.0	10.9	verilog	6	tv80n	yes	yes	N	N	64K	64K	Y				2004	2012	z80 data sheets	derived from Daniel Wallner's T80, ASIC implementations	
tv80	TV80	mature	Guy Hutchison, Howar	Z80	8	8x	spartan-3-5	James Brakefiel		2095	4			54	##	14.7	0.33	3.0	2.9	verilog	6	tv80n	yes	yes	N	N	64K	64K	Y				2004	2012	z80 data sheets	derived from Daniel Wallner's T80, ASIC implementations	
tv80	TV80	mature	Guy Hutchison, Howar	Z80	8	8x	spartan-6-3	James Brakefiel		1180	6			83	##	14.7	0.33	3.0	7.8	verilog	6	tv80n	yes	yes	N	N	64K	64K	Y				2004	2012	z80 data sheets	derived from Daniel Wallner's T80, ASIC implementations	
tv80	TV80	mature	Guy Hutchison, Howar	Z80	8	8x	kintex-7-3	James Brakefiel		1207	6			182	##	14.7	0.33	3.0	16.6	verilog	6	tv80n	yes	yes	N	N	64K	64K	Y				2004	2012	z80 data sheets	derived from Daniel Wallner's T80, ASIC implementations	
wb_z80	Wishbone High I	stable	Brewster Porcella	Z80	8	8x	kintex-7-3	James Brakefiel		2025	6			144	##	14.7	0.33	3.0	7.8	verilog	4	z80_core_t	yes	yes	N	N	64K	64K	Y				2004	2012	z80 data sheets	derived from Guy Hutchison TV80	
y80e	Y80e Z80/Z180 c	stable	Sergey Belyashov	Z80	8	8x	kintex-7-3	James Br	empty projec		6					14.7	1.00	3.0		verilog	15	y80_top	yes	yes	N	N	64K	64K	Y				2013	2013	z80 data sheets	based on Y80 from "Microprocessor Design Using Verilog HDL" by Mont	

z80soc	Z80 System on C	stable	Ronivon Costa	Z80	8	8x	cyclone-3	James Brakefiel	2831	4		22	82	##	q13.1	0.33	3.0	3.2	vhdl	19	top_de1	yes	yes	N	N	64K	64K	Y				2008	2010	z80 data sheets	based on Daniel Wallner's T80	removed pin assignments
z80soc	Z80 System on C	stable	Ronivon Costa	Z80	8	8x	spartan-3e-	James Brakefiel	2474	4	2	19	78	##	14.7	0.33	3.0	3.4	vhdl	19	top_s3e	yes	yes	N	N	64K	64K	Y				2008	2010	z80 data sheets	based on Daniel Wallner's T80	

0 # usable(beta, stable or mature): "A"(clones) & "W"(originals) 6 # # # # adrs

6 "B" or "X" of limited interest **171 unique usable designs**

Web page DMIPS per clock cycle per core en.wikipedia.org/wiki/Instructions_pe community.freescale.c www.eembc.org/coremark/index.php

MIPS/MHz Pro-rating for data size:

1-bit 0.04
8-bit 0.33
16-bit 0.67
32-bit 1.00

Under the assumption that the core is capable of one instuction per clock

Silicon Area equivalents

LUTS/DSP48 16:1
LUTS/Block RAM 32:1

Following has DMIPS per clock for many microprocessors
http://en.wikipedia.org/wiki/Instructions_per_second

uP	MIPS		/MHz	CoreMarks MHz		guessed average clocks/inst
4004	0.10					
6502	0.50		0.02	0.06		4
8051	0	DMIPS	0.08	0.24		1, 4 or 6
8080	0.17			0.25		9
68K	0.10			0.15		4
ARM Cortex A9	2.50	DMIPS		2.90	1000	
ARM Cortex M0	0.90	DMIPS		1.50	70	
ARM Cortex M3	1.25	DMIPS		2.17	25	
ARM7	0.90		0.74	2.04	600	
AVR	1.00		0.21	0.53	8	
AVR32				1.62	60	
BA21				2.44	400	
Coldfire				2.80	400	
Coldfire				0.77	150	Virtex-5 2
HCS08			0.04	0.12		4
HC11						4
LEON3/Spartan-6				1.96	100	
MC6809	1.24		0.07	1.86		3
MicroBlaze 3-stage	1.03			1.50		
MicroBlaze 5-stage	1.38			1.90	125	
MIPS32	1.51			2.28		
MSP430			0.40	1.20		2
MSP430				1.10	25	2
Nios II	0.64	DMIPS		0.93	200	
Nios II -e	0.15	DMIPS		0.25		
Nios II -f	1.13	DMIPS		1.60	200	
PIC16	0.25					
PIC18				0.04	40	
PIC24			0.72	1.86	40	
PIC32				3.45	80	
Super H-2				1.44	180	
VAX780	1.00	DMIPS		1.50		DMIPS # is by definition
Z80	1.60		0.01	0.03		3
eSi-1600				1.98		

Column Titles	Details
"A"	A: 1st choice clone, B: 2nd choice clone, W: 1st choice original, X: 2nd choice original
"B"	used to indicate best KIPS/LUT for a given design, usually using fast FPGA family
_uP_cores_test folder	if opencores design is their folder name, otherwise my folder name
opencores name	
status	ASIC, planning, alpha, beta, stable, mature, proprietary
author	First Name, Last Name
style / clone	part number or "forth", RISC, accumulator, etc
data size	data memory word size
inst size	instruction size
FPGA	FPGA family for compile, place, route & timing, usually using fastest part grade
reporter	First Name, Last Name
comments	compile, place, route & timing problems
LUTs ALM	4-LUT, 6-LUT, Altera ALM, Actel Tile
LUT?	total number of LUTs or ALMs used including route-thrus & otherwise unavailable
mults	total number of multipliers/DSPs used; 9x9 multiplier counts divided by two and rounded up
blk RAM	total # of block RAMs used, Xilinx half block RAM counts divided by two and rounded up, Altera count is percent used times # avail
Fmax	maximum primary clock speed from compile, place, route & timing run
date	date of compile, place & route; serves to identify source version
tool ver	Altera, Xilinx, Lattice Semiconductor or MicroSemi tool version number
MIPS /clk	prorated DMIPS per clock, reduced for data word sizes under 32-bits, greater than one for multiple issue processors
clks/ inst	number of clocks per instruction, typically 1.0 for modern pipelined processors, subjective for older uP
KIPS /LUT	figure of merit, does not include effects of memory capacity, floating point or instruction set quality
src code	VHDL or Verilog or System Verilog or schematic or gates
# src files	number of source files for compile, place, route & timing
top file	top file for compile, place, route & timing run
doc	is documentation provided
tool chain	is there a compiler or assembler provided or available
fltg pt	does the compile, place, route & timing run include floating point
Ha vd	separate instruction and data memory(s), there can be more than one data memory, M for MMU & caches
max data	maximum data address
max inst	maximum instruction address
byte adrs	is byte addressing provided
# inst	number of unique instructions, somewhat subjective
# reg	number of registers in register file
pipe len	number of pipeline stages
start year	year of first design activity
last revis	last year for revisions
reference	web address or generic information (for clones)
note worthy	anything special about the design
comments	catchall