ROIS24_24min processor

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Summary:

Supports 32-16M 24-bit word merged instruction/data RAM
Single word data instructions to/from data register file
Return address posted to register file. A return address stack or a C frame stack implemented via software.
Parameterization: instruction address size (6-32), register file size (16-64) and word size (24-32).

Register file dominated ISA:

`xxxxxx dddddd rrrrrr ssssss:` two source registers and one destination register
ADD, SUB, ADC, SBC, AND, ANDC, OR, XOR, LD, ST, CALL, JMPCC

`xxxxxx dddddd rrrrrr nnnnnn:` one unsigned immediate, one source register & one destination register
ADDI, SUBI, ADCI, SBCI, ANDI, ANDCI, ORI, XORI, LDN, STN, IN, OUT, CALLN, JMPCCN

`xxxxxx dddddd snnnnn nnnnnn:` one signed immediate & one destination/condition code register
LDI, BRCC, CALLR

`xxxxxx nnnnnn nnnnnn nnnnnn:` one unsigned immediate
PFX

Condition codes: A/NOP, Z/NZ, CS/CC, MI/PL, VS/VC, LE/GT, GE/LT, LS/HI,
OD/EV, 1/N1, M1/NM1, NM2/NM2, 01/NO1, 0M1/N0M1, 01M1/N01M1, 01M12/N01M12:
Twice as many condition codes provide the ability to test for even/odd, 1, -1 and -2. Test for max/min floating point exponent/mantissa also possible but not implemented.

Implementation:

6-LUTs:		min	max	Current	Form
Instructions: 1024x12 single port block RAM					
PC: 6 to 24 bit register with N, register file and PC+1inputs		06	24	09	Dff+LUT
DM (register file): quad port LUT RAM		48	96	48	64x4
Condition code		08	08	08	Dff+LUTs
Inst decode		30	30	30	LUT
Adders (2PC6-24, 2ALU24)		60	96	66	LUT
MUXing (2 each 4:1 for PC6-24, 1 for ALU24)		36	72	42	LUT
LUT Totals (estimate):		188	326	299	LUT
Actual LUT count	Kintex-7-3, speed mode, 182MHz			461	6-LUT
Actual LUT count	Kintex-7-3, area mode, 170MHz			384	6-LUT

Comments:

Multiply and divide not implemented. Floating-point not implemented. Rotates and shifts normally via multiply immediate. Source code uses inferred LUT/block RAM. See the “constants.vhd” file for op-code and condition code allocations.