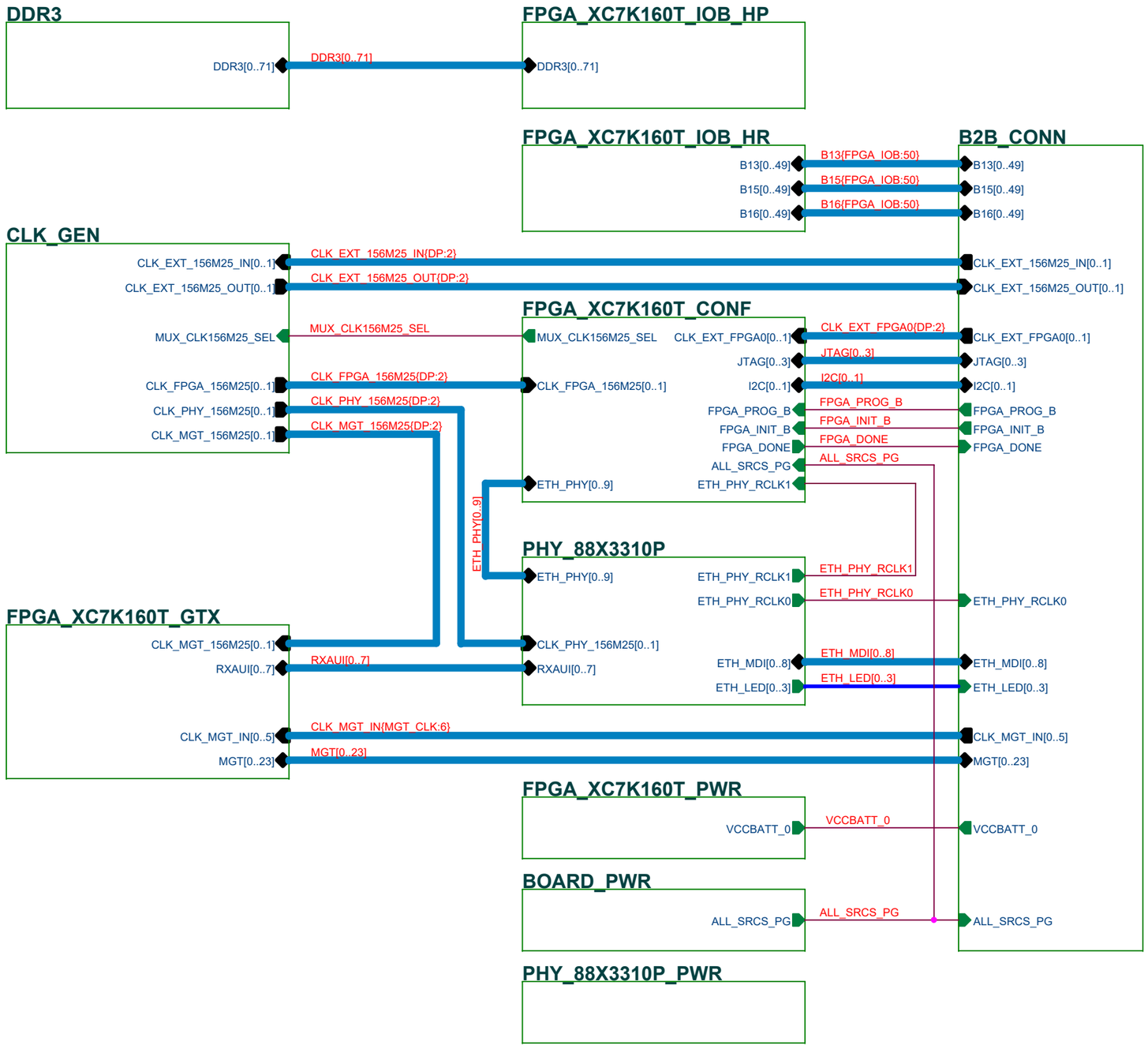
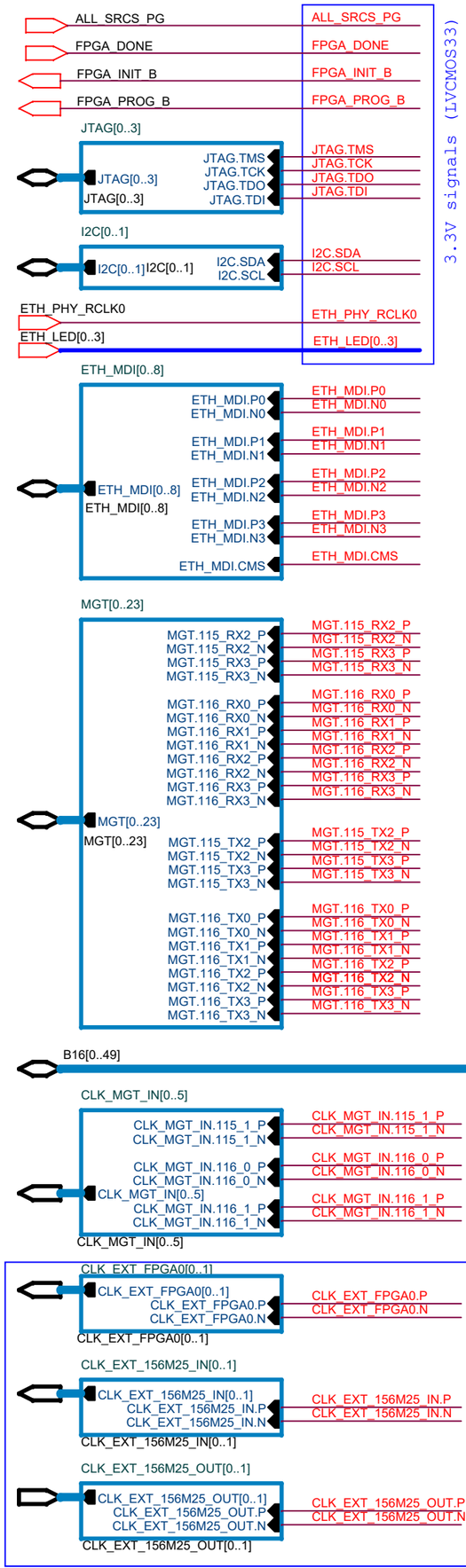


DFC Design, s.r.o.
Strmá 3001/11B, 616 00, Brno, Czech Republic

Title	Xenie Xenie	
Size A3	Document Name XENIE_TOP Designer: Kucera S.	Rev 1.0
Date: 10/25/16 10:43:59	Sheet 1 of 12	



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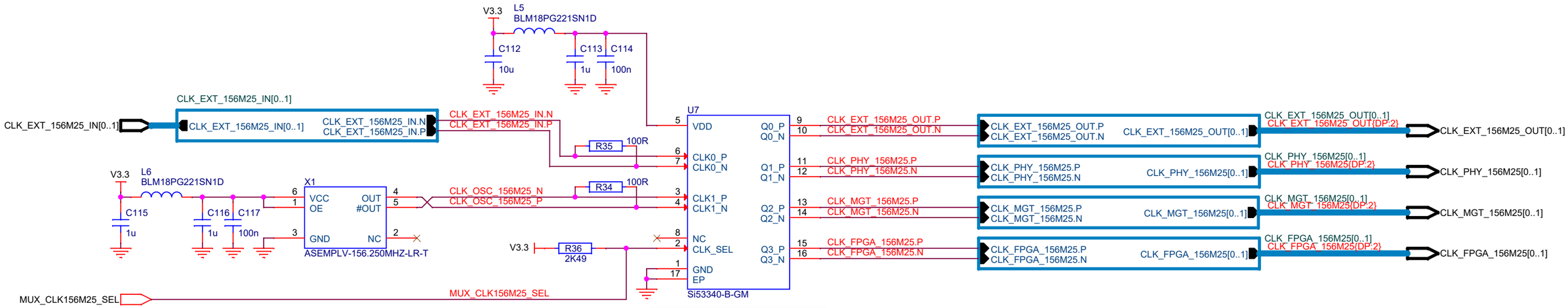
Title	Xenie Xenie	
Size: A3	Document Name: B2B_CONN Designer: Kucera S.	Rev: 1.0
Date: 10/25/16 10:43:59	Sheet 2 of 12	



Input MUX	
CLK_SEL	Q[0:3]
L	CLK0
H (def.)	CLK1

DFC Design, s.r.o.
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Title	Xenie Xenie	
Size: A3	Document Name: CLK_GEN Designer: Kucera S.	Rev: 1.0
Date: 10/25/16 10:43:59	Sheet 3 of 12	

V3.3
R95
330R
D1
Green
Q1
PDTC143ZM
JTAG[0..3]
JTAG[0..3]
JTAG[0..3]
JTAG.TMS
JTAG.TCK
JTAG.TDO
JTAG.TDI
V3.3
R38
R39
R40
4K99
4K99
4K99
U1I
N8 TMS_0
L8 TCK_0
R7 TDO_0
R6 TDI_0
QSPI.CLK
R41
33R
C8 CCLK_0
T5 M0_0
T2 M1_0
P5 M2_0
V3.3
FPGA_DONE
FPGA_INIT_B
FPGA_PROG_B
J7 DONE_0
G7 INIT_B_0
P6 PROGRAM_B_0
P7 CFGBVS_0
V3.3
N12 VP_0
P11 VN_0
P12 VREFP_0
N11 VREFN_0
R12 DXP_0
R11 DXN_0
XC7K160T-xFFG676C
Config. mode:
Master SPI (x4)
V3.3 V3.3 V3.3
R44 R46 R47
330R 4K99 4K99
FPGA_DONE
FPGA_INIT_B
FPGA_PROG_B
V3.3
R48 R49 R50
4K99
4K99
4K99
V3.3
C135
10u
C136
100n
U6
8 VCC
4 VSS
CS# 1
SCK 6
SI/IO0 5
SO/IO1 2
WP#/IO2 3
HOLD#/IO3 7
S25FL256SAGNFI001
QSPI.CSn
QSPI.CLK
QSPI.D0
QSPI.D1
QSPI.D2
QSPI.D3
QSPI.D0
QSPI.D1
QSPI.D2
QSPI.D3
U1C
K21 IO_0_14
B24 IO_L1P_T0_D00_MOSI_14
A25 IO_L1N_T0_D01_DIN_14
B22 IO_L2P_T0_D02_14
A22 IO_L2N_T0_D03_14
B25 IO_L3P_T0_DQS_PUDC_B_14
B26 IO_L3N_T0_DQS_EMCCLK_14
A23 IO_L4P_T0_D04_14
A24 IO_L4N_T0_D05_14
D26 IO_L5P_T0_D06_14
C26 IO_L5N_T0_D07_14
C23 IO_L6P_T0_FCS_B_14
C24 IO_L6N_T0_D08_VREF_14
D21 IO_L7P_T1_D09_14
C22 IO_L7N_T1_D10_14
B20 IO_L8P_T1_D11_14
A20 IO_L8N_T1_D12_14
E21 IO_L9P_T1_DQS_14
E22 IO_L9N_T1_DQS_D13_14
C21 IO_L10P_T1_D14_14
B21 IO_L10N_T1_D15_14
D23 IO_L11P_T1_SRCC_14
D24 IO_L11N_T1_SRCC_14
F22 IO_L12P_T1_MRCC_14
E23 IO_L12N_T1_MRCC_14
G22 IO_L13P_T2_MRCC_14
F23 IO_L13N_T2_MRCC_14
G24 IO_L14P_T2_SRCC_14
F24 IO_L14N_T2_SRCC_14
E25 IO_L15P_T2_DQS_RDWR_B_14
D25 IO_L15N_T2_DQS_DOUT_CSO_B_14
G25 IO_L16P_T2_CSI_B_14
G26 IO_L16N_T2_A15_D31_14
F25 IO_L17P_T2_A14_D30_14
E26 IO_L17N_T2_A13_D29_14
J26 IO_L18P_T2_A12_D28_14
H26 IO_L18N_T2_A11_D27_14
H21 IO_L19P_T3_A10_D26_14
G21 IO_L19N_T3_A09_D25_VREF_14
H23 IO_L20P_T3_A08_D24_14
H24 IO_L20N_T3_A07_D23_14
J21 IO_L21P_T3_DQS_14
H22 IO_L21N_T3_DQS_A06_D22_14
J24 IO_L22P_T3_A05_D21_14
J25 IO_L22N_T3_A04_D20_14
L22 IO_L23P_T3_A03_D19_14
K22 IO_L23N_T3_A02_D18_14
K23 IO_L24P_T3_A01_D17_14
J23 IO_L24N_T3_A00_D16_14
L23 IO_25_14
XC7K160T-xFFG676C
PUDC_B
V3.3
R54
330R
R100
DNP
Pull-Up During Configuration:
DISABLED
ETH_PHY[0..9]
ETH_PHY[0..9]
ETH_PHY.GPIO[0..5]
ETH_PHY.MDC
ETH_PHY.INTN
ETH_PHY.MDIO
ETH_PHY.RESETN
ETH_PHY.GPIO[0..5]
ETH_PHY.MDC
ETH_PHY.INTn
ETH_PHY.MDIO
ETH_PHY.RESETn
ETH_PHY.GPIO2
ETH_PHY.GPIO4
ETH_PHY.GPIO1
LED1
ETH_PHY.GPIO3
QSPI.CSn
ETH_PHY.GPIO0
ETH_PHY.MDC
ETH_PHY.GPIO5
ETH_PHY.INTn
ETH_PHY.MDIO
MUX_CLK156M25_SEL
ETH_PHY.RESETn
MUX_CLK156M25_SEL
MUX_CLK156M25_SEL
CLK_EXT_FPGA0[0..1]
CLK_EXT_FPGA0[0..1]
CLK_EXT_FPGA0.P
CLK_EXT_FPGA0.N
R106
100R
CLK_EXT_FPGA0.P
CLK_EXT_FPGA0.N
CLK_FPGA_156M25.N
CLK_FPGA_156M25.P
CLK_FPGA_156M25[0..1]
CLK_FPGA_156M25[0..1]
CLK_FPGA_156M25.N
CLK_FPGA_156M25.P
R107
100R
ETH_PHY_RCLK1
ETH_PHY_RCLK1
ETH_PHY_RCLK1
ALL_SRCS_PG
ALL_SRCS_PG
ALL_SRCS_PG
I2C.SDA
I2C.SCL
LED0
D3
Red
V3.3
R108
330R
LED1
User LEDs
D4
Red
V3.3
R109
330R
LED0
I2C[0..1]
I2C[0..1]
I2C.SDA
I2C.SCL
I2C.SDA
I2C.SCL
V3.3
R98
R99
4K99
4K99
U8
6 VCC
4 A1
5 A0
3 SDA
1 SCL
2 VSS
24AA025E48T-I/OT
V3.3
C360
100n
EUI-48 EEPROM I2C Address:
"1010000" 50hex

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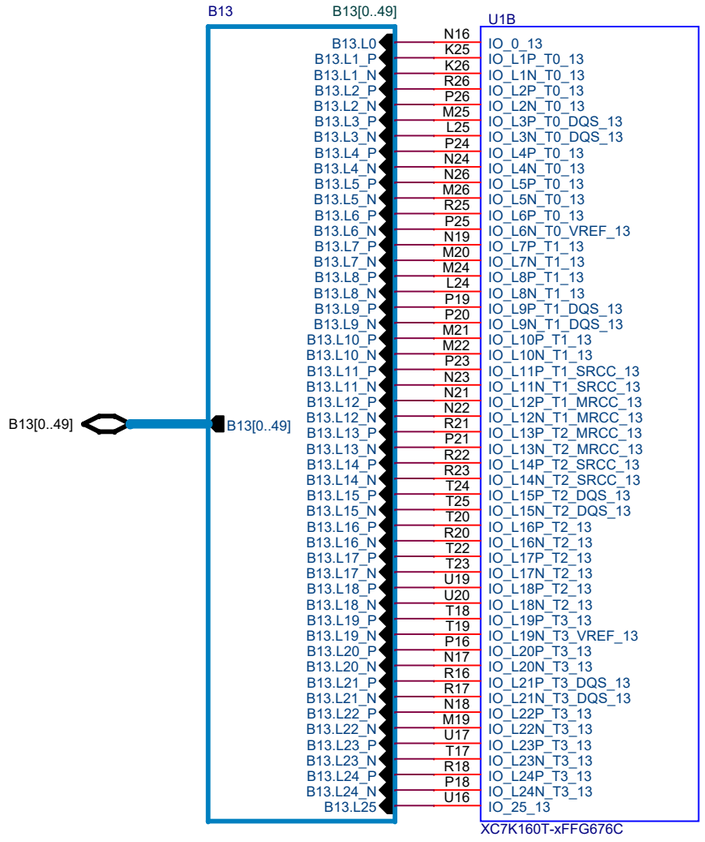
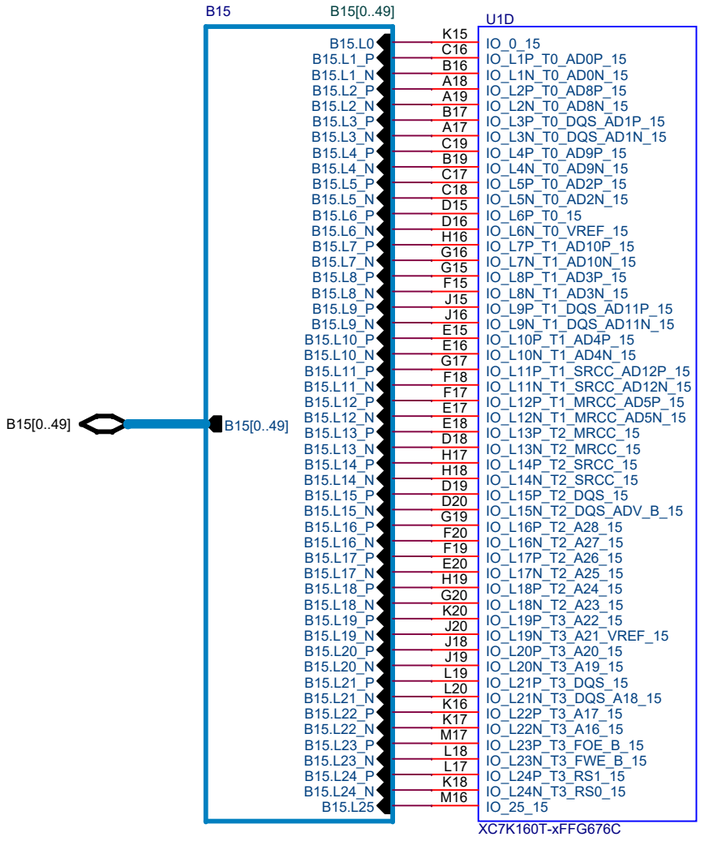
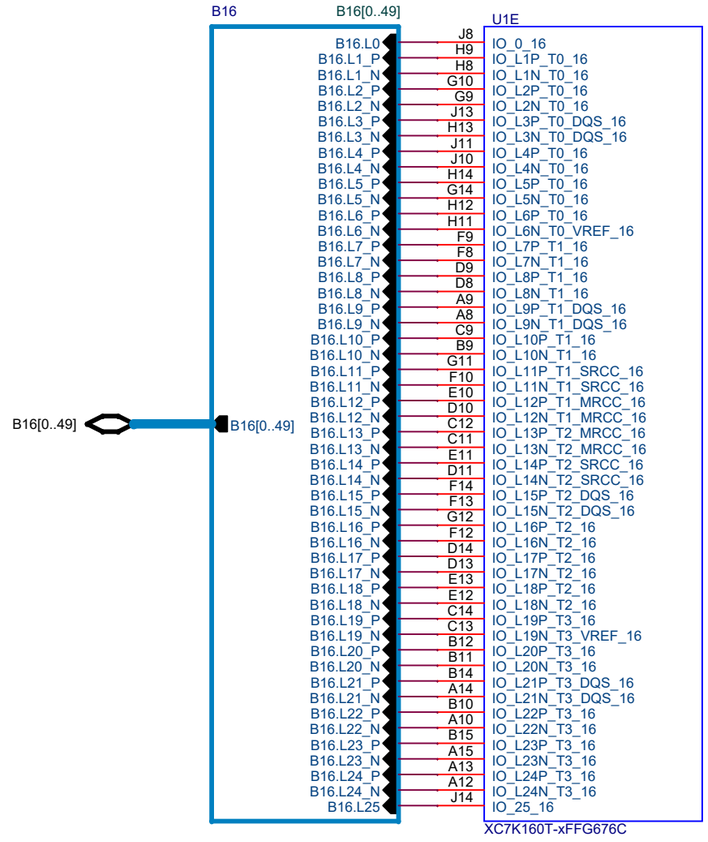
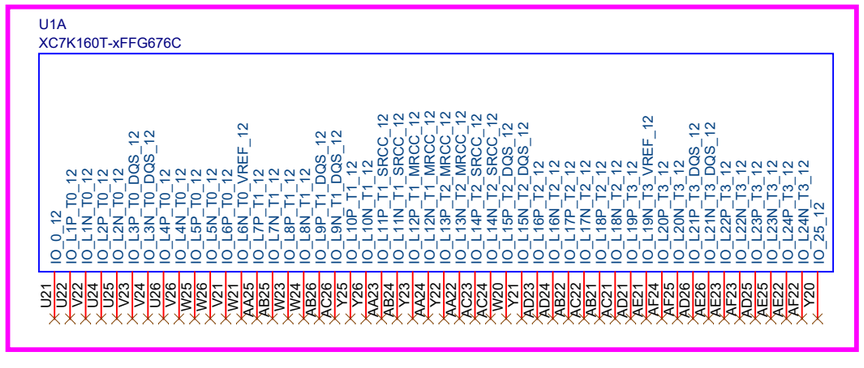
Title	Xenie Xenie	
Size A3	Document Name FPGA_XC7K160T_CONF	Rev 1.0
	Designer: Kucera S.	
Date: 10/25/16 10:43:59	Sheet 4 of 12	







XC7K70T:
IOB12 NOT CONNECTED



DFC Design, s.r.o.
Strmá 3001/11B, 616 00, Brno, Czech Republic

Title	Xenie Xenie	
Size A3	Document Name FPGA_XC7K160T_IOB_HR Designer: Kucera S.	Rev 1.0
Date: 10/25/16 10:43:59	Sheet 5 of 12	

DDR3_VDD
R57 100R
U1G
XC7K160T-xFFG676C
IO_0_VRN_33 U9
IO_L1P_T0_33 V11
IO_L1N_T0_33 W11
IO_L2P_T0_33 V8
IO_L2N_T0_33 V7
IO_L3P_T0_DQS_33 W10
IO_L3N_T0_DQS_33 W9
IO_L4P_T0_33 Y8
IO_L4N_T0_33 Y7
IO_L5P_T0_33 Y11
IO_L5N_T0_33 Y10
IO_L6P_T0_33 V9
IO_L6N_T0_VREF_33 W8
IO_L7P_T1_33 DDR3.CLK_P AE7
IO_L7N_T1_33 DDR3.CLK_N AF7
IO_L8P_T1_33 DDR3.A2 AA8
IO_L8N_T1_33 DDR3.A5 AA7
IO_L9P_T1_DQS_33 DDR3.A10 AC8
IO_L9N_T1_DQS_33 DDR3.CASn AD8
IO_L10P_T1_33 DDR3.CKE AB7
IO_L10N_T1_33 DDR3.RASn AC7
IO_L11P_T1_SRCC_33 DDR3.A1 AA9
IO_L11N_T1_SRCC_33 DDR3.BA1 AB9
IO_L12P_T1_MRCC_33 DDR3.A15 AC9
IO_L12N_T1_MRCC_33 DDR3.CSn AD9
IO_L13P_T2_MRCC_33 AB11
IO_L13N_T2_MRCC_33 AC11
IO_L14P_T2_SRCC_33 AA10
IO_L14N_T2_SRCC_33 AB10
IO_L15P_T2_DQS_33 AB12
IO_L15N_T2_DQS_33 DDR3.A14 AC12
IO_L16P_T2_33 AA13
IO_L16N_T2_33 AA12
IO_L17P_T2_33 AC13 DDR3.A8
IO_L17N_T2_33 AD13 DDR3.A11
IO_L18P_T2_33 Y13
IO_L18N_T2_33 Y12
IO_L19P_T3_33 AD11 DDR3.A9
IO_L19N_T3_VREF_33 AE11 DDR3.A12
IO_L20P_T3_33 AD10 DDR3.BA2
IO_L20N_T3_33 AE10 DDR3.A3
IO_L21P_T3_DQS_33 AE12 DDR3.A4
IO_L21N_T3_DQS_33 AF12 DDR3.A6
IO_L22P_T3_33 AE8 DDR3.ODT
IO_L22N_T3_33 AF8 DDR3.WEn
IO_L23P_T3_33 AE13 DDR3.A7
IO_L23N_T3_33 AF13 DDR3.A13
IO_L24P_T3_33 AF10 DDR3.A0
IO_L24N_T3_33 AF9 DDR3.BA0
IO_25_VRP_33 R58 100R V12

V3.3
L11 BLM18PG221SN1D
C357 1u
C358 1u
C359 100n
X2 DSC1123CI2-200.0000
VCC 6
OE 1
GND 3
OUT 4
#OUT 5
NC 2
CLK_OSC_200M.P
CLK_OSC_200M.N
R110 100R

DDR3[0..71]
DDR3.CLK_P
DDR3.CLK_N
DDR3.RASN
DDR3.CASN
DDR3.WEN
DDR3.CSN
DDR3.CKE
DDR3.ODT
DDR3.A[0..15]
DDR3.BA[0..2]
DDR3.RASn
DDR3.CASn
DDR3.WEn
DDR3.CSn
DDR3.CKE
DDR3.ODT
DDR3.A[0..15]
DDR3.BA[0..2]
DDR3.DQ[0..31]
DDR3.DM[0..3]
DDR3.DQS2_P
DDR3.DQS2_N
DDR3.DQS3_P
DDR3.DQS3_N
DDR3.RESETN
DDR3.DQS0_P
DDR3.DQS0_N
DDR3.DQS1_P
DDR3.DQS1_N
DDR3[0..71]

U1H
XC7K160T-xFFG676C
IO_0_VRN_34 U4
IO_L1P_T0_34 DDR3.DQ23 U6
IO_L1N_T0_34 DDR3.DQ20 U5
IO_L2P_T0_34 DDR3.DQ22 U2
IO_L2N_T0_34 DDR3.DQ16 U1
IO_L3P_T0_DQS_34 W6
IO_L3N_T0_DQS_34 W5
IO_L4P_T0_34 DDR3.DM2 V3
IO_L4N_T0_34 DDR3.DQ19 W3
IO_L5P_T0_34 DDR3.DQ18 U7
IO_L5N_T0_34 DDR3.DQ21 V6
IO_L6P_T0_34 DDR3.DQ17 V4
IO_L6N_T0_VREF_34 W4
IO_L7P_T1_34 DDR3.DQ26 Y3
IO_L7N_T1_34 DDR3.DM3 Y2
IO_L8P_T1_34 DDR3.DQ27 V2
IO_L8N_T1_34 DDR3.DQ29 V1
IO_L9P_T1_DQS_34 AB1
IO_L9N_T1_DQS_34 AC1
IO_L10P_T1_34 DDR3.DQ31 W1
IO_L10N_T1_34 DDR3.DQ25 Y1
IO_L11P_T1_SRCC_34 DDR3.DQ28 AB2
IO_L11N_T1_SRCC_34 DDR3.DQ30 AC2
IO_L12P_T1_MRCC_34 DDR3.DQ24 AA3
IO_L12N_T1_MRCC_34 AA2
IO_L13P_T2_MRCC_34 DDR3.DQ4 AA4
IO_L13N_T2_MRCC_34 DDR3.DQ0 AB4
IO_L14P_T2_SRCC_34 DDR3.DQ1 AC4
IO_L14N_T2_SRCC_34 DDR3.DQ7 AC3
IO_L15P_T2_DQS_34 AA5
IO_L15N_T2_DQS_34 AB5
IO_L16P_T2_34 AB6
IO_L16N_T2_34 DDR3.DQ5 AC6
IO_L17P_T2_34 DDR3.DQ6 Y6
IO_L17N_T2_34 DDR3.DQ2 Y5
IO_L18P_T2_34 DDR3.DQ3 AD6
IO_L18N_T2_34 DDR3.DM0 AD5
IO_L19P_T3_34 DDR3.DQ13 AD4
AD3
IO_L19N_T3_VREF_34 DDR3.DQ11 AD1
IO_L20P_T3_34 DDR3.DQ15 AE1
IO_L20N_T3_34 AF5
IO_L21P_T3_DQS_34 AF4
IO_L21N_T3_DQS_34 DDR3.DM1 AE3
IO_L22P_T3_34 DDR3.DQ9 AE2
IO_L22N_T3_34 DDR3.DQ14 AE6
IO_L23P_T3_34 DDR3.DQ10 AE5
IO_L23N_T3_34 DDR3.DQ8 AF3
IO_L24P_T3_34 DDR3.DQ12 AF2
IO_L24N_T3_34 T7
IO_25_VRP_34

DDR3_VREF
C137 100n
C138 100n

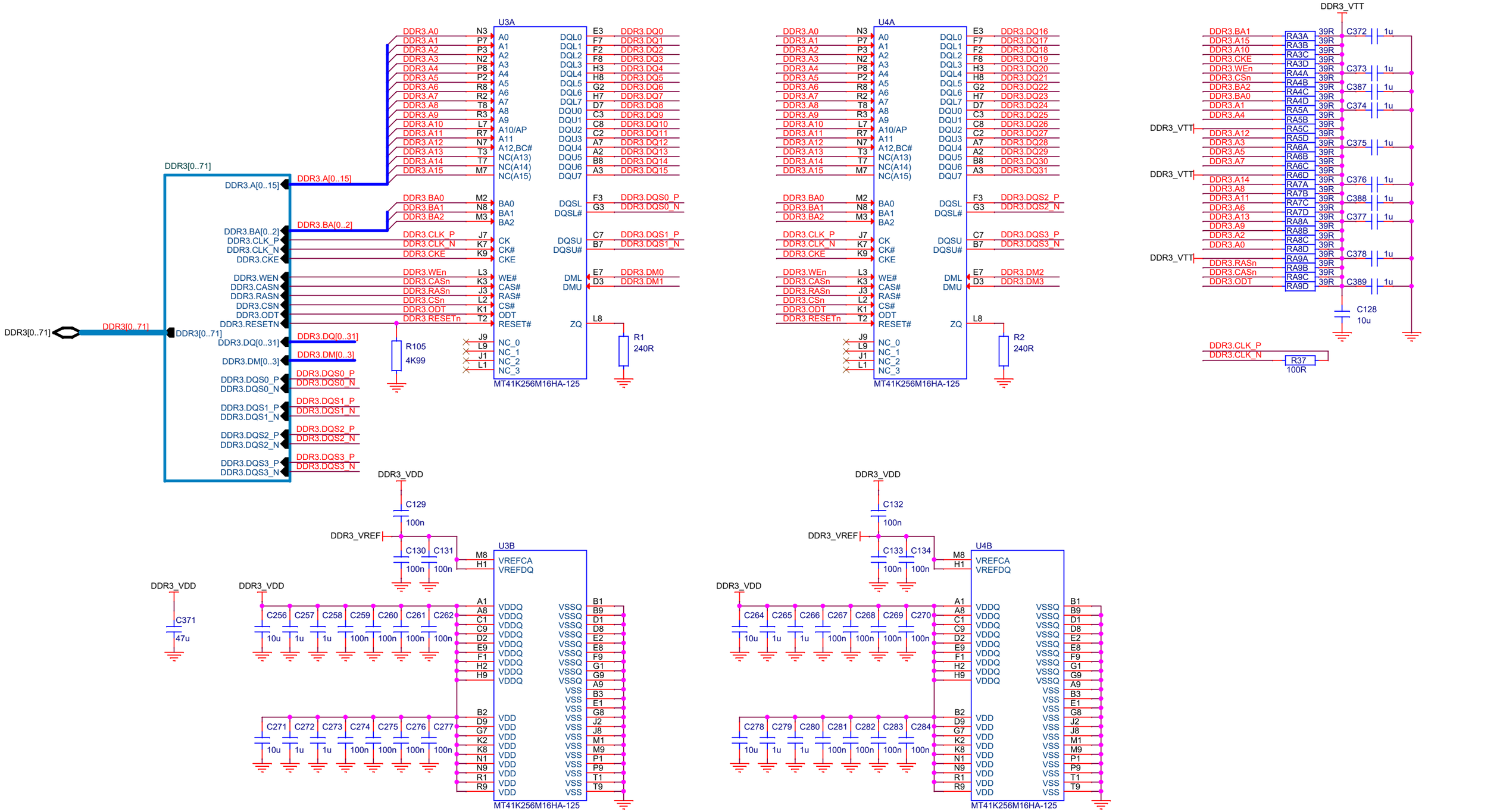
DDR3[0..71]
DDR3[0..71]
DDR3[0..71]
DDR3_VREF
DDR3_VREF

XC7K70T:
IOB32 NOT CONNECTED

U1F
XC7K160T-xFFG676C
IO_0_VRN_32 V13
IO_L1P_T0_32 AE17
IO_L1N_T0_32 AF17
IO_L2P_T0_32 AF14
IO_L2N_T0_32 AF15
IO_L3P_T0_DQS_32 AE18
IO_L3N_T0_DQS_32 AF18
IO_L4P_T0_32 AD15
IO_L4N_T0_32 AE15
IO_L5P_T0_32 AF19
IO_L5N_T0_32 AF20
IO_L6P_T0_32 AD16
IO_L6N_T0_VREF_32 AE16
IO_L7P_T1_32 AA14
IO_L7N_T1_32 AA15
IO_L8P_T1_32 AC14
IO_L8N_T1_32 AD14
IO_L9P_T1_DQS_32 Y15
IO_L9N_T1_DQS_32 Y16
IO_L10P_T1_32 AB14
IO_L10N_T1_32 AB15
IO_L11P_T1_SRCC_32 AA17
IO_L11N_T1_SRCC_32 AA18
IO_L12P_T1_MRCC_32 AB16
IO_L12N_T1_MRCC_32 AC16
IO_L13P_T2_MRCC_32 AC18
IO_L13N_T2_MRCC_32 AD18
IO_L14P_T2_SRCC_32 AB17
IO_L14N_T2_SRCC_32 AC17
IO_L15P_T2_DQS_32 AD20
IO_L15N_T2_DQS_32 AE20
IO_L16P_T2_32 AA19
IO_L16N_T2_32 AA20
IO_L17P_T2_32 AC19
IO_L17N_T2_32 AD19
IO_L18P_T2_32 AB19
IO_L18N_T2_32 AB20
IO_L19P_T3_32 Y17
IO_L19N_T3_VREF_32 Y18
IO_L20P_T3_32 V16
IO_L20N_T3_32 V17
IO_L21P_T3_DQS_32 W18
IO_L21N_T3_DQS_32 W19
IO_L22P_T3_32 W15
IO_L22N_T3_32 W16
IO_L23P_T3_32 V18
IO_L23N_T3_32 V19
IO_L24P_T3_32 V14
IO_L24N_T3_32 W14
IO_25_VRP_32 W13

DFC Design, s.r.o.
Strmá 3001/11B, 616 00, Brno, Czech Republic

Title	Xenie Xenie	
Size A3	Document Name FPGA_XC7K160T_IOB_HP Designer: Kucera S.	Rev 1.0
Date: 10/25/16 10:43:59	Sheet 6 of 12	



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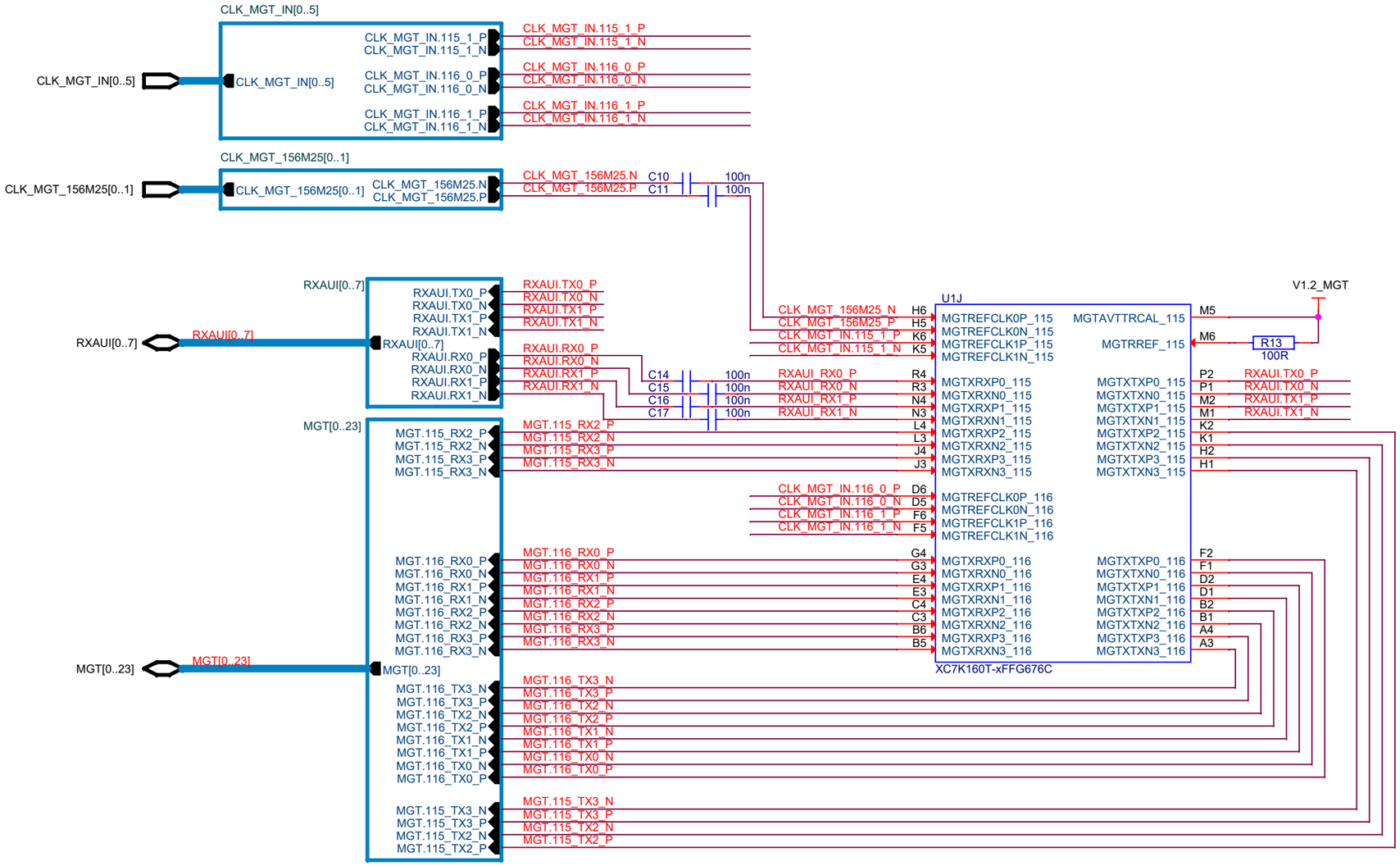
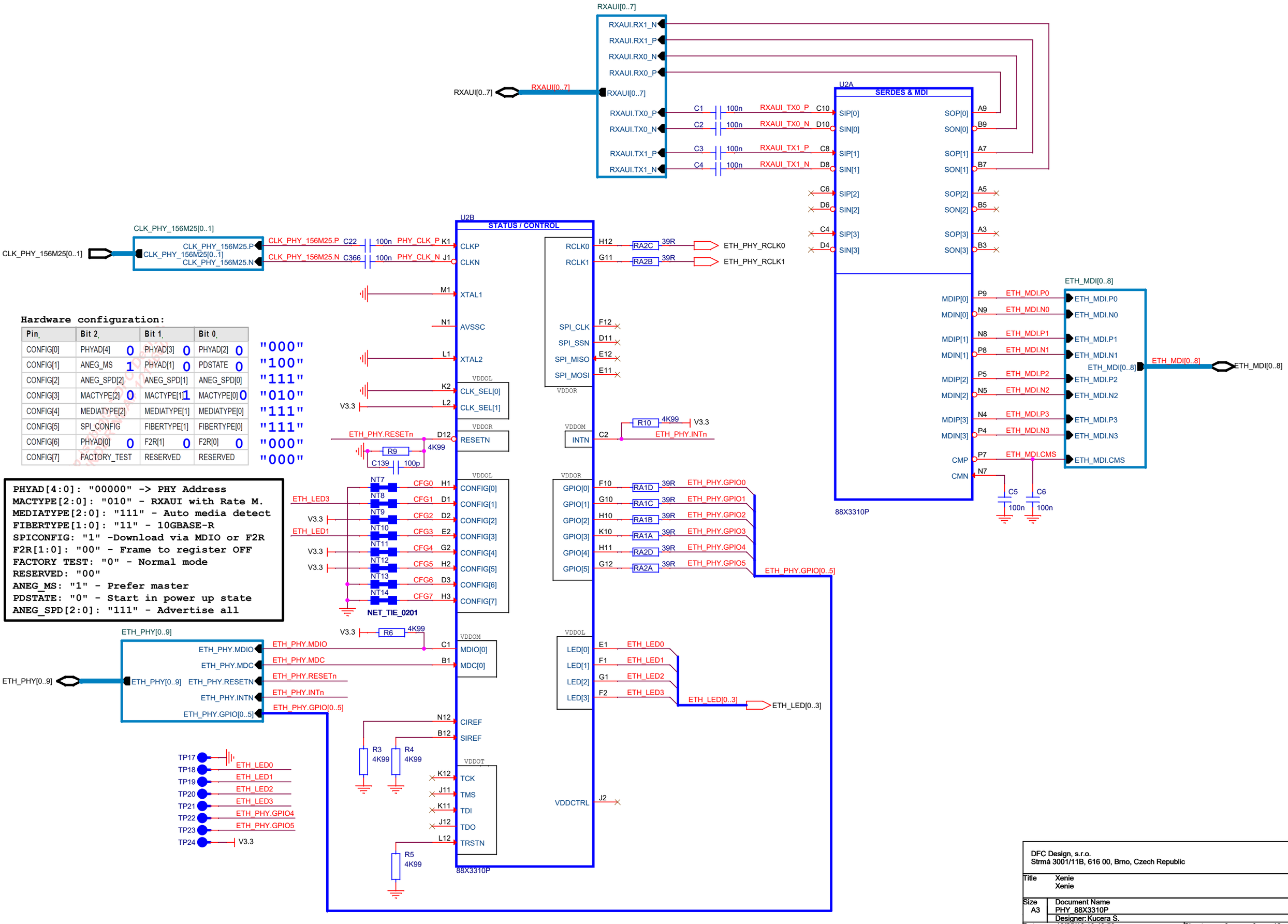
Title	Xenie Xenie		
Size A3	Document Name DDR3		Rev 1.0
	Designer: Kucera S.		
Date:	10/25/16 10:43:59	Sheet 7 of 12	



DFC Design, s.r.o. Strmá 3001/11B, 616 00, Brno, Czech Republic		
Title	Xenie Xenie	
Size A3	Document Name FPGA_XC7K160T_GTX Designer: Kucera S.	Rev 1.0
Date: 10/25/16 10:43:59	Sheet 8 of 12	



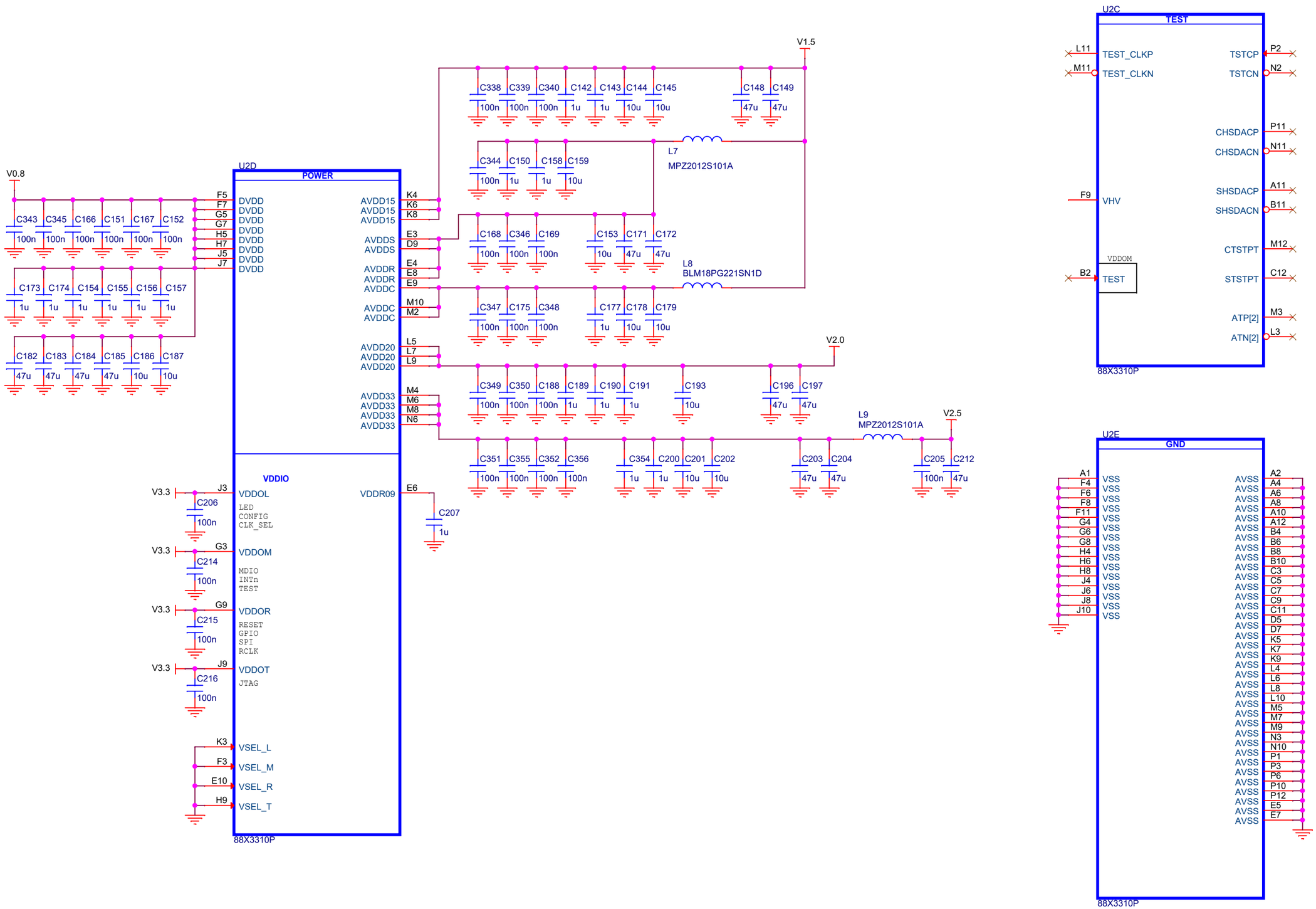
Hardware configuration:

Pin	Bit 2	Bit 1	Bit 0	
CONFIG[0]	PHYAD[4] 0	PHYAD[3] 0	PHYAD[2] 0	"000"
CONFIG[1]	ANEG_MS 1	PHYAD[1] 0	PDSTATE 0	"100"
CONFIG[2]	ANEG_SPD[2]	ANEG_SPD[1]	ANEG_SPD[0]	"111"
CONFIG[3]	MACTYPE[2] 0	MACTYPE[1] 1	MACTYPE[0] 0	"010"
CONFIG[4]	MEDIATYPE[2]	MEDIATYPE[1]	MEDIATYPE[0]	"111"
CONFIG[5]	SPI_CONFIG	FIBERTYPE[1]	FIBERTYPE[0]	"111"
CONFIG[6]	PHYAD[0] 0	F2R[1] 0	F2R[0] 0	"000"
CONFIG[7]	FACTORY_TEST	RESERVED	RESERVED	"000"

```
PHYAD[4:0]: "00000" -> PHY Address
MACTYPE[2:0]: "010" - RXAUI with Rate M.
MEDIATYPE[2:0]: "111" - Auto media detect
FIBERTYPE[1:0]: "11" - 10GBASE-R
SPICONFIG: "1" -Download via MDIO or F2R
F2R[1:0]: "00" - Frame to register OFF
FACTORY TEST: "0" - Normal mode
RESERVED: "00"
ANEG_MS: "1" - Prefer master
PDSTATE: "0" - Start in power up state
ANEG_SPD[2:0]: "111" - Advertise all
```


DFC Design, s.r.o.
Strmá 3001/11B, 616 00, Brno, Czech Republic

Title	Xenie Xenie		
Size A3	Document Name PHY_88X3310P		Rev 1.0
	Designer: Kucera S.		
Date: 10/25/16 10:43:59	Sheet 9 of 12		



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Title	Xenie Xenie	
Size: A3	Document Name: PHY_88X3310P_PWR	Rev: 1.0
	Designer: Kucera S.	
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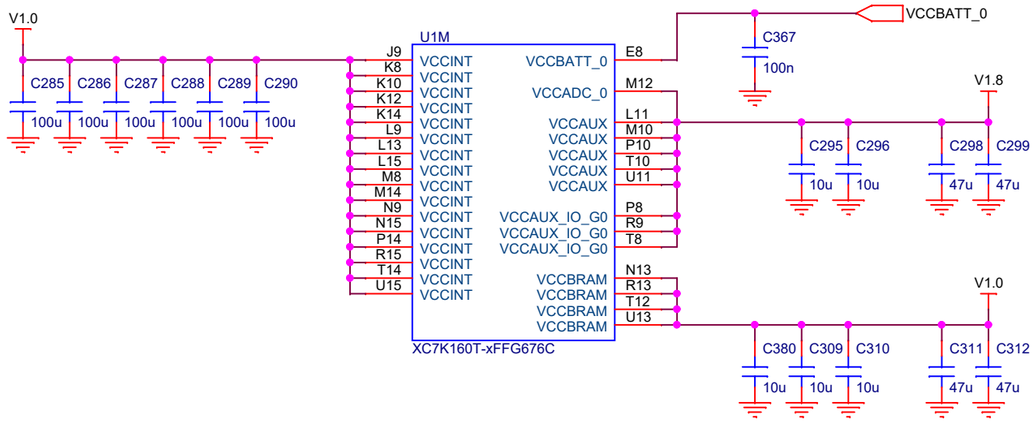

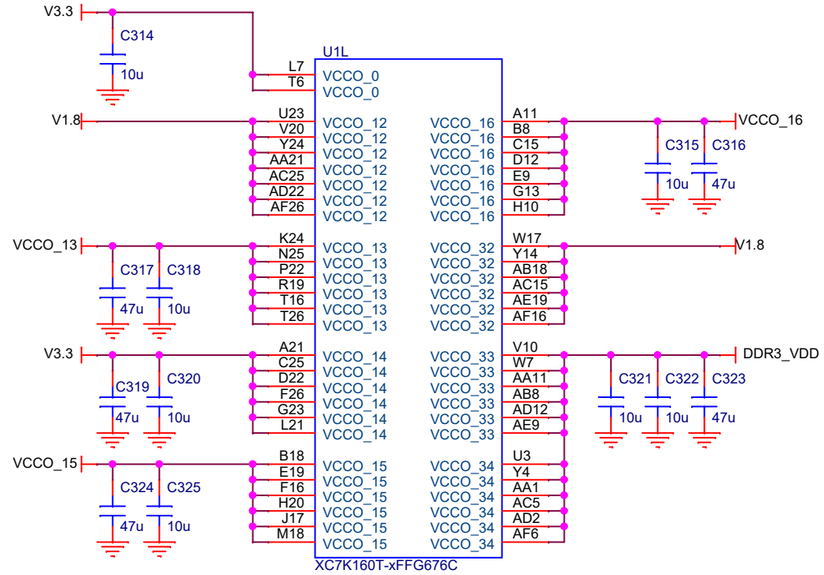

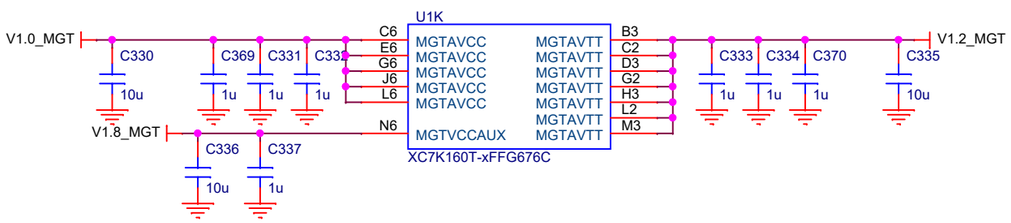

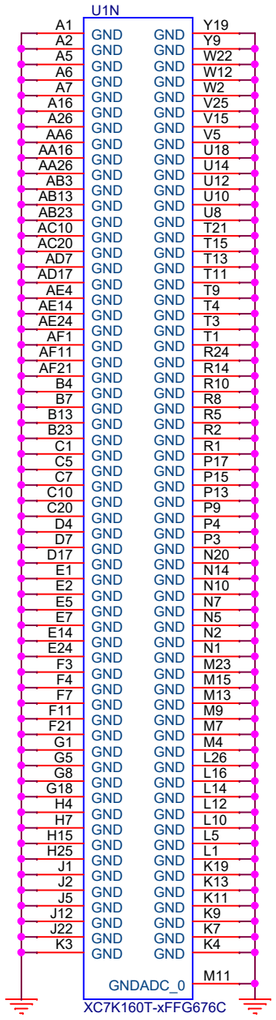

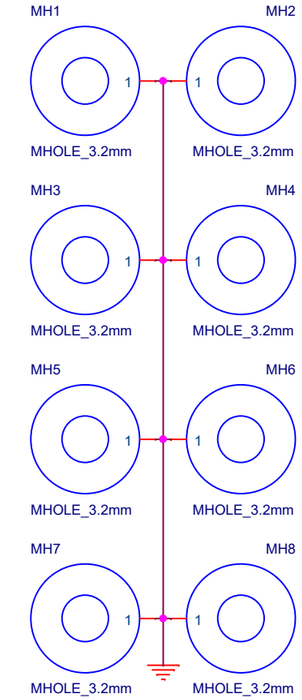

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Title	Xenie Xenie	
Size A3	Document Name FPGA_XC7K160T_PWR	Rev 1.0
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PHY 88X3310

FPGA_MGT

1.35v

U5A EN6362QI — V3.3_IN; V1.0; PG_V1.0; R87 10R; R84 300K; R86 20K5; C253 22p; R85 442K; R82 10K; C254 100n; NT15 NET_TIE_0201

U9 TPS82085 — V3.3_IN; R101 DNP; C227 22u; R65 187K; R66 150K; C228 47u; V1.8; R88 10K; PG_V1.8

U10 TPS82085 — V3.3_IN; C220 22u; R61 110K; R62 150K; C221 47u; DDR3_VDD

U11 TPS51200DRCT — V3.3_IN; C217 10u; C218 100n; ALL_SRCS_PG; DDR3_VDD; C223 10u; R63 10K; R64 10K; C226 1n; C222 10u; C219 10u; DDR3_VTT; DDR3_VREF; C368 100n

C381 10u; C382 10u; C383 1u; C384 1u; C385 100n; C386 100n

U12 TPS22965N — V3.3_IN; V3.3; C361 1n

V3.3; R94 330R; D2 Green; R102 10K; Q2 PDTC143ZM; ALL_SRCS_PG

PG_V1.8; ALL_SRCS_PG

U13 TPS82085 — V3.3_IN; C229 22u; V0.8; NT6 NET_TIE_0201; C230 47u

U16 TPS82085 — V3.3_IN; C232 22u; R68 130K; R69 150K; V1.5; C233 47u

U18 TPS82085 — V3.3_IN; C240 22u; R74 220K; R75 150K; V2.0; C241 22u

U20 TPS82085 — V3.3_IN; C247 22u; R80 316K; R81 150K; V2.5; C248 22u

U14 TPS82085 — V3.3_IN; C237 22u; R72 100K; R73 150K; V1.33; L14 MPZ2012S101A; C238 22u; C231 10u

U15 TPS74901DRC — PG_V1.0; PG_V1.0&V1.8_MGT; V3.3_IN; C235 1u; C236 1n; R70 1K2; R71 4K99; C234 22u; V1.0_MGT

R104 10K — V3.3_IN; PG_V1.0&V1.8_MGT

U17 TPS82085 — V3.3_IN; C243 22u; R78 100K; R79 110K; V1.53; L15 MPZ2012S101A; C244 22u; C239 10u

U19 TPS74901DRC — PG_V1.0&V1.8_MGT; ALL_SRCS_PG; V3.3_IN; C245 1u; C246 1n; R76 2K49; R77 4K99; C242 22u; V1.2_MGT

U21 TPS74901DRC — V3.3_IN; C362 10u; PG_V1.0; PG_V1.0&V1.8_MGT; C363 1u; C364 1n; R92 3K57; R93 2K87; C365 22u; V1.8_MGT

V0.8 TP1; V1.5 TP2; V2.0 TP3; V2.5 TP4; V1.33 TP5; V1.53 TP6; V1.0_MGT TP7; V1.2_MGT TP8; V1.8_MGT TP9; V1.0 TP10; DDR3_VDD TP11; V1.8 TP12; V3.3 TP13; DDR3_VTT TP14; DDR3_VREF TP15; TP25; TP26; TP27

U5B EN6362QI — NC1 … NC60; NC(SW); NC49(SW); NC50(SW); NC51(SW); NC52(SW); NC53; NC54; NC55; NC56

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