Opencore and other soft core processors

		_uP_all_soft folder	opencores or prmary link	status	author	style / clone	data size	inst size	FPGA	report	comment	LUTs ALUT	LUT?	mults	blk ram	F max	date	tool ver	MIPS /inst	clks/ inst	KIPS /LUT	vendor	SOC	src code	# src files	top file	doc	tool chain	fltgpt	Hav'	max data	max inst	byte adrs	# inst	adr mod	# reg	pipe len	start year	last revis	secondary web link	note worthy	comments
A	1	cosmac	https://github.co	beta	Eric Smith	1802	8	8x	kintex-7-3	James	Brakef	244	6			270	##	14.7	0.33	1.0	365.5	X		vhdl	1	cosmac	Y	asm	N	N	64K	64K	Y	100		16		2009	2018		AKA COSMAC ELF of 1976	Fmax is for bare core, runs CamelForth
A	1	cosmac	https://github.co	beta	Eric Smith	1802	8	8x	kintex-7-3	James	inferre	598	6		17	87	##	14.7	0.33	1.0	48.0	X	X	vhdl	14	elf	Y	asm	N	N	64K	64K	Y	100		16		2009	2018		uses PIXIE graphics core	modified to use block RAM
	1	mcs-4	https://opencore	alpha	Reece Pollack	4004	4	4	kintex-7-3	James	Brakef	228	6			376	##	14.7	0.16	4.0	66.0	X		verilog	7	i4004			N		4K	4K	N					2012	2012		4004 was multi-chip	4004 CPU & MCS-4
		af65k	https://github.co	alpha	Andre Fachat	6502	32	8	kintex-7-3	James	Brakef	4424	6			69	##	14.7	1.00	4.0	3.9	X		vhdl	13	gecko65k	Y		N	N								2011		http://www.6502.org	extended 6502 AKA 65K with 16, 32 or 64 bit data	
A	1	ag_6502	https://opencore	beta	Oleg Odintsov	6502	8	8x	kintex-7-3	James	Brakef	824	6			176	##	14.7	0.33	4.0	17.7	ILX		verilog	2	ag_6502		yes	N	N	64K	64K	Y					2012	2012		verilog code generation, "phase level accurate"	
		apple2fpga	http://www.cs.c	stable	Stephen A Edwards	6502	16	8	kintex-7-3	James	uncon	1417	6		9	159	##	14.7	0.33	4.0	9.2	IX	Y	vhdl	19	de2_top	Y	yes	N	Y	64K	64K	Y					2007	2009		emulation of Apple II computer	replaced Altera PLL with stub
W	1	bc6502	http://finitron.ca	beta	Robert Finch	6502	8	8x	kintex-7-3	James	Brakef	619	6			197	##	14.7	0.33	4.0	26.2	X		verilog	18	bc6502		yes	N	N	64K	64K	Y					2012	2012			bare source
		c65gs	https://github.co	missing files		6502	8	16	kintex-7-3	James	missing files		6				##	14.7	0.33	3.0		X	Y	vhdl	60	machineC	Y	yes	N		64K	64K	Y	30				2015	2018	https://github.com/g	Commodore 64 emulator	work in progress, missing files
A	1	cpu6502_true_	https://opencore	stable	Jens Gutschmidt	6502	8	8x	kintex-7-3	James	Brakef	1678	6			159	##	14.7	0.33	4.0	7.8	X		vhdl	7	r6502_tc		yes	N	N	64K	64K	Y					2008	2010		cycle accurate	
A		cpu65c02_true	https://opencore	stable	Jens Gutschmidt	6502	8	8x	spartan-6-3	James	latch v	4794	6			47	##	14.7	0.33	4.0	0.8	X		vhdl	8	core		yes	N	N	64K	64K	Y					2008	2013		cycle accurate	
		fpga-64	http://www.syn	stable	Peter Wendrich	6502	8	8	kintex-7-3	James	Brakef	2210	6		2	156	##	14.7	0.33	4.0	5.8	X	Y	vhdl	26	fpga64_c	Y	yes	N	N	64K	64K	Y			26		2005	2008		Rendition of Commodore 64	altera top level schematic
A	1	free6502	http://web.archi	stable	David Kessner	6502	8	8x	kintex-7-3	James	Brakef	646	6			193	##	14.7	0.33	4.0	24.6	X		vhdl	5	free6502	Y	yes	N	N	64K	64K	Y					1999	2000	http://www.sprow.co	microcoded	
A	1	lattice6502	https://opencore	beta	Ian Chapman	6502	8	8x	kintex-7-3	James	Brakef	4942	6			214	##	14.7	0.33	4.0	3.6	X		vhdl	3	ghdl_proc	Y	yes	N	N	64K	64K	Y					2010	2010		targeted to LCMXO2280	
B		m65	www.ip-arch.jp/	stable	Naohiko Shimizu	6502	8	8x	arria-2	James	Brakef	483	A			110	##	q13.1	0.33	4.0	18.8	X		sfl & TDF	8	m65cpu	Y	yes	N	N	4K	4K	Y					2001	2002			
A	1	m65c02	https://opencore	mature	Michael Morris	6502	8	8x	spartan-6-3	James	Brakef	466	6		3	118	##	14.7	0.33	4.0	20.8	X	Y	verilog	13	M65C02	Y	yes	N	N	64K	64K	Y					2013	2014			micro-coded via F9408 soft sequencer
		mcl65	http://www.mic	stable	Ted Fried	6502	8	8	kintex-7-3	James	insert	326	6		2	196	##	14.7	0.33	4.0	49.6	X		verilog	1	mcl65	Y	yes	N	N	64K	64K	Y					2017		6502 data sheets	microcoded, cycle exact	**excellent micro-coding LUT counts**
A	1	pet_fpga	https://github.co	stable	Thomas Skibo	6502	8	8x	kintex-7-3	James	Brakef	1052	6			242	##	14.7	0.33	4.0	19.0	X		verilog	1	cpu6502	Y	yes	N	N	64K	64K	Y					2007	2011	https://github.com/sl	for Commodore PET	
A	1	t65	https://opencore	stable	Daniel Wallner	6502	8	8x	kintex-7-3	James	Brakef	575	6			291	##	14.7	0.33	4.0	41.7	IX		vhdl	7	T65	Y	yes	N	N	64K	64K	Y					2002	2010	6502 data sheets	6502, 65C02 & 65C816; wide use	
A		t6507lp	https://opencore	beta	Gabriel Oshiro, Samuel	6502	8	8x	spartan-6-3	James	errors							14.7		4.0				verilog	22	t6507lp	Y	yes	N	N	64K	64K	Y					2009	2010	6502 data sheets	for use in ATARI 2600	
A	1	verilog_6502	https://github.co	stable	Arlet Ottens	6502	8	8	kintex-7-3	James	Brakef	407	6			200	##	14.7	0.33	4.0	40.6	X		verilog	2	cpu		yes	N	N	64K	64K	Y					2007	2011	http://ladybug.xs4all.	for Acorn Atom	
A	1	verilog-6502B	https://github.co	untested	Arlet Ottens	6502	16	8	kintex-7-3	James	Brakefield		6					14.7	0.67	4.0				verilog				yes	N	N	4G	4G						2011	2013	http://forum.6502.org	16-bit data RAM "bytes"	
A	1	hd63701	https://opencore	planning	Tsuyoshi Hasegawa	6801	8	8x	spartan-6-3	James	Brakef	1412	6	1	3	31	##	14.7	0.33	4.0	1.8	X		verilog	6	HD63701_CORE			N	N	64K	64K	Y					2014			Used in Atari game console, 6801 clone?	
A	1	system68	https://opencore	stable	John Kent, David Burne	6801	8	8x	spartan-3-5	James	Brakef	2235	4		4	46	##	14.7	0.33	4.0	1.7	X	Y	vhdl	21	cpu68	Y	yes	N	N	64K	64K	Y					2003	2009	http://members.optushome.com.au/jekent/		
B	1	system6801	https://opencore	stable	Michael L. Hasenfratz	6801	8	8x	cyclone-3	James	Brakef	1507	4		3	73	##	14.7	0.33	4.0	4.0	I		vhdl	15	wb_cyclo	Y	yes	N	N	64K	64K	Y					2003	2009	http://members.optu	based on John Kent's 6801	tested on Apex20K, Cyclone & Straix boards
B	1	68hc05	https://opencore	stable	Ulrich Riedel	6805	8	8x	kintex-7-3	James	Brakef	1225	6			300	##	14.7	0.33	4.0	20.2	X		vhdl	1	6805		yes	N	N	64K	64K	Y					2007	2009			
A	1	df6805	www.hitechglob	proprietar	Hitech Global	6805	8	8x	stratix-1	Hitech Global		1690	4			83			0.33	4.0	4.1	I		proprietary			Y	yes	N	N	64K	64K	Y							6805 data sheets		
A	1	system05	https://opencore	beta	John Kent, David Burne	6805	8	8x	kintex-7-3	James	Brakef	834	6			204	##	14.7	0.33	4.0	20.2	X	Y	vhdl	10	System05	Y	yes	N	N	64K	64K	Y					2003	2009	http://members.optushome.com.au/jekent/		
B	1	68hc08	https://opencore	stable	Ulrich Riedel	6808	8	8x	kintex-7-3	James	Brakef	2290	6			101	##	14.7	0.33	4.0	3.6	X		vhdl	1	x68ur08		yes	N	N	64K	64K	Y					2007	2009			
A	1	6809_6309	https://opencore	beta	Alejandro Paz Schmidt	6809	8	8x	stratix-5	James	Brakef	1711	A			223	##	q14.0	0.33	3.0	14.3	AIX		verilog	5	MC6809_	Y	yes	N	N	64K	64K	Y					2012	2015		6309 op-codes not yet implemented	
B		mc6809e		beta	Flint Weller	6809	8	8x	kintex-7-3	James	gate level prin		6					14.7	0.33	3.0				vhdl	26	core_680	Y	yes	N	N	64K	64K	Y					1999		https://www.linkedin	course work, ASIC orientation	
		rtf6809	https://github.co	alpha	Robert Finch	6809	8	8	kintex-7-3	James	many	7506	6	1	2	106	##	14.7	0.33	4.0	1.2	X		verilog	4	rtf6809	Y	yes	N	N	4G	4G	Y			8		2012	2015	http://www.finitron.c	6809 with 32-bit "FAR" addressing	probably for simulation?
A	1	system09	https://opencore	stable	John Kent, David Burne	6809	8	8x	kintex-7-3	James	Brakef	1945	6			154	##	14.7	0.33	3.0	8.7	IX	Y	vhdl	40	cpu09l	Y	yes	N	N	64K	64K	Y					2003	2016	http://members.optu	from John Kent web page	14 project directories
B	1	8051	https://opencore	alpha	Simon Teran, Jakas	8051	8	8x	kintex-7-3	James	tunrec	1744	6	1		111	##	14.7	0.33	4.0	5.3	ILX		verilog	32	oc8051_t	Y	yes	N		64K	64K	Y					2001	2016			
X	1	altium/TSK51A	http://techdocs.	proprietar	Altium	8051	8	8x	spartan-3-5	Altium		1890	4		1	50			0.33	6.0	1.5	AILX		proprietary			Y	yes	N	N	64K	64K	Y					2004	2017	CR0140.pdf, CR0115.p	frozen, asm, C, C++, schem, VHDL & Ve	default clock speed is 50MHz
W	1	cast_8051	http://www.cast	proprietar	CAST Inc	8051	8	8	virtex-6	CAST I	820 sli	1800	6		2	81	##	12.1	0.33	3.0	5.0	X		proprietary			Y	yes	N		64K	64K	Y			32				http://www.cast-inc.c	Cast has uP related IP	several versions, FPGA kits
A	1	dalton_8051	www.cs.ucr.edu	stable	Tony Givargis	8051	8	8x	kintex-7-3	James	Brakef	2725	6	1	1	105	##	14.7	0.33	1.0	12.7	X		vhdl	7	i8051_all	Y	yes	N	N	64K	64K	Y					1999	2003		ASIC	
		dp8051	https://www.dig	proprietar	Digital Core Design	8051	8	8														ILX		proprietary			Y	yes											1999			also PIC, HC11, 68000, 680x, d32pro	see more recent DQ8051CPU
		i8051		stable	Tony Givargis	8051	8	8	kintex-7-3	James	Brakef	2690	6	1	1	105	##	14.7	0.33	4.0	3.2	X		vhdl	9	i8051_all	Y	yes	N		64K	64K	Y					1999	1999		author has book & course	Embedded System Design: A Unified Hardware/
A	1	light52	https://opencore	beta	Jose Ruiz	8051	8	8	kintex-7-3	James	Brakef	1022	6	1	1	154	##	14.7	0.33	6.0	8.3	IX	Y	vhdl	8	light52_m	Y	yes	N	N	64K	64K	Y					2012	2018		targeted to balanced	~ 6 clocks/inst
A	1	mc8051	http://www.ore	stable	Helmut Mayrhofer	8051	8	8x	kintex-7-3	James	Brakef	3022	6	1		83	##	14.7	0.33	4.0	2.3	X		vhdl	49	mc8051cc	Y	yes	N	N	256	64K	Y					1999	2013	www.oreganosystem	fast 8051, version available with floating-point by David Lundgren	
A	1	mcl51	http://www.mic	stable	MicroCore Labs	8051	8	8x	artix-7-3	MicroCore La		312	6		2	180			0.33	8.0	23.8	X					Y	yes	N	N	64K	64K	Y					2016		8051 data sheets	micro-coded	
		oms8051mini	https://opencore	alpha	Simon Teran, Dinesh A	8051	8	8	kintex-7-3	James	Brakef	1991	6	1	32	133	##	14.7	0.33	5.0	4.4	X	Y	verilog	66	digital_co	Y	yes	N		64K	64K	Y					2000	2018			
		pulserain	https://www.pu	stem veril	PulseRain Tech LLC	8051	8	8																system verilog														2017		https://www.pulserain.com/fp51		238.0952381
		r8051		stable		8051	8	8	kintex-7-3	James	Brakef	1031	6	1		139	##	14.7	0.33	4.0	11.1	X		verilog	2	r8051	Y	yes	N	N	64K	64K	Y					2015	2015		source code & simulation only	
A	1	t51	https://opencore	stable	Andreas Voggeneder	8051	8	8x	kintex-7-3	James	Brakef	1942	6	1		147	##	14.7	0.33	4.0	6.2	IX		vhdl	17	T8032	Y	yes	N	N	64K	64K	Y					2002	2010	8032 data sheets	8052 & 8032	8032 SoC
A	1	turbo8051	https://opencore	beta	Dinesh Annayya	8051	8	8x	kintex-7-3	James	Brakef	1985	6	1		127	##	14.7	0.33	4.0	5.3	IX		verilog	74	oc8051_t	Y	yes	N	N	64K	64K	Y					2011	2016	8051 data sheets	includes perpherials	
		am9080	https://opencore	beta	Moshe Shavit	8080	16	8	kintex-7-3	James	hung in synthe		6				##	14.7	0.33	9.0		X		vhdl	31	cpu	Y	yes	N	N	64K	64K	Y					2917	2018	https://en.wikichip.or	emulation of AM9080 using bit-slice &	has VHDL for AMD bit-slice chips
		am9080	https://opencore	beta	Moshe Shavit	8080	16	8	kintex-7-3	James	hung in synthe		6				##	14.7	0.33	9.0		X	Y	vhdl	31	sys9080	Y	yes	N	N	64K	64K	Y					2917	2018	https://en.wikichip.or	emulation of AM9080 using bit-slice &	has VHDL for AMD bit-slice chips
A	1	cpu8080	https://opencore	stable	Scott Moore	8080	8	8x	kintex-7-3	James	Brakef	1179	6			299	##	14.7	0.33	9.0	9.3	X		verilog	1	m8080	Y	yes	N	N	64K	64K	Y					2006	2016		includes VGA display generator, three variants	
A	1	ep8080	https://github.co	beta	C.H. Ting	8080	8	8x	kintex-7-3	James	Brakef	1276	6			184	##	14.7	0.33	9.0	5.3	X		vhdl	4	ep80.vhd	Y	yes	N	N	64K	64K	Y					2002	2016	8080 data sheets	initialized Lattice memory blocks	work related to eP16
A	1	light8080	https://opencore	stable	Jose Ruiz, Moti Litoche	8080	8	8	kintex-7-3	James	Brakef	154	6		1	247		14.7	0.33	9.0	58.9	IX		verilog	5	i80soc	Y	yes	N	N	64K	64K	Y					2007	2015		targeted to area, includes UART, interr	older versions have both VHDL & Verilog
A		gl85	http://simlab.ec	stable	Alex Miczo	8085	8	8x	kintex-7-3	James	gate level des		6					14.7	0.33	4.0		X		vhdl	1	i8085	Y	yes	N	N	64K	64K	Y					1993		http://www.fpga.wor	also a TTL implementation in VHDL	
		ep994a	https://github.co	stable	Erik Piehl	9900	16	16	kintex-7-3	James	Brakef	1340	6		5	286	##	14.7	0.83	3.0	59.0	X		vhdl	10	ep994a	Y	yes	N	N	64K	64K	Y			16		2016	2017	https://hackaday.io/p	TI 990 emulation	
A	1	ao68000	https://opencore	beta	Aleksander Osman	68000	16	16x	arria-2	James	Brakef	3479	A		6	169	##	q13.1	0.67	3.0	10.8	I	Y	verilog	1	ao68000	om	yes	N		4G	4G	Y					2010	2012		uses microcode, instruction prefetch buffer	
B		aoocs	https://github.co	beta	Aleksander Osman	68000	16	16x	cyclone-2	Aleksander O		26227	4	2	65		##	q10.1	0.67	4.0		I	Y	verilog	22	aoOCS	om	yes	N		4G	4G	Y					2010	2011	68000 data sheets	uses ao68000 core, Amiga chip set em	Wishbone Amiga OCS SoC
B		aoocs	https://github.co	beta	Aleksander Osman	68000	16	16x	kintex-7-3	James	altera pimitive		6				##	14.7	1.00	1.0		I	Y	verilog	22	aoOCS	om	yes	N		4G	4G	Y					2010	2011	68000 data sheets	uses ao68000 core, Amiga chip set em	Wishbone Amiga OCS SoC
B		aoocs	https://github.co	beta	Aleksander Osman	68000	16	16x	cyclone-4	James	fitter e	27795	4	2	65		##	q17.0	0.67	4.0		I	Y	verilog	22	aoOCS	om	yes	N		4G	4G	Y					2010	2011	68000 data sheets	uses ao68000 core, Amiga chip set em	Wishbone Amiga OCS SoC
		apollo	http://wiki.apollo	proprietar	Gunnar von Boehn	68000	32	16																proprietary			Y	yes	N		4G	4G	Y			32				http://www.apollo-ac	sells Amiga card, 68080 with 64-bit ins	claims very fast FPGA versions
A	1	k68	https://opencore	alpha	Shawn Tan	68000	8	16x	kintex-7-3	James	Brakef	2392	6			24	##	14.7	0.67	4.0	1.7	X		verilog	15	k68_cpu	Y	yes	N	N	4K	4G	Y			16		2003	2009		68K binary compatible	
		mc68kods	https://sites.goo	beta	Olivier De Smet	68000	32	16	kintex-7-3	James	errors	4617	6				##	14.7	1.00	8.0			Y	vhdl	10	mc68kods													2011			SOC for HP9816 computer emulation	
A	1	minimig	https://code.goo	stable	Frederic Requin	68000	32	16	stratix-2	Freder	speed	1900	4		4	180			1.00	6.0	15.8	I		verilog	1	j68	Y	yes	N		4G	4G	Y			16		2009	2014		for use with Minimig	micro-coded on stack machine
B		rtf68ksys	https://opencore	alpha	Robert Finch	68000	16	16x	spartan-3e-	James	need t	13639	4	12	17		##	14.7	0.67	4.0		X	Y	verilog	49	rtf68kSys	Y	yes	N	N	4G	4G	Y			16		2011	2011	https://github.com/rc	based on Tobias Gubener's TG68	
A	1	suska-III	http://www.exp	beta	Wolfgang Forster	68000	16	16	arria-2	James	Brakef	7388	A			55	##	q13.1	0.67	4.0	1.3	I		vhdl	11	wf68k00il	Y	yes	N	N	4G	4G	Y			16		2003	2013	68000 data sheets	for use as an Atari ST	
A	1	tg68	https://opencore	stable	Tobias Gubener	68000	16	16x	kintex-7-3	James	Brakef	2331	6			44	##	14.7	0.67	4.0	3.2	X		vhdl	2	TG68_fas	Y	yes	N	N	4G	4G	Y			16		2007	2012	68000 data sheets	TG68 - execute 68000 Code	for use with Minimig
A	1	v1_coldfire	https://www.silv	proprietar	IPextreme	68000	16	16x	cyclone-3	freescale		5000	4			80			0.89	1.0	14.2	I		verilog			Y	yes	N	N	4G	4G	Y			16		2008		https://www.silvaco.c	free for Altera	3500 LUTs on Stratix-III
		whitham_68k	https://www.jwh	errors	Jack Whitham	68000	32	16	kintex-7-3	James	no top module						##	14.7	0.67	4.0				vhdl			Y	asm			4G	4G	Y			16		2002	2003		university project, 68020 subset	read thesis, code generator for top modules
		cf_ssp	https://opencore	stable	Tom Hawkins	?																		confluence														2003	2009		confluence to VHDL	CF State Space Processor
A	1	gup	https://opencore	stable	Kevin Phillipson	68HC11	8	8x	arria-2	James	Brakef	925	A	1	1	127	##	q13.1	0.33	4.0	11.3	I		vhdl	25	gator_up	Y	yes	N	N	64K	64K	Y					2008	2011	https://www.mil.ufl.e	top level is schematic	
A	1	hc11core	http://www.gmv	stable	Green Mountain Comp	68HC11	8	8x	kintex-7-3	James	Brakef	2190	6			127	##	14.7	0.33	4.0	4.8	X		vhdl	1	hc11rtl	Y	yes	?	N	64K	64K	N	53		8	2	2000		6811 data sheets	restricted use license, with corrections	
A	1	system11	https://opencore	alpha	John Kent, David Burne	68HC11	8	8x	kintex-7-3	James	Brakef	1218	6			153	##	14.7	0.33	4.0	10.3	X	Y	vhdl	17	cpu11	Y	yes	N	N	64K	64K	Y					2003	2009	http://members.optu	known bugs & untested instructions	

	_uP_all_soft folder	opencores or prmary link	status	author	style / clone	data size	inst size	FPGA	reporter	comment	LUTs ALUT	LUT?	mults	blk ram	F max	date	tool ver	MIPS /inst	clks/ inst	KIPS /LUT	vendor	SOC	src code	# src files	top file	doc	tool chain	fltg pt	Hav	max data	max inst	byte adrs	# inst	adr mod	# reg	pipe len	start year	last revis	secondary web link	note worthy	comments
	8bit-verilog_mcu		stable	Josh Friend	accum	8	8	kintex-7-3	James	insert	240	6		1	328	##	14.7	0.33	2.0	225.5	X		verilog	11	cpu					512	512	Y	16						for class project, small data stack	PB clock, students to add features
	acc	https://github.co	stable	Juan Gonzalez-Gomez	accum	15	15	kintex-7-3	James	rom &	88	6		1	227	##	14.7	0.67	2.0	865.2	IX		verilog	1	acc2	Y	yes	N			4K					2016	2016	https://github.com/O	26 chptr course using Apollo Comman	??why LUT count different from agcnorm
X	1 agcnorm	https://opencore	beta	Dave Roberts	accum	15	15	spartan-3a-	James	Brakef	3732	4		2	20	##	14.7	0.66	1.0	3.5	X		vhdl	5	AGC	Y		N	Y	4K	72K	N	11		1		1962	2012	http://klabs.org/histo	Apollo Guidance Computer via 3-input	NOR gate emulation
	ahmes	https://github.co	stable	Fabio Pereira	accum	8	8	kintex-7-3	James	Brakef	186	6			476	##	14.7	0.33	3.0	281.6	X		vhdl	3	ahmes			N	N	256	256	Y	15	1			2016	2017			bare CPU with no RAM
W	1 blue	https://opencore	stable	Al Williams	accum	16	16	spartan-3-5	James	remov	1025	4			63	##	14.7	0.67	1.0	41.1	X		verilog	16	topbox	web		N		4K	4K	N	16		2		2009	2010		derived from Caxton Foster's Blue	http://www.youtube.com/watch?v=dt4zezZP8v
	c88	https://github.co	alpha	Daniiel Bailey	accum	8	8	spartan-3-5	James	Dff ge	2664	4	2		54	##	14.7	0.33	1.0	6.7	X		vhdl	25	C88	Y	asm	N		8	256	Y	10		8		2015	2015	https://www.youtube	only 8 memory locations	used 3785 Dff, doesn't infer block or LUT RAM
	c88	https://github.co	alpha	Daniiel Bailey	accum	8	8	kintex-7-3	James	Brakef	3088	6	2		167	##	14.7	0.33	2.0	8.9	X		vhdl	25	C88	Y	asm	N		8	256	Y	10		8		2015	2015	https://www.youtube	only 8 memory locations	used 3658 Dff, doesn't infer block or LUT RAM
	1 classic_HP_calc	https://github.co	stable	Brian Nemetz	accum	56	10	kintex-7-3	James	Brakef	1750	6		3	233	##	14.7	0.17	10.0	2.2	X		vhdl	15	classichp_	Y		N		30	4K	N	40		7		2012			processor & ROMs for HP-55, 45 & 35	includes LED display driver & UART, for Papilio C
	ez8	https://github.co	stable	Howard Mao	accum	8	16	kintex-7-3	James	replac	644	6		2	233	##	14.7	0.33	2.0	59.6	X		verilog	13	ez8_cpu					256	4K						2014	2014	http://zhehaomao.com/		not sure inferred RAM correct?
	fpga4_8bit_up	http://www.fpga	stable	Van Loi Le	accum	8	8	kintex-7-3	James	Brakef	258	6		1	200	##	14.7	0.33	3.0	85.3	X		vhdl	9	computerpme			N		96	128	Y	10		2		2016	2016	book: LaMeres Introd	educational	16 input & 16 output ports fill out 256 byte adr s
	fpga4_up8_12	http://www.fpga	errors	Van Loi Le	accum	8	12	kintex-7-3	James	degenerate de		6				##	14.7	0.33	1.0				verilog	7	microcontroller			N									2016	2016		educational, simplified PIC12	incomplete
X	1 inst_list_proces	https://opencore	planning	Mahesh Palve	accum	8	15	kintex-7-3	James	using	786	6		1	340	##	14.7	0.33	1.0	142.6	X		verilog	34	top	Y		N		128	1K		32				2014			pipelined, state machine	UART, SPI & timer included
	lem1_9	https://opencore	alpha	James Brakefield	accum	1	9	kintex-7-3	James	1 stag	75	6		1	171	##	14.5	0.04	1.0	91.2	IX		vhdl	2	lem1_9	Y		N	Y	32	2K	N	24			1	2016			single bit at a time, absolute adrs	
W	1 lem1_9min	https://opencore	stable	James Brakefield	accum	1	9	kintex-7	James	1 stag	63	6		1	358	##	14.5	0.04	1.0	227.2	ILX		vhdl	3	lem1_9m	Y	asm	N	Y	64	2K	N	8		64	1	2003	2009		logic emulation machine	
W	1 lem1_9ptr	https://opencore	beta	James Brakefield	accum	1	9	kintex-7-3	James	1 stag	147	6		1	176	##	14.5	0.06	1.0	72.0	IX		vhdl	2	lem1_9pt	Y		N	Y	512	2K	N	24			1	2016			use speed opt, logic emulation machin	4 index registers: (ix),(--ix),(ix++),(ix+off)
	lem16_18		alpha	James Brakefield	accum	16	18	kintex-7-3	James	Brakef	483	6		1	294	##	14.5	0.16	1.0	97.4	X		vhdl	2	lem16_18m			N		256	1K		77			1	2010	2018		variable bit-length memory read/write	op-codes coded, untested
W	lem4_9	https://opencore	beta	James Brakefield	accum	4	9	kintex-7-3	James	1 stag	144	6		1	195	##	14.5	0.16	1.0	216.7	IX		vhdl	2	lem1_9	Y		N	Y	32	2K	N	24			1	2016			binary & BCD digit addition, speed mode	
W	1 lem4_9ptr	https://opencore	beta	James Brakefield	accum	4	9	kintex-7-3	James	1 stag	151	6		1	151	##	14.5	0.24	1.0	240.0	IX		vhdl	2	lem1_9pt	Y		N	Y	512	2K	N	24			1	2016			binary & BCD digit addition, speed mo	4 index registers: (ix),(--ix),(ix++),(ix+off)
W	1 leros	https://opencore	stable	Martin Schoeberl	accum	16	16	spartan-6	Martin	Schoe	112	6		1	182			0.67	1.0	1088.8	IX		vhdl	5	leros	Y	yes	N	Y	256	64K				2	2	2008	2012	https://github.com/sc	256 word data RAM, PIC like	short LUT inst ROM
	leros32	https://github.co	simulation	Jon Pry	accum	32	16	kintex-7-3	James	missing memory components											IX		vhdl	10	leros_nexys2			N		4G	4G						2013			see Leros entry, simulation only	missing several dual port RAMs
X	1 lwrisc	https://opencore	stable	Li Wu	accum	8	12	arria-2	James	Brakef	88	A		1	230	##	q13.1	0.17	1.0	443.6	I		verilog	9	risc_core		asm	N	Y	256	2K	Y	16				2008	2009		ClaiRISC simplified PIC, 4 reg rtn stack	absolute addressing only, lowered MIPS/clk
	mano_machine	https://github.co	stable	Susam Pal	accum	16	16	kintex-7-3	James	needs	364	6				##	14.7	0.67	2.0				vhdl	5	microproc	Y		N		4K	4K	N	25				2005	2016	Computer System Arc	course project, bidir mem data	for XC9572 CPLD, large # of latches
X	1 mcpu	https://opencore	stable	Tim Boscke	accum	8	8	spartan-6-3	James	Brakef	41	6			384	##	14.7	0.08	1.0	749.0	X		vhdl	1	tb02cpu2	Y	asm	N		64	64	Y	4				2007	2014		MCPU A minimal CPU for a CPLD	reduced MIPS/clk due to only 4 inst
	mcu8	https://opencore	alpha	Dimo Pepelyashev	accum	8	8	kintex-7-3	James	Brakef	274	6			299	##	14.7	0.33	1.0	360.1	X		vhdl	16	processor_E		asm			256	256	Y	17				2008	2009		asm, simulated, builds?	
X	1 micro16b	http://members	beta	John Kent	accum	16	16	kintex-7	James	Brakef	205	6			434	##	14.7	0.33	2.0	349.0	X		vhdl	1	u16bcpu	Y	asm	N	N	64K	4K	Y	8				2002	2008	http://members.optu	very limited inst set	MIPS/clk adj'd, 2 clks/inst
X	1 micro8a	http://members	beta	John Kent	accum	8	16	kintex-7	James	Brakef	531	6			204	##	14.7	0.33	3.0	42.3	X		vhdl	11	Micro8	Y		N	N	2K	2K	Y					2002	2002	http://members.optu	derived from Tim Boscke's mcpu	also micro8 and micro8b variants
	mroell_cpu	https://bitbucke	stable	Matthias Roell	accum	8	8	kintex-7-3	James	added	185	6			357	##	14.7	0.33	1.0	637.1	X		vhdl	8	cpu	Y							10				2014	2016		university course project	
W	1 mycpu	http://www.myc	mature	Dennis Kuschel	accum	8	8	kintex-7-3	James	Brakef	3428	6	1		155	##	14.7	0.33	3.0	5.0	X		vhdl	28	cpu_top	Y		N		64M	64M	Y					2010			originally in TTL	micro-coded
	ncore	https://opencore	alpha	Stefan Istvan	accum	16	8	kintex-7-3	James	Brakef	223	6			105	##	14.7	0.67	1.0	316.3	X		verilog	3	nCore	Y		N		128K	64K		16		16		2006	2015		This is a little-little processor core	
	non-von-1	http://www.chri	stable	Christopher Fenton	accum	8	8	kintex-7-3	James	Brakef	230	6			556	##	14.7	0.33	1.0	797.1			verilog	1	nonvontop		no	N		64		Y	30							SIMID in tree structure	A & B regs, instructions broadcast
	parwan		stable	Zainalabedin Navabi	accum	8	8	kintex-7-3	James	Brakef	157	6			435	##	14.7	0.33	4.0	228.5	X		verilog	16	par_beh	Y	yes	N	N	4K	4K	Y					1995	1997	2nd uP in directory	from VHDL: Analysis and Modeling of D	AKA cpu8, both vhdl & verilog versions
	parwan		stable	Zainalabedin Navabi	accum	8	8	kintex-7-3	James	Brakef	161	6			76	##	14.7	0.33	4.0	38.8	X		vhdl	2	parwan	Y	yes	N	N	4K	4K	Y					1995	1997	2nd uP in directory	from VHDL: Analysis and Modeling of D	AKA cpu8, both vhdl & verilog versions
X	1 popcorn	http://www.fpga	stable	Jeung Joon Lee	accum	8	8	kintex-7-3	James	Brakef	267	6			347	##	14.7	0.33	1.0	428.4	X		verilog	4	pc	Y		N		64K	64K	Y	43				1998	2000		small 8 bit uP	
	prawn		errors	Tadatoshi Ishii	accum	8	8	spartan_6-3	James	missing files		6				##	14.7	0.33	3.0				vhdl	2	prawn	Y	yes	N	N	4K	4K	Y					1992			reduced version of parwan from VHDL:	Analysis and Modeling of Digital Systems, 1993
	pt13	http://www.sing	untested	Daniel Ogilvie	accum	8	8	kintex-7-3	James	Brakef	301	6			357	##	14.7	0.33	3.0	130.5			verilog	1	pt13	Y	asm	N	Y	64K	8K	Y	40	3			2011	2018	https://www.edn.com	PT13 is optimized to be completely em	micro-code & register updates, minimal ISA
W	1 rtf65002	https://opencore	alpha	Robert Finch	accum	32	8	kintex-7-3	James	Brakef	11216	6	4	6	123	##	v14.1	0.67	2.0	3.7	X		verilog	10	rtf65002c	Y		N		4G	4G	Y			16		2013	2013	https://github.com/rc	32-bit 6502 + 6502 emulation	"proven"
	sap	https://opencore	stable	Ahmed Shahein	accum	8	8	kintex-7-3	James	no LU	48	6			200	##	14.7	0.10	4.0	104.2	X		vhdl	15	mp_struct			N		16	16	Y	5				2012	2017	https://shirishkoirala.	Simple as Possible Computer from Mal	https://www.youtube.com/watch?v=prpyEFxZC
	t180-cpu		stable		accum	8	8	kintex-7-3	James	bypass	709	6			83	##	14.7	0.33	3.0	12.9	X		vhdl	23	cpu			N	N	64K	64K	Y					2016	2016	https://www.vttoth.c	8-bitter with pc, sp, a, b, c & d regs	based on Viktor Toth's 4 bit microcontroller
	td4	https://github.co	stable	cielo_ee	accum	8	8	spartan-3	James	Brakef	102				200	##	14.7	0.20	1.0	392.2	X		verilog	5	td4_top						16	Y					2012	2015			very small uP
	tiny8	https://opencore	altera dsg	Ulrich Riedel	accum	8	8	kintex-7-3	James	altera project		6				##	14.7	0.33	3.0		I		ahdl							256	64K	Y			256		2002			Altera megafunctions	
X	1 tisc	https://opencore	beta	Vincent Crabtree	accum	8	8	kintex-7-3	James	Brakef	195	6			87	##	14.7	0.33	1.0	147.1	X		vhdl	1	TISC			N		256	1K	Y			2		2009	2009		Tiny Instruction Set Computer	minimal accumulator machine
	uos	https://opencore	mature	Daniel Roggen	accum	8	16	kintex-7-3	James	Brakef	441	6			270	##	14.7	0.33	3.0	67.4	X		vhdl	14	cpu	Y								3	4		2014	2017		UoS Educational Processor	inspired by x86 ISA
	up3	https://people.e	stable	Bruce Land	accum			cyclone-2	Bruce	Land	186	4		1		##	q8.0						verilog	1	de2_top														Cornell ECE576	basic core is scomp, used by up3 & de2_top'
X	1 usimplez	https://opencore	stable	Pablo Salvadeo etal	accum	12	12	stratix-2	Pablo	Salvade	48	4			134		q9.1	0.17	2.0	237.9	I		vhdl	3	usimplez_cpu			N		512	512		8				2011		http://www-gti.det.u	part of university course, simplez+i4	has an index register
	ARC	https://www.syn	proprietar	Synopsys	ARC	32	16	porprietary											1.0				proprietary			Y	yes			4G	4G									several families each with options	for ASIC use
	core_arm	https://opencore	beta	Konrad Eisele	ARM	32	16	kintex-7-3	James	Brakef	1239	6		3	250	##	14.7	1.00	1.0	201.8	X	Y	vhdl	151	arm_proc	Y	yes	N		256M	256M				16		2004	2009	http://cfw.sourceforg	very large project with many unused s	missing files found in sourceforge dir, very little
	cortex_m3	http://www.clou	proprietar	Tobias Strauch	ARM	32	16																proprietary												16		2013		cortex M3 data sheet	claims to be mature	various academic papers, several projects
A	1 ARM_Cortex_A	https://develope	ASIC	ARM	ARM a53	64	32	asic	Xilinx		6000	A			1500			2.00	0.5	1000.0			asic			Y	yes	Y				Y							https://en.wikipedia.c	uses pro-rated LC area	dual issue, includes fltg-pt & MMU & caches
A	1 ARM_Cortex_A	https://develope	ASIC	ARM	ARM a9	32	16	arrira V	altera		4500	A			1050			2.50	1.0	583.3			asic			Y	yes	Y		4G	4G	Y	80		16	10		2012	https://en.wikipedia.c	uses pro-rated LC area	dual issue, includes fltg-pt & MMU & caches
A	1 ARM_Cortex_M	https://www.arm	proprietar	ARM	ARM M1	32	12	virtex-5	ARM	65nm	1900	6			200			1.00	1.0	105.3	AIX					Y	yes	N		4G	4G	Y			16	3	2007		https://en.wikipedia.c	ARM Cortex M0, M1 & M3 avail for FP	see xilinx Xcell64
A	1 ARM_Cortex_R	https://develope	ASIC	ARM	ARM r5	32	16	asic	Xilinx			A			600				1.0				asic			Y	yes	Y		4G	4G	Y	80		16				https://en.wikipedia.c	uses pro-rated LC area	real-time interrupt handling
A	1 amber	https://opencore	stable	Conor Santifort	ARM7	32	32	kintex-7-3	James	Brakef	6409	6		2	82	##	14.7	0.75	1.0	9.6	ILX		verilog	25	a23_core	Y	yes	N		4G	4G	Y				3	2010	2017	https://en.wikipedia.c	no MMU, shared cache	2048 LUTs used as single port RAM
A	1 arm4u	https://opencore	stable	Joanathan Masur, Xavi	ARM7	32	32	aria-2	James	Brakef	1668	A	4	8	66	##	q13.1	0.75	1.0	29.5	I		vhdl	12	cpu	Y	ues	N		4G	4G	Y	80		16	5	2013	2014		university project	altera memory
B	oks8	https://opencore	alpha	Kongzilee	ARM7	32	32	kintex-7-3	James	bad coding pra		6				##	14.7	0.67	1.0				verilog	8	oks8	Y	yes	N		64K	64K	Y					2006	2009		clone of KS86C4204/C4208/P4208, SAM87RI	instruction set
A	1 storm_core	https://opencore	beta	Stephan Nolting	ARM7	32	32	kintex-7-3	James	Brakef	2312	6	3		179	##	14.7	1.00	1.0	77.4	IX		vhdl	16	CORE	Y	yes	N		4G	4G	Y			32	8	2011	2014		Storm Core (ARM7 compatible)	I & D caches not compiled
	storm_soc	https://opencore	beta	Stephan Nolting	ARM7	32	32	kintex-7-3	James	empty design,		6				##	14.7	1.00	1.0				vhdl			Y	yes	N		4G	4G	Y			32	8	2012	2015		STORM SoC	
	zap	https://opencore	alpha	Revanth Kamaraj	ARM7	32	32	kintex-7-3	James	Brakef	7723	6	1	9	114	##	14.7	1.00	1.0	14.7	X		verilog	37	zap_top	Y	yes	N	N	4G	4G	Y			16		2017	2017	ddi0100e_armv1-5_rn	ARMv4T & Thumbv1	has cache & mmu
	atmega8_pong	https://fr.wikive	stable		AVR	8	16	spartan-3-5	James	clock	2767	4	1	10	53	##	14.7	0.33	1.0	6.3	X	Y	vhdl	37	avr_fpga_	Y	yes	N		64K	64K	Y	17		4		2017	2017		several projects using avr core	uses Sauermann core
	atmega8_pong	https://fr.wikive	stable		AVR	8	16	spartan-3-5	James	clock	2898	4	1	11	53	##	14.7	0.33	1.0	6.0	X	Y	vhdl	37	pacman_l	Y	yes	N		64K	64K	Y	17		4		2017	2017		several projects using avr core	uses Sauermann atmega16 core
A	1 avr_core	https://opencore	stable	Rusian Lepetenok	AVR	8	16	kintex-7-3	James	Brakef	2135	6			127	##	14.7	0.33	1.0	19.7	X		verilog	15	avr_core	Y	yes	N		64K	128K	Y			32		2002	2017		VHDL core also	
	avr_fpga	https://opencore	stable	Juergen Sauermann	AVR	8	16	kintex-7-3	James	Brakef	1606	6	1	6	120	##	14.7	0.33	1.0	24.7	X		vhdl	20	cpu_core	Y	yes	N		64K	128K	Y			32		2009	2010		from PDF file	
	avr_fpga	https://opencore	stable	Juergen Sauermann	AVR	8	16	kintex-7-3	James	Brakef	1877	6	1	6	115	##	14.7	0.33	1.0	20.2	X	Y	vhdl	20	avr_fpga	Y	yes	N		64K	128K	Y			32		2009	2010	https://fr.wikiversity.	from PDF file & atmega8_pong_vga	missing module in atmega8_pong_vga
A	1 avr_hp	https://opencore	stable	Strauch Tobias	AVR	8	16	kintex-7-3	James	2 slot	1554	6			223	##	14.7	0.33	1.0	47.4	X		vhdl	10	avr_core_pm	Y	yes	N		64K	128K	Y			32		2010	2012		hyper pipelined (eg barrel) AVR	
A	1 avr8	https://opencore	beta	Nick Kovach	AVR	8	16	kintex-7-3	James	Brakef	174	6			418	##	14.7	0.33	1.0	792.2	X		verilog	1	rAVR	Y	yes	N		64K	64K	Y	17		4		2010	2010		Reduced AVR Core for CPLD	not a full clone, doc is opencores page
A	1 avrtinyx61core	https://opencore	beta	Andreas Hilvarsson	AVR	8	16	kintex-7-3	James	Brakef	1243	6			194	##	14.7	0.33	1.0	51.5	X		vhdl	1	mcu_core		yes	N		64K	128K	Y			32		2008	2009			
A	ax8	https://opencore	stable	Daniel Wallner	AVR	8	16	spartan-6-3	James	missin	1549	6		1	213	##	14.7	0.33	1.0	45.3	X		vhdl	14	A90S1200		yes	N		64K	128K	Y			32		2002	2010		both A90S1200 & A90S2313	inserted fake inst ROM
A	1 navre	https://opencore	stable	Sebastien Bourdeaudu	AVR	8	16	kintex-7-3	James	Brakef	990	6			207	##	14.7	0.33	1.0	69.0	AILX		verilog	1	softusb_r	Y	yes	N		64K	64K	Y			32	2	2010	2013	https://www.milkymi	AVR clone, part of www.milkymist.org	
	pavr	https://opencore	alpha	Doru Cuturela	AVR	8	16	kintex-7-3	James	Brakef	2630	6		1	132	##	14.7	0.33	1.0	16.5	X		vhdl	18	pavr_con	Y	yes	N	Y	4K	4M	Y			32	6	2003	2009		superset of AVR	
A	riscmcu	https://opencore	stable	Yapzihe	AVR	8	16	arria-2	James	LPM paramete		6					14.7	0.33	1.0		I		vhdl	15	v_riscmcu	Y	yes	N		128	512	Y	92		16		2002	2009	AVR data sheets	RISC Microcontroller	
	xmega_core	https://opencore	beta	Gheorghiu Iulian	AVR	8	16	kintex-7-3	James	Brakef	1116	6			120	##	14.7	0.33	1.0	35.6	X		verilog	34	mega_co	Y	yes	N		64K	128K	Y			32		2018		https://git.morgothdi	1 core complete, 7 more variants in the	works
W	1 c16	https://opencore	stable	Jsauermann	C	16	8x	spartan-3-5	James	Brakef	1751	4		16	57	##	14.7	0.33	1.0	10.7	X		vhdl	22	Board_cp	min	C,asm	N		64K	64K	Y			5		2003	2012		8080 derivative, optional UART, 8-bit n	xilinx 4K RAM primitives
	hp86b	https://sites.goo	errors	Olivier De Smet	Capricorn	8	8	spartan-3-5	James	unresolved xil		4				##	14.7	0.33	2.0				verilog	85	cpu										64		2010		https://en.wikipedia.c	uses PicoBlaze, emualtes HP86B	picoblaze uart uses LUT4s

		_uP_all_soft folder	opencores or prmary link	status	author	style / clone	data size	inst size	FPGA	reporter	comment	LUTs ALUT	LUT?	mults	blk ram	F max	date	tool ver	MIPS /inst	clks/ inst	KIPS /LUT	vendor	SOC	src code	# src files	top file	doc	tool chain	fltg pt	Hav	max data	max inst	byte adrs	# inst	adr mod	# reg	pipe len	start year	last revis	secondary web link	note worthy	comments
X	1	vtach	https://opencore	mature	Al Williams	CARDIAC	13	12	spartan-3-4	James Brakef		557	4			71	##	14.7	0.50	1.0	64.1	X		verilog	16	vtach			N		256	256	Y					2013	2014		ISE project only, BCD arithmetic	VTACH Bell Labs CARDIAC reimagined in Verilog
		lc-2	http://www.cs.u	mature	Eric Frohnhoefer	CISC	16	16	kintex-7-3	James	gate level prin		6				##	14.7	0.67	2.0				vhdl	13	lc2_all	Y	yes	N		64K	64K	N	16		8		2002	2002	https://en.wikipedia.(	from book: 978-0072467505 by Patt &	educational, compiled via Synopsys
X	1	raptor16	www.spacewire.	stable	Steve Haywood	CISC	16	16	kintex-7-3	James Brakef		590	6			319	##	14.7	1.40	2.7	280.2	X		vhdl	1	raptor16	Y	yes	N	N	64K	64K	N					2004			8 data & 8 adr regs	no multiply, 8 adr modes
		w450		errors	Ze Long	CISC	8	8	kintex-7-3	James	blocking & no		6				##	14.7	0.33	3.0				verilog	3	w450					256	256	Y	8		4	3	2012			appears to be class project	3 versions of w450, used latest, patches caused
X		xproz	http://www.bitli	stable	Herbert Kleebauer	CISC	16	16x			schematic based									1.0				schematic			Y	asm	N		64K	64K						1995			documentation in German	schematic design
		z3	https://opencore	stable	Charles Cole	CISC	8	8	kintex-7-3	James	altera PLL		6				##	14.7	0.33	3.0		I		verilog	3	zmachine	Y				128K	128K						2014	2014	https://en.wikipedia.(	Infocom Z-Machine V3, youtube video	http://inform-fiction.org/zmachine/standards/
		z-machine	https://github.co	stem veril	Robert Baruch	CISC	8	8	kintex-7-3	James Brakefield			6				##	14.7	0.33	3.0				system v	15	plugh	Y		N									2016		http://inform-fiction.(	Z-machine (Zork)	https://www.youtube.com/watch?v=2fNBkUCjl
		t400	https://opencore	stable	Arnim Laeuger	COP400	4	8	spartan-2	Arnim Laeuge		643	3		2	60			0.16	4.0	3.7	IX		vhdl	36	t400_core	Y	yes	N	Y	64	1K	Y					2006	2009		implementation of National's 4-bit COP400 microcontroller	
A	1	cray1	www.chrisfenton	alpha	Christopher Fenton	cray1	64	16	kintex-7-3	James Brakef		13463	6	19	10	127	##	14.7	6.00	1.0	56.6	X		verilog	46	cray_sys_	Y	yes	Y	N	4M	4M	N			512		2010	2015	CRAY data sheets	homebrew Cray1	
		cray2_reboot	https://opencore	beta	John Kula	cray2	64	16																no files			Y											2016	2017	Cray 1, 2 & 3 docs	gate level code	goal of gate and clock equivalence
A	1	aspida	https://opencore	stable	Sotiriou	DLX	32	32	kintex-7-3	James Brakef		3586	6			257	##	14.7	1.00	1.0	71.7	X		verilog	10	DLX_top	Y	yes			4G	4G						2002	2009		DLX	compiled sync version
		dlx		errors	Martin Gumm	DLX	32	32	kintex-7-3	James	errors		6				##	14.7	1.00	1.0				vhdl	120		Y	asm								32		1995	2014		University of Stuttgart, asic dsgn	case statmt others clause has problems
X	1	bobcat		beta	Stan Drey	DSP	16	24	kintex-7-3	James Brakef		1622	6	1		107	##	14.7	0.67	1.0	44.0	X		vhdl	30	bobcat_c	Y		N		64K	64K						1998	2000			dead web links
		dspuva16	http://www.DTE	stable	Santiago de Pablo	DSP	16	16	kintex-7-3	James Brakef		332	6			317	##	14.7	0.67	1.0	640.7	X		verilog	1	dspuva16		asm	N	Y	256	4K		40		16		2001	2004		16 bit data memory, 24 bit regs	broken web link
A	1	oc54x	https://opencore	beta	Richard Herveille	DSP	16	16	kintex-7-3	James Brakef		2225	6	1		180	##	14.7	0.67	1.0	54.1	X		verilog	10	oc54_cpu	Y	yes	N	Y	64K	64K						2002	2009		40-bit accumulator, barrel shifter	C54x clone
W	1	ensilica	http://www.ens	proprietar	ensilica.com	eSi-3200	32		stratix-4	ensilica		1800	A			200			1.00	1.0	111.1	IX		proprietary			Y	yes			4G	4G				16	5				verilog source included with license	10 addressing modes
X	1	8bit_chapman	http://www.ece	beta	Rob Chapman, Steven	forth	8	8	kintex-7-3	James Brakef		176	6			131	##	14.7	0.33	1.0	245.5	ILX		vhdl	10	stack_prc	Y		N		256	256						1998	1998		course work	
W	1	b16	www.bernd-pay	stable	Bernd Paysan	forth	16	5	spartan-6-3	James Brakef		554	6			134	##	14.7	0.67	1.0	161.7	IX		verilog	1	b16	Y	yes	N									2002	2011		two versions: one/15 source files, derived from c18	
		bytemachine	https://github.co	mature	c0pperdragon	forth	8	8	kintex-7-3	James Brakef		319	6		1	250	##	14.7	0.33	2.0	129.3	IX		vhdl	7	bytemachine			N	N		4K	Y	30				2016	2017		top is Altera schematic	results are for 2016 bare core
		cd16	http://anycpu.or	stable	Brad Eckert	forth	16	16	spartan-3-5	James Brakef		681	4			83	##	14.7	0.67	2.0	41.0	IX		vhdl	16	cd16			N		128K	8M						2003	2003	http://web.archive.or	Spartan-3 block RAM	bare core
		cd16	http://anycpu.or	stable	Brad Eckert	forth	16	16	spartan-3-5	James Brakef		618	4		7	31	##	14.7	0.67	2.0	16.9	IX	Y	vhdl	16	demosocext			N		128K	8M						2003	2003	http://web.archive.or	Spartan-3 block RAM	includes stack RAMs & some inst RAM
		cpu16	http://www.ultr	stable	C.H. Ting	forth	16	5	kintex-7-3	James Brakef		347	6			364	##	14.7	0.67	1.0	702.1	X		vhdl	1	cpu16			N	N	64K	64K	N	28				2000	2000		P16 in VHDL	CPU24.vhd with width=16
X		dataflow_chapl	https://opencore	alpha	Rob Chapman, Steven	forth	16	16	kintex-7-3	James	file WebCase		6					14.7	0.33	1.0				vhdl	27	DataFlow	Y		N		256	256						2003			course work	
W	1	dfp	https://opencore	stable	Ron Chapman	forth	8	Y	kintex-7-3	James Brakef		297	6			192	##	14.7	0.33	1.0	213.2	X		vhdl	25	DataFlow	Y											2003	2009		8-bitter, generates a custom VHDL stack machine, compiler is in Forth	
W	1	ep16	https://github.co	beta	C.H. Ting	forth	16	5	kintex-7-3	James Brakef		837	6			254	##	14.7	0.67	1.0	203.6	X		vhdl	5	ep16.vhd	Y	yes	N	N	32K	32K	N	32				2005	2012	PDF files	initialized Lattice memory blocks	5-bit instructions
		ep24		stable	C.H. Ting	forth	24	6	kintex-7-3	James	substi	1020	6		3	167	##	14.7	0.83	1.0	135.6	X		vhdl	1	ep24	Y	asm	N	N		4K		27				2002	2002		room for 37 additional op-codes	removing stack clear: 503 LUT6 & 143MHz
		ep32		proprietar	C.H. Ting	forth	32																	proprietary																	PDFs only	
W	1	eric5		proprietar	entner-electronics.com	forth	9	8	cyclone-4-6	enter-electro		110	4	opt		60			0.42	1.0	229.1	I		proprietary							512	1K				3-4		2007			25 MIPS: ERIC5xs, ERIC5Q	
		f18a	http://www.gree	asic	Chuck Moore	forth																		proprietary			Y	yes													AKA G144A12: 12x12 array	family of parallel processors
		f21		asic	Jeff Fox	forth																		proprietary																	from Ultra Technology	
		fc16		paper	Richard Haskell	forth	16																	proprietary																	PDF papers	see his book: VHDL By Example: Fundamentals c
		forth_kf532	https://github.co	stable	Tarasov Ilia	forth	32	6	kintex-7-3	James	no *.c	1719	6	4	4	172	##	14.7	1.00	1.0	100.3	X		vhdl	1	kf532	N		N	Y	1K	16K						2013	2013		no trace of source code on web	
		forth-cpu	https://opencore	alpha	Richard Howe	forth	16	16	kintex-7-3	James Brakef		1858	6		9	149	##	14.7	0.67	1.0	53.8	X	Y	vhdl	11	top					64K	64K		21				2018			H2 Forth SoC, VHDL reads *.hex & *.bi	derived from J1, hex & bin files in 2/16/2018 tar
		ignite_ptsc		asic	George Shaw	forth	32	8												1.0				proprietary					N		4G	4G						1995	2002		ShBoom clone, fast ASIC with high cod	PTSC web site had full documentation
W	1	J1	www.excamera.	stable	James Bowman	forth	16	16	kintex-7-3	James Brakef		335	6		1	180	##	14.7	0.80	1.0	431.0	X		vhdl	1	j1	Y	forth	N		64K	64K		16			2	2006	2010	https://github.com/ja	uCode inst, dual port block RAM	16 deep data & return stacks
W	1	J1a	www.excamera.	stable	James Bowman	forth	16	16	kintex-7-3	James	DFF ex	518	6			412	##	14.7	0.80	1.0	636.1	X		verilog	3	j1	Y	forth	N		64K	64K		16			2	2006	2015		uCode inst, dual port block RAM	DFF used for 18 deep data & return stacks
		J1a32	www.excamera.	stable	James Bowman	forth	32	16	kintex-7-3	James	DFF ex	930	6			358	##	14.7	1.00	1.0	384.4	X		verilog	3	j1	Y	forth	N		64K	64K		16			2	2006	2015		uCode inst, dual port block RAM	DFF used for 18 deep data & return stacks
W	1	J1b	www.excamera.	stable	James Bowman	forth	32	16	kintex-7-3	James	DFF ex	2612	6			302	##	14.7	1.00	1.0	115.5	X		verilog	3	j1	Y	forth	N		64K	64K		16			2	2006	2015		uCode inst, dual port block RAM	DFF used for 32 deep data & return stacks
		J1b_16	www.excamera.	stable	James Bowman	forth	32	16	kintex-7-3	James	DFF ex	1588	6			355	##	14.7	1.00	1.0	223.4	X		verilog	3	j1	Y	forth	N		64K	64K		16			2	2006	2015		uCode inst, dual port block RAM	DFF used for 16 deep data & return stacks
		j1sc	https://github.co	spinalHDL	Steffen Reith	forth	32	16			no vhdl or verilog													scala/spi	11	j1												2017	2018		J1 reimplemented using Scala/Spinal to generate VHDL or Verilog	
W	1	jop	https://opencore	stable	Martin Schoeberl etal	forth	16	16	cyclone-1	Martin Schoe		2000	4			100		q10.0	0.67	1.0	33.5	I		vhdl	11	core	Y	yes	N		256K	256K						2004	2014		https://github.com/jop-devel/jop	java app builds some source code files
		kestrel-2	kestrelcomputer	stable	Samuel Falvo II	forth	16	16	kintex-7-3	James Brakef		735	6		8	172	##	14.7	0.67	1.0	157.2	X		verilog	27	M_kestre	Y	ues	N		64K	64K		16			2	2012	2015	https://hackaday.com	reimplementation of J1	M_j1a runs at 244MHz & 368 LUTs
W	1	microcore110	http://www.pldv	beta	Klaus Schleisiek	forth	12	8	kintex-7-3	James Brakef		399	6		1	294	##	14.7	0.40	2.0	147.4	X		vhdl	30	core	Y	asm	N	Y	512	2K						1999	2004	www.microcore.org/	indexing into return stack, auto inc/de	only one block RAM? simplest core
W		microcore120	http://www.pldv	beta	Klaus Schleisiek	forth	16	8	kintex-7-3	James Brakef		1101	6			168	##	14.7	0.67	2.0	51.1	X		vhdl	17	ucore	Y	asm	N	Y	4K	4K						1999	2004	www.microcore.org/	indexing into return stack, auto inc/de	no block RAM?, uses tri-state signals
X	1	msl16		beta	Philip Leong, Tsang, Le	forth	16	4	kintex-7-3	James Brakef		303	6			256	##	14.7	0.67	1.0	566.4	X		vhdl	13	cpu	Y	asm	N		256			16				2001			CPLD prototype	
W	1	myforthprocess	https://opencore	stable	Gerhard Hohner	forth	32	8	SP-kintex7-3	James Brakef		2959	6		6	223	##	14.7	1.00	1.0	75.3	X		vhdl	58	mycpu	Y	yes	N		64M	64M		96				2004	2012		DPANS'94 32-bit Forth, masters thesis,	25.15 Whetstones
		nc4016	https://en.wikich	asic	Chuck Moore	forth	16																	proprietary																	chapter in Koopman	
W	1	nige_machine	https://github.co	stable	Andrew Read	forth	32	8	kintex-7-3	James Brakef		5033	6	8	33	123	##	14.7	1.00	1.0	24.5	X		vhdl	29	Board	Y	yes	N		16M	16M		512		512			2014			standalone Forth system	https://www.youtube.com/watch?v=PRltE8q62
		nybbleForth	https://github.co	errors	Lars Brinkhoff	forth	16	4	kintex-7-3	James Brakef		missing	6				##	14.7	0.67	1.0				verilog	1	cpu	Y	yes			4K	4K	Y	11				2017			empty design, no init file	tiny
X		p16		alpha	Don Golding	forth	16	5	kintex-7-3	James	bad syntax		6					14.7	0.67	1.0				vhdl	1	p16			N		64K	64K						2000				
X	1	p16b		beta	C. H. Ting	forth	16	5	kintex-7-3	James	case c	367	6			355	##	14.7	0.67	1.0	648.1	X		vhdl	1	cpu16	Y	asm	N		64K	64K		28				2000			part of eForth?	data width can be expanded
X	1	p24e		beta	C. H. Ting	forth	24	6	spartan_3-5	James Brakef		1175	4		16	51	##	14.7	0.83	1.0	36.0	X		vhdl	1	p24c	Y	asm	N		2K	2K		28				2000			part of eForth?	data width can be expanded
		rtx2000	http://www.mpe	asic	Tom Hand	forth	16	16																proprietary																	Harris Corp., FPGA version at MPEforth	
		sc20	http://www.fort	proprietar	Brad Eckert	forth	32	8x	virtex-6	Brad Eckert		1977	6			150			1.00	1.0	75.9	X																				PDF file, Forth Inc.	
W	1	ssbcc	https://opencore	stable	Rodney Sinclair	forth	8	9	kintex-7	Rodney Sincla		196	6			474		14.7	0.33	1.0	797.9	ILX		verilog	3	core	Y	asm	N	Y	1K	8K	Y	41		3		2012	2014	https://github.com/si	Python program generates the Verilog	inst after branch/call/rtn always execs
		streamer16	http://www.ultr	stable	Myron Plichota	forth	16	3	kintex-7-3	James Brakef		143	6			417	##	14.7	0.20	1.2	485.6	X		vhdl	8	streamer	Y	yes	N	N	64K	64K	N	8	2			2001	2001	http://www3.sympat	MIPS/inst reduced	2nd web adr non-functional
X		x32	http://citeseerx.	stable	Sijmen Woutersen	forth	32	8	kintex-7-3	James	missing define		6				##	14.7	1.00	1.0				vhdl	32	core	Y	yes	N		4G	4G	Y					2006	2007	https://pdfs.semantic	MS thesis, byte code, needs caches	uses preprocessor on VHDL
		xpu	http://excamera	macros	James Bowman	forth	16	8	kintex-7-3	James	requres prepr		6					14.7	0.67	1.0				vhdl	1	c2a												2003	2003		predates J1	uses preprocessor on VHDL
W	1	yafc	https://github.co	alpha	Tim Wawrzynczak	forth	16		kintex-7-3	James Brakef		617	6		4	247	##	14.7	0.67	1.0	268.5	X		vhdl	20	cpu		asm	N	Y	8K	8K		26					2014				influenced by J1, F16 & C18
W	1	zpu	https://github.co	stable	Oyvind Harboe	forth	32	8	kintex-7-3	James Brakef		1073	6	3		283	##	14.7	1.00	4.0	65.9	X		vhdl	23	zpu_core	Y	yes	N		4G	4G	Y	37				2008	2009		zpu4: 16 & 32 bit versions, code size 80	ZPU the worlds smallest 32 bit CPU with GCC to
W	1	zpuino	http://alvie.com	alpha	Alvaro Lopes	forth	32	8	spartan_6-3	James Brakef		2547	6	4	12	126	##	14.7	1.00	4.0	12.3	X	Y	vhdl		papilio_pl	Y	yes	N		4G	4G	Y	37				2008	2012		SoC version of modified ZPU	pipelined, removed ucf file
		nyuzi_gpu	http://nyuzi.org/	stem veril	Jeff Bush	GPU	32	32	kintex-7-3	James Brakefield			6				##	14.7	1.00	1.0				system v	63	nyuzi	Y	yes								64						32 scalar & 32 vector reg
		igor	https://github.co	errors		lisp			kintex-7-3	James	missing files		6				##	14.7	0.33	1.0				vhdl	25	leval												2010	2010		IGOR - A microprogrammed LISP mach	two versions, spartan3 LUT4
		lispmicrocontro	http://nyuzi.org/	errors	Jeff Bush	lisp	32	32	kintex-7-3	James Brakef		missing	6				##	14.7	1.00	1.0				verilog	10	ulisp	Y		N													program.hex missing
A	1	t48	https://opencore	stable	Arnim Laeuger	MCS-48	8	8x	cyclone-1	Arnim Laeuge		738	4		1	59			0.33	4.0	6.6	IX		vhdl	70	t48_core	Y	asm	N		256	1K						2004	2009	MCS-48 data sheets	T48 uController	used in several projects
		brainfuckcpu	https://opencore	beta	Aleksander Maminski	mem	8	3	kintex-7-3	James Brakef		110	6			432	##	14.7	0.08	2.0	157.2	X		verilog	1	brainfuck_cpu			N	Y				8		0		2014	2015		Touring machine like	adj prog & data mem size, terrible name
		32-bit_MIPS		errors		MIPS	32		kintex-7-3	James	runs out of me		6	1			##	14.7	1.00	1.0				vhdl	18	mips_mo	Y	yes	N		4G	4G	Y			32		2011	2018		Cairo University EE dept	ISE runs out of memory (6GB)
A	1	aor3000	https://opencore	beta	Aleksander Osman	MIPS	32	32	kintex-7-3	James Brakef		5307	6	4	9	129	##	14.7	1.00	1.0	24.2	IX		verilog	19	aoR3000	Y	yes	N		4G	4G	Y			32	5	2014	2015		MIPS R3000A compatible, has MMU	moved declarations forward
X	1	edge	https://opencore	alpha	Hesham ALMatary	MIPS	32	32	spartan-6-3	James Brakef		5345	6	7	1	8	##	14.7	1.00	1.0	1.5	X		verilog	30	edge_cor	Y	yes	N	N	4G	4G	Y			32	5	2014	2014		Edge Processor (MIPS)	MIPS1 clone
		fpga4_mips_5p	http://www.fpga	errors	Van Loi Le	MIPS	32	32	kintex-7-3	James	degenerate de		6				##	14.7	1.00	1.0				verilog			Y	yes	N	N	4G	4G	Y			32	5	2017	2017		educational, full pipelined MIPS	incomplete
A	1	hf-risc	https://opencore	stable	Sergio Johann Filho	MIPS	32	32	kintex-7-3	James Brakef		1446	6		4	115	##	14.7	1.00	1.0	79.2	X		vhdl	9	spartan3e_n	Y	yes	N	N	4G	4G	Y	41		32		2016		https://github.com/si	MIPS I subset, no multiplier	
A	1	**ion**	https://opencore	mature	Jose Ruiz	MIPS	32	32	kintex-7-3	James Brakef		1533	6			163	##	14.7	1.00	1.0	106.0	IX		vhdl	12	mips_soc	Y	yes	N		4G	4G	Y			32		2011	2018	https://github.com/ja	new version: moving to MIPS32r1	new version not ready, keeping old numbers

		_uP_all_soft folder	opencores or prmary link	status	author	style / clone	data size	inst size	FPGA	reporter	comment	LUTs ALUT	LUT?	mults	blk ram	F max	date	tool ver	MIPS /inst	clks/ inst	KIPS /LUT	vendor	SOC	src code	# src files	top file	doc	tool chain	fltg pt	Hav	max data	max inst	byte adrs	# inst	adr mod	# reg	pipe len	start year	last revis	secondary web link	note worthy	comments
A	1	mais		stable	Rene Doss	MIPS	32	32	kintex-7-3	James	Brakef	2760	6	4	5	245	##	14.7	1.00	1.0	88.7	X		vhdl	22	MAIS_soc	Y	yes	N	N	4G	4G				32	5	2013		use MIPS tools	register forwarding around ALU	license req'd for commercial use
A		mips_fault_tole	https://opencore	stable	Lazaridis Dimitris	MIPS	32	32	kintex-7-3	James	Brakef	2017	6	4	6	45	##	14.7	1.00	1.0	22.5	X		vhdl	40	main	Y	yes	N		4G	4G	Y			32	5	2013	2013	MIPS data sheets	arithmetic includes fault detection	no external memory port?
		mips32	https://opencore	stable	Jin Jifang	MIPS	32	32	kintex-7-3	James	Brakef	3696	6		8	192	##	v17.4	1.00	1.0	52.0	X		verilog	17	pipelinem	Y	yes			4G	4G	y			32	5	2017			vivado project	"classic MIPS"
A	1	mips32r1	https://opencore	stable	Grant Ayers	MIPS	32	32	arria-2	James	Brakef	3716	A	8		79	##	q13.1	1.00	1.0	21.3	IX		verilog	20	processor	Y	yes	N	Y	4G	4G	Y			32	5	2012	2015	https://github.com/g	Harvard arch	complete software tool chain
A	1	mips789	https://opencore	stable	Li Wei	MIPS	32	32	kintex-7-3	James	Brakef	1432	6		1	171	##	14.7	1.00	1.0	119.1	IX		verilog	10	mips_cor	Y	yes	N		4G	4G	Y			32	5	2007	2014	MIPS data sheets	supports most MIPSI instructions	
		mipsfpga	https://www.mi	stable	MIPS Technologies	MIPS	32	32	atrix-7-3	James	did no	10221	6		14		##	14.7	1.00	1.0				verilog	166	m14k_top					4G	4G	Y			32		2014	2018	https://www.youtube	MIPS M14K core, Harris^2 uP course	did not infer LUT RAM, 483 IOs=> atrix, extensiv
		mips-lite	https://github.co	errorz	Jon Craton	MIPS	32	32	kintex-7-3	James	errors		6				##	14.7	1.00	1.0				vhdl	65	cpu		asm	N							32		2009	2009			
A	1	mipsr2000	https://opencore	stable	Lazaridis Dimitris	MIPS	32	32	kintex-7-3	James	Brakef	1971	6	4	6	71	##	14.7	1.00	1.0	36.2	X		vhdl	35	Dm	Y	yes	N		4G	4G	Y			32	5	2012	2016	MIPS data sheets	supports almost all instructions of mip	course project
		octagon	https://opencore	beta	Jon Pry	MIPS	32	32	kintex-7-3	James	Brakef	3021	6	4	9	333	##	14.7	1.00	1.0	110.2	X		vhdl	46	octagon		asm			4G	4G	Y			32		2015	2015	https://github.com/jd	8 thread barrel processor, largely MIPS compatible	
A	1	plasma	https://opencore	stable	Steve Rhoads	MIPS	32	32	kintex-7-3	James	Brakef	2462	6		3	97	##	14.7	1.00	1.0	39.5	X		vhdl	22	plasma	Y	yes	N		4G	4G	Y			32		2001	2013	MIPS data sheets	wide outside use, opencores page has	list of related publications
		plasma_fpu	https://opencore	stable	Maximilian Reuter	MIPS	32	32		James	errors																		Y		4G	4G	Y			32		2015	2015	MIPS data sheets	plasma with FPU	based on Plasma by Steve Rhoads
		r4000		untested	Michael Povlin	MIPS	32	32	kintex-7-3	James	Brakefield		6				##	14.7	1.00	1.0				verilog														1994			does not implement 64-bit data	Verilog output from Synplicity?
		sardmips	https://opencore	systemC	Igor Loi	MIPS	32	32																systemC			Y	yes	N		4G	4G	Y			32		2006	2009		synthesizable parametric IP core supporting	full MIPS R2000 ISA
W	1	sweet32	https://opencore	alpha	Valentin Angelovski	MIPS	32	16	kintex-7-3	James	Brakef	1050	6	1		142	##	14.7	1.00	1.0	135.1	X		vhdl	2	Sweet32_	Y	yes	N	N	4G	4G	Y	26		16		2014			no RAM	targets MACHXO2
A	1	ucore	https://opencore	stable	Whitewill	MIPS	32	32	kintex-7-3	James	Brakef	2469	6		1	231	##	14.7	1.00	1.0	93.5	X		verilog	25	ucore	Y	yes	N		4G	4G	Y			32	6	2005	2010	MIPS data sheets	MMU & caches	
A		yacc	https://opencore	stable	Tak Sugawara	MIPS	32	32	kintex-7-3	James	map e	2220	6	6			##	14.7	1.00	1.0		IX		verilog	10	yacc2	Y	yes	N		4G	4G	Y			32	5	2005	2009	MIPS data sheets	derived from, but independent of plas	YACC Yet Another CPU CPU
		yari	https://github.co	stable	Tommy Thorn	MIPS	32	32	kintex-7-3	James	Brakef	3610	6		15	189	##	14.7	1.00	1.0	52.3	X	Y	verilog	8	top					2M	2M				32		2004	2008		subset of MIPS R3000	
		ztapchip		altera dsg	Vuony Nguyen	MIPS	32	32	kintex-7-3	James	altera LPM pir		6				##	14.7	1.00	1.0		I	Y	vhdl	53	ztachip												2015	2015		multi-core with MIPS master	files no longer available, was under developmer
A	1	m1_core	https://opencore	beta	Fabrizo Fazzino, Albert	MIPS?	32	32	arria-2	James	Brakef	2101	A			190	##	q13.1	1.00	1.0	90.6	IX		verilog	9	m1_core		yes	N		4G	4G	Y			32		2007	2012		GCC target?	
W	1	dragonfly	http://www.leox	beta	LEOX team	MISC	16	16	kintex-7-3	James	Brakef	788	6			164	##	14.7	0.67	1.0	139.3	X		vhdl	6	dgf_core	Y		N		256	2K						2001			unusual, uses FIFOs	
A	1	fpgammix	https://github.co	stable	Tommy Thorn	MMIX	64	32	arria-2	James	Brakef	11605	A	8	10	94	##	q13.1	1.50	4.0	3.0	I		system v	3	core	Y	yes	Y	Y	16Q	16Q	Y	256		288		2006	2008	https://en.wikipedia.o	clone of Knuth's MMIX	micro-coded
		msp430_vhdl	https://opencore	beta	Peter Szabo	msp430	16	16	kintex-7-3	James	Brakef	1735	6			127	##	14.7	0.67	2.0	24.5	IX		vhdl	9	cpu_1	Y	yes	N		64K	64K	Y			16		2014	2017	msp430 data sheets	Comprehensive verification was not	compiles on cyclone II
A	1	neo430	https://opencore	alpha	Stephan Nolting	msp430	16	16	artiix-7	Stephan Nolt		442	6	1	2	190	##	14.7	0.67	8.0	36.0	IX		vhdl	19	neo430_t	Y	yes	N		28K	32K	Y			16		2015	2018	https://github.com/st	non-std IO, wishbone interface	~8+ clocks for R-R inst
A	1	neo430	https://opencore	alpha	Stephan Nolting	msp430	16	16	artiix-7	James	chang	947	6		2	203	##	14.7	0.67	8.0	17.9	IX	Y	vhdl	19	neo430_t	Y	yes	N		28K	32K	Y			16		2015	2018	https://github.com/st	edit neo430_sysconfig.vhd to set optic	~8+ clocks for R-R inst
A	1	openmsp430	https://opencore	stable	Oliver Girard	msp430	16	16x	stratix-3-2	Oliver Girard		1147	A	1		98			0.67	2.0	28.5	IX		verilog	30	openMSP	Y	yes	N	N	64K	64K	Y			16		2009	2014		near cycle accurate	performance spreadsheet
A	1	m32632	https://opencore	stable	Udo Moeller	N32032	8X	8X	kintex-7-3	James	Brakef	10167	6	19	16	83	##	14.7	1.00	1.0	8.2	IX		verilog	18	example	Y	yes	Y	Y	4G	4G	Y	200		24	3	2009	2016	http://cpu-ns32k.net/		17 VAX Mips at 35MHz
A	1	nios2		proprietar	Altera	Nios II	32	32	stratix-3	Altera	consis	1020	A			290	##	q13.1	0.90	1.0	255.9	I		proprietary			Y	yes	opt		4G	4G	Y			32		2004		NIOS2 data sheets	fltg-pt, caches & MMU options	Nios II/f: fastest version, DMIPS adj, 2.15 CoreM
A	1	nios2		proprietar	Altera	Nios II	32	32	stratix-5	Altera	consis	584	A			420	##	q16.0	0.10	1.0	71.9	I		proprietary			Y	yes	opt		4G	4G	Y			32		2004		NIOS2 data sheets	fltg-pt, caches & MMU options	Nios II/e: min LUTs version, DMIPS adj, 1.68 Cor
W	1	altor32	https://opencore	stable	Ultra Embedded	OpenRISC	32	32	kintex-7-3	James	Brakef	2505	6		5	192	##	14.7	1.00	1.0	76.8	ILX		system v	16	altor32	Y	yes	N	Y	4G	4G	Y					2012	2015		simplified OpenRISC 1000	xilinx S3 primitives
W	1	altor32_lite	https://opencore	stable	Ultra Embedded	OpenRISC	32	32	kintex-7-3	James	Brakef	1928	6			236	##	14.7	1.00	2.0	61.3	ILX		system v	7	altor32	Y	yes	N	Y	4G	4G	Y					2012	2014		simplified OpenRISC 1000, no pipeline	xilinx S3 primitives
W	1	minsoc	https://opencore	stable	Raul Fajardo etal	OpenRISC	32	32	kintex-7-3	James	Brakef	4945	6	4	8	107	##	14.7	1.00	1.0	21.7	ILX	Y	verilog	88	or1200_t	Y	yes	Y	M	4G	4G	Y			32		2009	2013	https://github.com/rk	minimal OR1200, vendor neutral, has	caches
W		mor1kx	https://github.co	stable	Julius Baxter	OpenRISC	32	32	kintex-7-3	James	Brakef	2718	6	3	3	217	##	14.7	1.00	1.0	80.0	X		verilog	48	mor1kx	Y	yes	N		4G	4G	Y			32		2012	2014	https://www.youtube	lots of configuration parameters	considered best openrisc design
		or1200	https://github.co	stable	Damjan Lampret	OpenRISC	32	32	kintex-7-3	James	Brakef	5231	6	4	8	118	##	14.7	1.00	1.0	22.5	X		verilog	78	or1200_t	Y	yes	Y	M	4G	4G	Y			32		2010	2015		best older openrisc implementation	no LUT RAM for reg file
W	1	or1200_hp	https://opencore	stable	Strauch Tobias	OpenRISC	32	32	virtex-5	Strauc	3 slot	5602	6			185	##		1.00	1.0	33.1	X		verilog	39	or1200_ic	Y	yes	Y	M	4G	4G	Y			32		2010	2013		3 slot barrel version of OR1200	numbers from published paper
		or1200_soc	https://opencore	beta	gaz	OpenRISC	32	32	cyclone-2	James	missing files		4				##	q11.1s	0.67	2.0			Y	verilog	39	top	Y	yes	Y	M	4G	4G	Y			32			2011		OpenRISC on Terasic DE1 board	
		or1200mp	https://github.co	stable	Stefan Wallentowitz	OpenRISC	32	32	kintex-7-3	James	Brakef	4960	6	4	8	111	##	14.7	1.00	1.0	22.4	X		verilog	104	or1200_t	Y	yes	Y	M	4G	4G	Y			32		2012	2012		multiprocessor variant, single core	
		or1k_soc	https://opencore	mature	Xianfeng Zeng	OpenRISC	32	32	kintex-7-3	James	altera primitiv		6				##	14.7	1.00	1.0		I	Y	verilog	194	or1k_soc	Y	yes			4G	4G	Y			32		2009	2010		SoC using OpenRISC 1200	huge tar file
		or1k-cf	https://opencore	alpha	Kenr	OpenRISC	32	32																confluence														2004	2009			
A	1	pdp1	https://opencore	alpha	Yann Vernier	PDP1	18	18	spartan-3a-	James	Brakef	1390	4		6	138	##	14.7	0.50	10.0	5.0	X		vhdl	15	top	Y	yes	N	N	4K	4K		28				2011	2017	http://pdp-1.compute	PDP-1 descended from MIT TX-0	uses Minimal UART from opencores
		ks10	http://www.tech	alpha	Rob Doyle	PDP10	36	36	spartan-6-2	Rob Doyle		4427	6		15	50	##	14.7	1.00	2.0	5.6	X		verilog	39	esm_ks10	Y	yes	Y	N			N					2011	2014		36-bit accum & 18-bit adrs	ucf file, most tests pass
A	1	pdp11-34verilo	www.heeltoe.co	stable	Brad Parker	PDP11	16	16x	arria-2	James	Brakef	2532	A			126	##	q13.1	0.67	2.0	16.7	IX	Y	verilog	24	pdp11	Y	yes	N	N	64K	64K				8		2009		PDP11 data sheets	boots & runs RT-11, EIS inst & MMU	
A	1	pdp2011	http://pdp2011.s	stable	Sytse van Slooten	PDP11	16	16x	kintex-7-3	James	Brakef	5060	6	1		205	##	14.7	0.67	2.0	13.6	IX	Y	vhdl	3	cpu	Y	yes	Y	N	64K	64K				8		2008	2014	PDP11 data sheets	SoC, build files for A&X boards	
		pop11-40	http://www.ip-a	simulation	Naohiko Shimizu	PDP11	8x	16X	ep1K	Naohiko Shim		2687	4			20	##					I		NSL	17	top	Y	yes		N	64K	64K	Y			8		2009		www.ip-arch.jp/index	Boots UNIX	various papers, no verilog or vhdl
A	1	w11	https://opencore	alpha	Walter Mueller	PDP11	16	16x	kintex-7-3	James	Brakef	1760	6	1	1	147	##	14.7	0.67	2.0	28.0	X	Y	vhdl	118	pdp11_co	Y	yes	N	N	4M	4M	Y			8		2010	2013	PDP11 data sheets	Boots UNIX, has MMU & cache, retro p	PDP-11/70 CPU core and SoC
A	1	pdp8	https://opencore	alpha	Joe Manojlovick, Rob D	PDP8	12	12	kintex-7-3	James	Brakef	1219	6	1		183	##	14.7	0.50	2.0	37.5	X	Y	vhdl	55	cpu	Y	yes	N	N	32K	32K				8		2012	2013	PDP8 data sheets	PDP-8 Processor Core and System	Boots OS/8, runs apps, several variants
A	1	pdp8l	https://opencore	beta	Ian Schofield	PDP8	12	12	cyclone-3	James	Brakef	1088	4		48	63	##	q13.1	0.50	2.0	14.4	I		vhdl	11	top	Y	yes	N	N	4K	4K						2013	2013	PDP8 data sheets	Minimal PDP8/L implementation with	4K disk monitor system
A	1	pdp8verilog	www.heeltoe.co	stable	Brad Parker	PDP8	12	12	kintex-7-3	James	Brakef	505	6			366	##	14.7	0.50	2.0	181.3	X		verilog	18	pdp8	Y	yes	N	N	32K	32K				8		2005	2010	PDP8 data sheets	boots & runs TSS/8 & Basic	
A	1	synpic12		stable	Miguel Angel Ajo Pelay	PIC12	8	12	kintex-7-3	James	Brakef	474	6		1	197	##	14.7	0.33	1.0	136.8	IX		vhdl	7	synpic12	Y	yes	N	N	256	2K	Y					2011	2011	http://projects.nbee.o	CHDL to verilog	bad weblink
X	1	altium/TSK165x	http://techdocs.	proprietar	Altium	PIC16	8	12	spartan-3-5	Altium		416	4			50			0.33	2.0	19.8	AILX		proprietary			Y	yes	N	Y	256	4K	Y					2004	2017	CR0140.pdf, CR0114.p	frozen, asm, C, C++, schem, VHDL & Ve	default clock speed is 50MHz
B		cqpic	http://www002.	stable	Sumio Morioka	PIC16	8	14	arria-2	James	ROM paramet		A				##	q13.1	0.67	1.0		I		vhdl & v	5	CQPIC	Y	yes	N	Y	256	4K	Y					1999	2004	PIC16 data sheets	LPM macros	
A	1	free_risc8	https://web.arch	stable	Thomas Coonan	PIC16	8	14	kintex-7-3	James	Brakef	355	6			142	##	14.7	0.33	1.0	132.2	X		verilog	8	cpu	Y	yes	N		256	4K	Y					2002	2011	https://web.archive.org/web/20120309123835/http://www.mindspring.com/~tcoonan/index.html		
A	1	m16c5x	https://opencore	mature	Michael Morris	PIC16	8	14	spartan-3-4	Michael Mor		1217	4		3	60	##		0.33	1.0	16.3	X	Y	verilog	3	m16C5x	Y	yes	N	Y	256	4K	Y					2013	2014		SOC LUT count	core at P16C5X
A	1	minirisc	https://opencore	stable	Rudolf Usselmann	PIC16	8	14	spartan-3	Rudolf Usselr		460	4			80			0.33	1.0	57.4	X		verilog	7	risc_core_	Y	yes	N	Y	256	4K	Y					2001	2012	PIC16 data sheets		
A	1	p16c5x	https://opencore	mature	Michael Morris	PIC16	8	14	kintex-7-3	James	Brakef	378	6			252	##	14.7	0.33	1.0	220.2	IX		verilog	3	P16C5x	Y	yes	N	Y	256	4K	Y					2013	2014	PIC16 data sheets		
B	1	pic_coonan		alpha	Tom Coonan	PIC16	8	14	kintex-7-3	James	Brakef	328	6		1	165	##	14.7	0.33	1.0	166.1	X		verilog	7	piccpu	Y	yes	N	Y	256	4K	Y					1999				risc8 by Tom Coonan also a PIC uP
		pic-16c5x	https://tams-ww	errors	Ernesto Romani	PIC16	8	12	kintex-7-3	James	std library pro		6				##	14.7	0.33	2.0				vhdl	16	pic_core	Y	yes	N	Y	256	4K	Y					1998	2002			as part of thesis?
A		ppx16	https://opencore	stable	Daniel Wallner	PIC16	8	14	kintex-7-3	James	missin	409	6			238	##	14.7	0.33	1.0	192.1	X		vhdl	10	P16C55	Y	yes	N	Y	256	4K	Y					2002	2009	PIC16 data sheets	both 16C55 & 16F84	with fake instruction ROM
A		recore54		beta	Hans Tiggeler	PIC16	8	14	kintex-7-3	James	Cannot find <r		6					14.7	0.33	1.0				vhdl	20	rcore54_s	Y	yes	N	Y	256	4K	Y					1999		PIC16 data sheets	not available at ht-lab website	www.ht-lab.com
A	1	risc16f84	https://opencore	stable	John Clayton	PIC16	8	14	kintex-7-3	James	Brakef	373	6			359	##	14.7	0.33	2.0	158.9	IX		verilog	1	risc16f84	Y	yes	N	Y	256	4K	Y					2002	2014	PIC16 data sheets	derived from CQPIC by Sumio Morioka	
A		risc5x	https://opencore	stable	MikeJ	PIC16	8	14	kintex-7-3	James	RLOC constrai		6					14.7	0.33	1.0				vhdl	15	cpu	Y	yes	N	Y	256	4K	Y					2002	2011	PIC16 data sheets	makes extensive use of xilinx primitives	
		risc8	https://web.arch	stable	Tom Coonan	PIC16	8	12	kintex-7-3	James	Brakef	355	6			154	##	14.7	0.33	2.0	71.5	X		verilog	8	cpu	Y	yes	N	Y	256	2K	Y					1999	1999	https://github.com/b	excellent HTML doc	directory contains derivative design by another
A	1	ae18	https://opencore	beta	Shawn Tan	PIC18	8	16	arria-2	James	Brakef	1084	A	1		207	##	q13.1	0.33	1.0	63.1	ILX		verilog	1	ae18_core		yes	N	Y	4K	1M						2003	2009	https://hackaday.io/p	not 100% compatable	negative edge reset "clock"
A	1	mcip_open	https://opencore	beta	Mezzah Jbrahim	PIC18	16	24	kintex-7-3	James	Brakef	881	6	1		200	##	14.7	0.67	1.0	152.1	X		vhdl	23	MCIOopen_	Y	yes	N	Y	4K	1M	Y					2014	2015		light version of PIC18	
A	1	copyblaze	https://opencore	stable	Abdallah Ellbrahimi	picoBlaze	8	18	kintex-7-3	James	missin	622	6			217	##	14.7	0.33	2.0	57.5	IX		vhdl	16	cp_copyb	Y	asm	N		256	2K	Y					2011	2016		wishbone extras	
		nanoblaze	https://opencore	beta	Francois Corthay	picoBlaze	8	18	kintex-7-3	James	Brakef	247	6		1	169	##	14.7	0.33	2.0	113.2	X		vhdl	12	nanoblaze		asm			256	2K	Y					2015	2015		nanoBlaze compatable, adjustable data width	
		nanoblaze	https://opencore	beta	Francois Corthay	picoBlaze	8	18	kintex-7-3	James	punctuation		6				##	14.7	0.33	2.0		X		vhdl	12	nanoblaze		asm			256	2K	Y					2015	2015		nanoBlaze compatable, adjustable data width	
A	1	pacoBlaze	www.bleyer.org	mature	Pablo Kocik	picoBlaze	8	18	spartan-3	Pablo Kocik		177	4		1	117			0.33	2.0	109.1	X		verilog	18	pacoblaze	Y	asm	N		256	2K	Y	57			2		2006		3 versions, behavioral coding	
A	1	picoblaze	https://www.xili	stable	Ken Chapman	picoBlaze	8	18	spartan-3-4	James	Brakef	178	4		1	182	##	14.7	0.33	2.0	168.9	X		vhdl	1	kcspm3	Y	asm	N		256	2K	Y					2003		https://en.wikipedia.o	2 clocks/inst, no prog ROM	this is the original picoBlaze author
A	1	picoblaze	https://www.xili	stable	Ken Chapman	picoBlaze	8	18	kintex-7-3	James	Brakef	317	6		2	195	##	14.7	0.33	2.0	101.6	X	Y	vhdl	19	kc705_kc	Y	asm	N		256	2K	Y					2003		https://en.wikipedia.o	2 clocks/inst	this is the original picoBlaze author
A	1	picoblaze	https://www.xili	stable	Ken Chapman	picoBlaze	8	18	kintex-7-3	James	Brakef	110	6		2	217	##	14.7	0.33	2.0	325.5	X		vhdl	1	kcspm6	Y	asm	N		256	2K	Y					2003		https://en.wikipedia.o	2 clocks/inst, no prog ROM	this is the original picoBlaze author
		riscuva1	https://www.scr	stable	S. de Pablo	picoBlaze	8	14	kintex-7-3	James	Brakef	109	6			370	##	14.7	0.33	2.0	560.7	X		verilog	1	riscuva1	pme		N	Y	256	1K	Y	35				2006	2006	https://github.com/b	Verilog source included in PDF file	also VHDL version by Bikash Gogoi with identica
		wb4pb	https://opencore	stable	Stefan Fischer	picoBlaze	13	13	kintex-7-3	James	incomplete pc		6				##	14.7	0.33	3.0			Y	vhdl or v	14	picoblaze_wb_uart				Y								2010	2013	https://en.wikipedia.o	software addon for picoBlazeSoftware	ported to kcpsm6
		wb4pb	https://opencore	stable	Stefan Fischer	picoBlaze	13	13	spartan-3	Stefan Fische		309	4		1	102	##	14.7	0.33	3.0	36.2	X	Y	vhdl or v	14	picoblaze_wb_uart				Y								2010	2013	https://en.wikipedia.o	software addon for picoBlazeSoftware	kcpsm3 only works for Spartan 3

		_uP_all_soft folder	opencores or prmary link	status	author	style / clone	data size	inst size	FPGA	reporter	comment	LUTs ALUT	LUT?	mults	blk ram	F max	date	tool ver	MIPS /inst	clks/ inst	KIPS /LUT	vendor	SOC	src code	# src files	top file	doc	tool chain	fltg pt	Hav	max data	max inst	byte adrs	# inst	adr mod	# reg	pipe len	start year	last revis	secondary web link	note worthy	comments
W	1	Lutiac		custom	David Galloway, David	reg	16	NA	stratix-4	David Gallow		140	A	4		198			0.67	1.0	947.6	I		vhdl & verilog								64	N	64		32	3		2010	Talks at Un. Toronto	synthesis maps PC into ucode	no inst mem: small state machine, ~200 inst opt
W	1	octavo	http://fpgacpu.c	beta	Charles LaForest	reg	16	16	stratix-4	Charles LaFor		500	A	1		550			0.67	1.0	737.0	I		verilog	18	Octavo	Y	asm	N					14		16	10		2012	Octavo: an FPGA-Cen	8 core barrel, adjustable data width	~= performance across word sizes, no call/rtn in
		8bit_piped_pro	https://opencore	stable	Mahesh Sukhdeo Palve	RISC	8	16	kintex-7-3	James	swapp	1049	6		1	370	##	14.7	0.33	1.0	116.4	X		verilog	28	top	Y							20		16		2013	2017	https://github.com/freecores/instruction_list_pipelined_pro	no ROM file, see top.v line 143	
		a_tiny_up	https://www.qu	errors	Chuck Thacker	RISC	32	32	kintex-7-3	James	missing const	6						14.7	0.67	1.0				verilog	1	tinycomp	Y		N	Y	1K	1K	N	13		128		2007	2007	https://www.cl.cam.a	104 lines of verilog	regs in block RAM, ttc.sv has simple clocking
		a2z	https://hackada	stable		RISC	16	24	cyclone-4	James	Brakef	1524	4	1	12	62	##	q17.0	0.67	1.0	27.4	I		verilog		top_a2z													2016			
		a2z	https://hackada	errors		RISC	16	24	kintex-7-3	James	replace Altera	6						14.7	0.67	1.0		I		verilog															2016		runs on Cyclone IV	
		aap	https://github.co	altera dsg	Simon Cook	RISC	16	16	kintex-7-3	James	altera design	6					##	14.7	0.67	1.0		I		verilog	7	execute	Y	yes		Y	64K	16M	Y			64		2015	2016	http://www.embecos	includes Altera project	4 to 64 reg, 24-bit pc, no status reg
		aap	https://github.co	stable	Simon Cook	RISC	16	16	cyclone-4	James	Brakef	10630	4			306	##	q17.0	0.67	1.0	19.3	I		verilog	7	de0_nanc	Y	yes		Y	64K	16M	Y			64		2015	2016	http://www.embecos	includes Altera project	4 to 64 reg, 24-bit pc, no status reg
X	1	aizup/aizup_mi	instruct1.cit.corr	stable	Yamin Li, Wanming Chu	RISC	8	16	arria-2	James	Brakef	121	A			298	##	q13.1	0.17	2.0	205.4	IX		vhdl	1	cpu			N	N	64K	64K		16		4		1996	1998		used in Cornell EE475 course	MIPS/inst reduced due to few inst
X		aizup/aizup_ov	instruct1.cit.corr	stable	Yamin Li, Wanming Chu	RISC	8	16	kintex-7-3	James	Brakef	138	6			318	##	14.7	0.17	3.0	128.3	IX		vhdl	1	cpu		asm	N	N	64K	64K	Y	16		4		1996	1998		used in Cornell EE475 course	MIPS/inst reduced due to few inst
X		aizup/aizup_pip	instruct1.cit.corr	stable	Yamin Li, Wanming Chu	RISC	8	16	kintex-7-3	James	Brakef	198	6			375	##	14.7	0.17	2.0	157.9	IX		vhdl	1	cpu		asm	N	N	64K	64K	Y	16		4		1996	1998		used in Cornell EE475 course	MIPS/inst reduced due to few inst
X		aizup/aizup_se	instruct1.cit.corr	stable	Yamin Li, Wanming Chu	RISC	8	16	kintex-7-3	James	Brakef	136	6			313	##	14.7	0.17	8.0	48.1	IX		vhdl	1	cpu		asm	N	N	64K	64K	Y	16		4		1996	1998		used in Cornell EE475 course	MIPS/inst reduced due to few inst
W	1	altium/TSK3000	http://techdocs.p	proprietar	Altium	RISC	32	32	spartan-3-5	Altium		2426	4		4	50			1.00	1.0	20.6	AILX		proprietary			Y	yes	N	N	4G	4G	Y					2004	2017	CR0140.pdf, http://te	frozen, asm, C, C++, schem, VHDL & Ve	default clock: 50MHz, opt mult/div
W	1	alwcpu	https://opencore	alpha	Andreas Hilvarsson	RISC	16	16	kintex-7-3	James	Brakef	377	6			194	##	14.7	0.67	1.0	345.5	ILX		vhdl	7	top	ome		N	N	64K	64K	Y			16		2009	2010		lightweight CPU	maximal features
W	1	atlas_2K	https://opencore	beta	Stephan Nolting	RISC	16	16	kintex-7-3	James	Brakef	1595	6	1	5	151	##	14.7	0.80	1.0	75.9	ILX		vhdl	19	ATLAS_2K	Y	asm	N	Y	64K	64K	M	80		8		2013	2015		ARM thumb like inst set	has MMU & full SOC features
W	1	atlas_core	https://opencore	beta	Stephan Nolting	RISC	16	16	kintex-7-3	James	Brakef	559	6	1		200	##	v14.1	0.80	1.0	286.2	IX		vhdl	8	ATLAS_CF	Y	asm	N	Y	64K	64K	Y	80		8		2013	2015		ARM thumb like inst set	non-MMU version
		babyrisc	http://www.sand	stable	John Rible	RISC	8	16	kintex-7-3	James	Brakef	468	6			141	##	14.7	0.33	2.0	49.7	X		verilog	1	qs5_mix	Y		N		64K	64K	Y	15		8		1997	1999	http://www.sandpipe	part of a three class course	memory rd/wt & ALU per clock
		bst-cpu	https://github.co	altera dsg	Yichun Ma	RISC	32	32	kintex-7-3	James	inserted infer	6					##	14.7	1.00	1.0		I		verilog		pl_computer			N		4G	4G				32		2016	2016		learning, pipeline uP	
		bst-cpu	https://github.co	altera dsg	Yichun Ma	RISC	32	32			altera LPM pimitives											I		verilog		sc_computer			N		4G	4G				32		2016	2016		learning, single cycle uP	
		c16too	https://www.scr	stable	Cole Design and Develo	RISC	16	16	kintex-7-3	James	Brakef	510	6			271	##	14.7	0.67	4.0	88.9	X		vhdl	1	core	Y	asm	N		64K	64K	N	20		8		2003		coledd.com/electroni	graphics capability	clock/2 and six phases
		carpe	https://github.co	simulation	Peter Gavin	RISC	32	32	kintex-7-3	James	Brakefield		6				##	14.7	1.00	1.0				vhdl	227		Y												2014		http://ww2.cs.fsu.edu	no top module	https://github.com/pgavin/
W	1	cast_ba22	http://www.cast	proprietar	CAST Inc	RISC	32	16x	spartan-6	CAST Inc		1800	6		32	72			1.00	1.0	40.0	X		proprietary			Y	yes			4G	4G				32				http://www.cast-inc.c	Cast has uP related IP	several versions, FPGA kits
		c-nit	http://www.c-ni	stable	Sumit	RISC	16	16	spartan-3-5	James	xilinx l	752	4		3	100	##	14.7	0.67	2.0	44.5	X		verilog	6	soc	om	asm	N	N	64K	64K	Y	22		15		2003	2004		RISC with several load/store modes	
X	1	cole_c16	https://www.scr	beta	Cole Design & Develop	RISC	16	16	spartan-6-3	James	Brakef	554	6			298	##	14.7	0.67	7.0	51.4	X		vhdl	1	core	Y	asm	N		64K	64K	N	20		8		2002	2012		(7) clks per inst, complete SOC	for teaching
		cowgirl	https://opencore	beta	Thebeekeeper	RISC	16	16	kintex-7-3	James	empty design	6						14.7	0.67	1.0				vhdl	14	cowgirl						64K				8		2006	2009		ISE reduces design to zero	
		cpugen	https://opencore	stable	Giovanni Ferrante	RISC	32	16	kintex-7-3	James	Brakef	474	6			192	##	14.7	0.67	1.0	271.8	IX		vhdl	14	cpu	Y	asm	N	N								2003	2009		x86 .exe generates VHDL RISC uP	using 16 bit example
		cpugen	https://opencore	stable	Giovanni Ferrante	RISC	32	16	kintex-7-3	James	Brakef	1597	6	8		154	##	14.7	1.00	1.0	96.3	IX		vhdl	14	cpuc	Y	asm	N	N								2003	2009		x86 .exe generates VHDL RISC uP	using 32 bit example
W	1	dcpu16	https://github.co	beta	Shawn Tan, Marcus Pe	RISC	16	16	kintex-7-3	James	Brakef	662	6	1		318	##	14.7	0.67	4.0	80.4	X		vhdl & v	5	dcpu16_c	Y	asm	N	N	64K	64K	N	37		8		2009	2012	https://en.wikipedia.c	for the 0X10c game	4+ addressing modes, 4 & 5-bit reg /modefields
W	1	dgb16	see FISA64	stable	Robert Finch	RISC	16	16	kintex-7-3	James	Brakef	780	6			313	##	14.7	0.67	1.0	269.0	X		verilog	1	dbg16	Y		N	Y						8				https://github.com/rc	inside FISA64 project	debug uP for fisa64
X	1	diogenes	https://opencore	beta	Fekknhifer	RISC	16	16	kintex-7-3	James	Brakef	807	6		1	297	##	14.7	0.67	1.0	246.3	X		vhdl	11	cpu	Y	asm	N			1K						2008	2009		"student RISC system"	
		dp32		errors	Peter Ashenden	RISC	32	32	kintex-7-3	James	errors	6					##	14.7	1.00	1.0				vhdl												32		2001	2001	book, CDROM	from The Designers Guide to VHDL	timing delays in source code
X	1	eco32	https://opencore	stable	Hellwing Geisse	RISC	32	32	kintex-7-3	James	Brakef	2339	6		1	160	##	14.7	1.00	1.5	45.5	ILX	Y	verilog	14	cpu	Y	yes	N		512M	256M	Y	61		32		2003	2014	homepages.thm.de/~	MIPS like, slow mul & div	
X	1	eco32	https://opencore	stable	Hellwing Geisse	RISC	32	32	kintex-7-3	James	Brakef	3367	6		5	147	##	14.7	1.00	1.5	29.1	ILX	Y	verilog	24	eco32	Y	yes	N		512M	256M	Y	61		32		2003	2014	homepages.thm.de/~	MIPS like, slow mul & div	
X		eight_bit_uc		stable	Synplicity	RISC	8	12	kintex-7-3	James	signal/variable	6						14.7	0.67	1.0				vhdl	10	eight_bit_uc						2K	Y			32		2000	2000		part of Amplify documentation	
		ejrh_cpu	https://github.co	stable	Edmund Horner	RISC	16	16	kintex-7-3	James	Brakef	928	6	1	2	196	##	14.7	0.67	1.0	141.6	X		verilog	17	machine	Y									16		2015	2015		see web archive for doc	
X	1	erp	https://opencore	stable	Shahzadjk	RISC	8	16	spartan-3-5	James	Brakef	366	4	1	1	70	##	14.7	0.33	1.0	63.5	X		verilog	1	ERPverilo	Y							15		6		2004	2014		two report PDFs & one Verilog file	
W	1	fisa32	https://github.co	beta	Robert Finch	RISC	32	32	kintex-7-3	James	Brakef	3479	6	3	2	152	##	14.7	1.00	1.0	43.7	X		verilog	1	FISA32	Y		N	Y						32		2014	2014	https://github.com/robfinch/Cores		
W	1	fisa64	https://github.co	beta	Robert Finch	RISC	64	32	kintex-7-3	James	Brakef	10404	6	12	7	65	##	14.7	1.50	1.0	9.4	X		verilog	1	FISA64	Y		N	Y								2015	2015	https://github.com/robfinch/Cores		need to use multi-cycle on mult
W	1	fluid_core	https://opencore	alpha	Azmathmoosa	RISC	8x	12	kintex-7-3	James	Brakef	956	4			381	##	14.7	0.33	1.0	131.7	X		verilog	17	FluidCore			N	Y						8		2015	2015		data width adj., mem sizes adj.	
		fpag4_risc16_1	http://www.fpga	errors	Van Loi Le	RISC	16	16	kintex-7-3	James	degenerate de	6					##	14.7	0.66	1.0				verilog	15	Risc_16_b	Y	no	N	Y	64K	64K		13	4	16		2017	2017		similar to mips16_16_1cycl	incomplete Risc_16_bit module
		fpga4_mips16	http://www.fpga	stable	Van Loi Le	RISC	16	16	kintex-7-3	James	Brakef	369	6			200	##	14.7	0.67	1.0	363.1	X		verilog	8	mips_16			N		65K	65K		13		8		2017	2017		educational, no block RAM inferred	same prog & data mem and alu as mips16_16_v
		fpga4_mips16_	http://www.fpga	stable	Van Loi Le	RISC	16	16	kintex-7-3	James	Brakef	352	6			213	##	14.7	0.67	1.0	405.0	X		vhdl	8	mips_vhdl			N		65K	65K		8		8		2017	2017		educational, no block RAM inferred	actual prog sz=16, actual data mem sz=256
W	1	gumnut	http://digitaldes	stable	Peter Ashenden	RISC	8	18	kintex-7-3	James	Brakef	388	6			259	##	14.7	0.33	1.0	220.7	IX		verilog	6	gumnut-r	Y	asm	N	Y	256	4K	Y			8		2007			see Digital Design: An Embedded Systems Approach Using VHDL	
X		hicovec	https://opencore	beta	Harald Manske, Gundo	RISC	32	32	kintex-7-3	James	compiler error	6						14.7	1.00	1.0				vhdl	28	cpu	Y	asm	N				Y					2008	2010		hybrid scalar & vector processor	
X	1	hpc-16	https://opencore	beta	Umair Siddiqui	RISC	16	16	kintex-7-3	James	Brakef	871	6			152	##	14.7	0.67	1.0	116.6	X		vhdl	20	cpu	Y	asm	N		64K	64K				16		2005	2015			
X	1	iDEA	https://github.co	alpha	Hui Yan Cheah etal	RISC	16	32	virtex-6	Liu Che	unable	321	6	1	2	405		13.2	0.67	1.0	845.3	X		verilog	22	cpu_top	Y	yes	N	Y	64K	64K	N	24		32	9	2011	2016	The iDEA DSP Block Ba	uses DSP slice in barrel mode for ALU	from GitHub, rq'd NOPs lower actual results
X	1	jam	https://github.co	stable	Johan Thelin etal	RISC	32	32	kintex-7-3	James	Brakef	1369	6			143	##	14.7	1.00	1.0	104.2	X		vhdl	17	cpu	Y		N	Y	128K	128K				32	5	2002	2014		serial multiply & divide	
X	1	jam	https://github.co	stable	Johan Thelin etal	RISC	32	32	kintex-7-3	James	Brakef	1396	6			159	##	14.7	1.00	1.0	113.7	X		vhdl	17	cpu_sys	Y		N	Y	128K	128K				32	5	2002	2014		serial multiply & divide	took out clock divider
W	1	jane_nn		stable	Suresh Devanathan	RISC	4	8	kintex-7-3	James	Brakef	723	6			178	##	14.7	0.33	1.0	81.4	X		vhdl	3	Processor	Y							27		16		2002			neural network microprocessor, specialized registers	
		jca		stable	John Cronin	RISC	8	32	kintex-7-3	James	replac	3287	6	3	3	157	##	14.7	0.33	1.0	15.8	IX	Y	verilog	17	soc										16					has VGA controller, plays Pong	altera memories
X		jpu16	https://github.co	stable	Joksan Alvarado	RISC	16	26	kintex-7-3	James	missing RAM f	6						14.7	0.67	1.0				vhdl	9	JPU16	Y	asm	N		64K	64K				16		2012			32 deep call stack, 8 addressing modes	
		klc32	https://opencore	planning	Robert Finch	RISC	32	32	kintex-7-3	James	Brakef	3790	6	4	1	200	##	14.7	1.00	4.0	13.2	X		verilog	25	KLC32	Y		N		4G	4G	Y			32		2011	2012	https://github.com/rc	single ported block RAM register file :(	heavy use of includes
		kpu	https://github.co	alpha	Andrea Corallo	RISC	32	32	kintex-7-3	James	missin	6178	6	3		19	##	14.7	1.00	1.0	3.0	X	Y	verilog	19	kpu	Y	yes	N	Y	4G	4G				32		2016	2018	http://andreacorallo.i	KPU is a minimal system on chip written	used as testbench for the KPU core
W	1	latticemicro32	http://www.latti	stable	Yann Siommeau, Micha	RISC	32	32	arria_2	James	Brakef	2166	A	4	30	149	##	q13.1	0.80	1.0	55.0	LX		verilog	24	lm32_cpu	Y	yes	N		4G	4G	Y			32		2006	2012	https://en.wikipedia.c	optional data & inst caches	
W	1	latticemicro8	http://www.latti	stable	Lattice Semiconductor	RISC	8	18	LFE2	Lattice Semic		265	4		1	104			0.33	2.0	64.4	ILX		vhdl	10	isp8_core	Y	yes	N		256	4K	Y			32		2005	2010	https://en.wikipedia.c	16 deep call stack, four configurations	
W	1	lxp32	https://opencore	beta	Alex Kuznetsov	RISC	32	32	kintex-7-3	James	Brakef	850	6	3	1	196	##	14.7	1.00	2.0	115.4	AIX		vhdl	20	lxp32u_tc	Y	asm	N	N	4G	4G	Y	30		256	3	2016			register file in block RAM	vendor neutral source code, no div inst
X		manik	https://www.dsp	stable	Sandeeo Dytta	RISC	32	32	kintex-7-3	James	needs editing	6						14.7	0.33	1.0				vhdl	45	manik2to	Y	yes	N		4K	4K	Y			16		2002	2006	www.niktech.com/	optional data & inst caches	supports Xilinx, Altera, Actel, Lattice; broken we
X	1	marca	https://opencore	stable	Wolfgang Puffitsch	RISC	16	16	arria-2	James	Brakef	1763	A		22	157	##	q13.1	0.67	6.0	10.0	I		vhdl	40	marca	Y		N		8K	16K		75		16	4	2007	2009		serial multiply & divide	clks/inst is approx
A	1	minimips	https://opencore	stable	Poppy etal	RISC	32	32	kintex-7-3	James	Brakef	2939	6	8		118	##	14.7	1.00	1.0	40.1	X		vhdl	12	minimips	Y	yes	N	N	4G	4G				32	5	2004	2009	MIPS I	based on MIPS I	
B		mips_16	https://opencore	stable	Doyya Doyya	RISC	16	16	kintex-7-3	James	collapsed in co	6						14.7	1.00	1.0				verilog	12	mips_16_	Y		N		64K	64K		13		8	5	2012	2013		Educational 16-bit MIPS Processor	
		misoc	https://github.co	stable	M-Labs	RISC	32	32	arria_2		python source code run thru migen						##	q13.1	0.80	1.0				V*HDL			Y	yes	N		4G	4G	Y			32		2007	2015	https://m-labs.hk	Video IP for Mist & others	choice of latticemicro32 or mor1kx uP
		mist1032e10fa	https://github.co	stem veril	Takahiro Ito	RISC	32	32	kintex-7-3	James	system verilog	6					##	14.7	1.00	1.0				system verilog												64			2014		mist32 uP, three versions: inorder, out of order & embedded uPs	
		mist1032isa	https://github.co	errors	Takahiro Ito	RISC	32	32	kintex-7-3	James	errors	6					##	14.7	1.00	1.0				verilog												64			2015		mist32 uP, three versions: inorder, out of order & embedded uPs	
		mist1032sa	https://github.co	errors	Takahiro Ito	RISC	32	32	kintex-7-3	James	errors	6					##	14.7	1.00	1.0				verilog												64			2014		mist32 uP, three versions: inorder, out of order & embedded uPs	
		moxie	https://github.co	altera dsg	Anthony Green	RISC	32	32	kintex-7-3	James	four read, two	6					##	14.7	1.00	1.0				verilog	16	moxie					4G	4G	Y			16		2009	2017	https://github.com/atgreen/moxie-cores		Altera IP: four read, two write register file
		moxielite	https://github.co	stable	Anthony Green	RISC	32	32	kintex-7-3	James	Brakef	3159	6	3		152	##	14.7	1.00	1.0	48.0	X		vhdl	11	moxielite					4G	4G	Y			16		2009	2017	https://github.com/atgreen/moxie-cores		
X	1	myrisc1		stable	Muza Byte	RISC	8	8	arria-2	James	Brakef	121	A		2	231	##	q13.1	0.33	1.0	628.7	I		verilog	1	myRISC1	Y		N	Y	256	256	Y	16		4		2011	2011		Verilog source included in PDF file	LPM macros
W	1	natalius_8bit_r	https://opencore	beta	Fabio Guzman	RISC	8	16	kintex-7-3	James	Brakef	232	6		1	175	##	14.7	0.11	3.0	27.7	X		verilog	12	natalius_l	Y	asm	N	Y	256	2K	Y	29		8		2012	2012		return stack & register file	3 clocks/inst
		niloofar1	http://ce.sharif.e	errors	Mahdi Amiri	RISC	16	16	kintex-7-3	James	ran out of me	6					##	14.7	0.67	1.0				verilog	3	nf1	Y														derived from risc-16	ASIC, uses Leonardo for synthesis
W	1	nocpu	https://github.co	beta	John Tzonevrakis	RISC	8	8	kintex-7-3	James	Brakef	175	6			243	##	14.7	0.33	1.5	306.1	X		verilog	5	cpu	N	no	N		256	256	Y			4					minimal & complete	8 ALU inst, 3 port reg file
W	1	oberon_sdram	http://projectob	beta	nicolae Dumitrache	RISC	32	32	kintex-7-3	James	Brakef	2103	6		1	104	##	14.7	1.00	1.0	49.5	X		verilog	16	risc5	Y	yes	Y		4G	4G				16		2013	2017		minimalist Wirth, part of Project Obero	modified to use DRAM, serial mult
		oldland-cpu	http://jamieiles.a	altera dsg	Jamie Iles	RISC	32	32	kintex-7-3	James	altera primitiv	6					##	14.7	1.00	1.0		I		verilog	19	oldland_c	Y		N	N	4G	4G	Y			16	5	2015	2017			runs on Cyclone V
W	1	open8_urisc	https://opencore	stable	Kirk Hays, Jshamlet	RISC	8	8	kintex-7-3	James	Brakef	691	6	1		263	##	14.7	0.33	1.0	125.6	X		vhdl	9	Open8	Y	yes	N		64K	64K	Y			8		2006	2013		accum & 8 regs, clone of Vautomation u	RISC processor, in use

	_uP_all_soft folder	opencores or prmary link	status	author	style / clone	data size	inst size	FPGA	reporter	comment	LUTs ALUT	LUT?	mults	blk ram	F max	date	tool ver	MIPS /inst	clks/ inst	KIPS /LUT	vendor	SOC	src code	# src files	top file	doc	tool chain	fltg pt	Hav	max data	max inst	byte adrs	# inst	adr mod	# reg	pipe len	start year	last revis	secondary web link	note worthy	comments
	ourisc	https://opencore	alpha	Joao Carlos	RISC	16	16	stratix-4	Joao Carlos		500	A	1		550			0.67	1.0	737.0	I		vhdl									26				2013	2013		very incomplete source code	
	p8x32a_propell	https://www.pa	stable	Parallax Inc	RISC	32	32	kintex-7-3	James Brakef		9498	6		20	160	##	14.7	1.00	0.1	134.8	X		verilog	9	top	Y	yes									2014			eight propellers, clocking from ucf file	several FPGA card build files
	patmos	https://github.co	stable	Martin Schoeberl	RISC	32	32																scala														2015		http://patmos.compute.dtu.dk/		http://www.t-crest.org/
X	1 qrisc32	https://opencore	alpha	Viacheslav	RISC	32	32	arria-2	James Brakef		3075	A	4		144	##	q13.1	1.00	1.0	46.9	I		system v	8	qrisc32	Y	yes	N		4G	4G	Y			32	4	2010	2011		qrisc32 wishbone compatible risc core	for PhD thesis
	qs5-rible	http://www.sam	stable	John Rible	RISC	8	16	kintex-7-3	James Brakef		468	6			135	##	14.7	0.33	1.0	95.3	X		verilog	1	qs5_mix			N		256	32K	Y					1998	1999		used in his class, also uses eP32	
	risc_16bit	http://www2.ec	errors	Raj Parihar	RISC	16	16	kintex-7-3	James	empty design		6				##	14.7	0.67	1.0				verilog	19	ftpipe	Y						16		16		2006	2009		original design for university course	needs IO to be non-empty
X	1 risc0	https://sourcefo	beta	Niklaus Wirth	RISC	32	32	kintex-7-3	James Brakef		1186	6	4	6	110	##	14.7	0.67	1.0	61.9	X		verilog	8	RISC0	Y	yes	N		4G	4G						2011			minimalist Wirth, education tool	
W	1 risc5	http://www.proj	beta	Niklaus Wirth	RISC	32	32	kintex-7-3	James Brakef		2441	6	4	1	92	##	14.7	1.00	1.0	37.8	ILX		verilog	8	RISC5	Y	yes	Y		4G	4G				16		2013	2017		minimalist Wirth, part of Project Oberc	32x32 multiplier
	riscff		proprietar	ExpressIf	RISC	16	16																proprietary														2004			now produce ESP8266 & ESP32	
W	1 riscompatible	https://opencore	beta	Andre Soares	RISC	32	32	kintex-7-3	James	set IO	2167	6		1	145	##	14.7	1.00	3.0	22.3	X		vhdl	12	riscompat	Y	yes	N	Y	4G	4G	Y			16		2014			based on RISCO processor by Junqueira	& Suzim 1993
	risc-processor	https://github.co	stable	Jeff Bush	RISC	32	32	kintex-7-3	James Brakef		1445	6		6	161	##	14.7	1.00	1.0	111.6	X		verilog	22	fpga_top	Y	yes	N		4G	4G	Y			32		2008	2012		to document an early effort	author: implementation is not very good
W	rise	https://opencore	beta	Jlechner etal	RISC	16	16	kintex-7-3	James	missing black		6	1				14.7	0.67	1.0		X		vhdl	26	rise	Y	asm	N		64K	64K				16	5	2006	2010	en.wikiversity.org/wik	ARM style register usage	
W	1 rois	https://opencore	alpha	James Brakefield	RISC	24	24	kintex-7-3	James Brakef		384	6		1	170	##	14.7	0.83	1.0	368.8	X		vhdl	2	rois24_24min			N		16M	16M	N	30		64	1	2016	2017		single pipe stage, passes simulation	24-word operations only
W	1 rois	https://opencore	alpha	James Brakefield	RISC	24	24	kintex-7-3	James Brakef		382	6		1	120	##	14.7	0.83	1.0	261.7	X		vhdl	2	rois24_24up			N		16M	16M	Y	55		64	1	2016	2017		single pipe stage, pre simulation stage	8, 16 & 24-bit load/store
	s6soc	https://opencore	stable	Dan Gisselquist	RISC	32	32	spartan-6-3	James	sparta	2820	6	1	10	133	##	14.7	1.00	1.0	47.3	X	Y	verilog	31	toplevel			N	N	4G	4G	N	20		16	5	2015				uses ZIP CPU
W	1 sayeh_processo	https://opencore	stable	Alireza Haghdoost, Arn	RISC	16	8x	kintex-7-3	James Brakef		479	6	1		164	##	14.7	0.67	1.0	229.7	X		verilog	13	Sayeh	Y		N		64K	64K				32		2008	2009	haghdoost.persiangig.com		simple RISC
	sayuri_cpu	http://www.mor	stable	Toyoaki Sagawa	RISC	32	32	kintex-7-3	James Brakef		1604	6			208	##	14.7	1.00	1.0	129.9	X		vhdl	13	cpu01				Y	4G	4G				32		2000	2000		dead weblink	high number of DFF
W	scarts	https://opencore	beta	Jlechner, Martin Walte	RISC	16	16	kintex-7-3	James	missing signal		6					14.7	0.67	1.0				vhdl	18	scarts		yes	N		64K	64K		122		16	4	2011	2012		Scarts Processor	GCC compiler
	senior-sagn-1	https://github.co	simulation	Niranjan Ramadas	RISC	64	32	kintex-7-3	James	way to	1E+05	6	32		75	##	14.7	1.00	1.0	0.6	X		verilog	28	pipeline			N	Y			Y	137		32	4-8	2012	2012	nrbramadas.appspot.	university ASIC project, read PDF	64-bit data paths, superscalar, branch analysis
	spartanMC	http://www.spa	stable	Falk Hassler	RISC	18	18	kintex-7-3	James Brakef		853	6	1	2	120	##	14.7	0.67	1.0	94.6	X	Y	verilog	38	spartanm	Y	asm										2012	2014		SPARC like register windows	
	supersmall	http://www.eec	stable	Michael Ritchie	RISC	32	32	stratix_3	Michael Ritch		207	A		2+8	126	##	q9.0	1.00	16.0	38.1	I		verilog														2005	2009		2-bit serial, Mostly MIPS-I compliant	Copyright 2005,2006,2009 Jonathan Rose, and t
W	sxp	https://opencore	beta	Sam Gladstone etal	RISC	32	32			too many Ios													verilog	12	sxp			N		4G	4G				32		2001	2009		basic RISC	too many Ios
	table887	https://github.co	alpha	Robert Finch	RISC	16	16	kintex-7-3	James Brakef		643	6		2	208	##	14.7	0.67	1.0	217.1	X		verilog	2	table887_	Y		N	N	64K	64K		28		8		2014	2016			included with Table888 source code
	table888	https://github.co	alpha	Robert Finch	RISC	32	16	kintex-7-3	James Brakef		5756	6	9	6	137	##	14.7	2.00	1.0	47.6	X		verilog	3	table888	ome				4G	4G	Y	130		8		2014	2016		2016 version gives same reults as 2014	code for cache & mmu incomplete
	theia_gpu	https://opencore	beta	Diego Valverde	RISC	96	64	kintex-7-3	James	huge a	9E+05	6				##	14.7	0.40	1.0			GPL	verilog	32	theia												2009	2012		Ray Cast Programable graphic Process	four cores, huge LUT count, 2/3rds LUT RAM
	thor	https://opencore	mature	Robert Finch	RISC	32	32		Robert	missin	90000			306									verilog		thor	Y	asm	Y		4G	4G	Y			64		2015	2018	https://github.com/rc	Thor-2: L1 & L2 caches, GP float & vect	plans for 64-bit version (Thor-II) & 2M LUTs
	tigli_cpu		stable	Cleiton Juffo	RISC	16	16	kintex-7-3	James Brakef		636	6			455	##	14.7	0.67	4.0	119.7	X		verilog	24	cpu	Y		N	Y	64K	64K		16		16		2013	2013		course project, not pipelined	no LUT RAM for reg file
	tiny64	https://opencore	stable	Ulrich Riedel	RISC	32	32	kintex-7-3	James Brakef		874	6			189	##	14.7	1.00	2.0	107.9	X		vhdl	6	tinyx					64K	64K		14		8		2004	2007		data size from 32 to 64 bits	micro-coded sub-ops
X	tinycpu	https://opencore	alpha	Jordan Earls	RISC	8	8x	arria-2	James Brakef		136	A			384	##	q13.1	0.17	2.0	235.5	IX		vhdl	2	tinycpu		asm	N	N	1K	1K		12		4		2012	2012	directory contains tw	subset of 6502	MIPS/inst reduced due to few inst
	totalcpu	https://opencore	alpha		RISC	12+	12	kintex-7-3	James Brakef		229	6	1		149	##	14.7	0.33	3.0	71.7	X		verilog	10	cpu			N							16		2007	2009		data width 12 bits and up, no data memory	
	ucode_cpu	http://minnie.tu	stable	Warren Toomey	RISC	16	16	atrix-7-3	James	4K LU	6748	6	1	1		##	14.7	0.67	2.0		I		vhdl	16	cpu			N	N	64K	64K	N			16		2012	2015			originally schematic based (Logisim)
	ucpuvhdl	https://github.co	stable	Reed Foster	RISC	8	16	kintex-7-3	James	512 LU	933	6			118	##	14.7	0.33	2.0	20.8	X		vhdl	29	core	Y	asm	N		256	64K	Y	12	2	7		2016	2017	https://github.com/re	six tutorials on uCPUvhdl	using muCPUv2_1 of 3 upwards compatible des
	up1232	http://www.dte.	stable	Santiago de Pablo	RISC	8	16	kintex-7-3	James Brakef		220	6			244	##	14.7	0.33	3.0	122.0	X		vhdl	3	up1232a			N		64K	64K	Y	33	2	32		2000	2000		bare core, prog size 4K to 64K	description in source files
	urisc		errors	Farhad Mavaddat	RISC	16	16	kintex-7-3	James	missing modu		6				##	14.7	0.67	4.0				vhdl	31	urisc	Y				64K	64K	N	1				1987	2012	https://cs.uwaterloo.(	Ultimate Reduced Inst Set Computer Un. Of Waterloo	
	xgate	https://opencore	alpha	Robert Hayes	RISC	16	16	kintex-7-3	James Brakef		2778	6			159	##	14.7	0.67	1.0	38.3	X		verilog	7	xgate_top	Y		N					42		16		2009	2013		high pin count	Freescale XGATE co-processor compatible
W	1 xr16	https://github.co	stable	Jan Gray	RISC	16	16	kintex-7-3	James Brakef		273	6			263	##	14.7	0.67	1.0	644.8	X		verilog	4	xr16	Y		N		64K	64K				16		1999	2001		handcrafted instruction set	tool FPGA P&R, speed mode better
	xsoc	http://www.fpga	stable	Jan Gray	RISC	16	16	kintex-7-3	James	very s	371	6				##	14.7	0.67	1.0		X		verilog	16	xsoc	Y	yes	N	N	64K	64K	Y	16	4	16		2000	2001		very compact, bare core	similar to xr16
	xtensa		proprietar	tensilica/cadence	RISC	16	16,24	proprietary															proprietary							4G	4G				32	5,7			ch 8, Processor Desigr	upward compatible family, sliding reg	ASIC usage, TIE tool generates RTL & software t
	xthundercore	http://forum.gad	alpha	majordomo	RISC	32	16	kintex-7-3	James Brakef		793	6		2	193	##	14.7	1.00	1.0	243.7	X		vhdl	49	xtc	pm	yes	N	Y	4G	4G				16	5	2014		http://www.xthunder	Gadget Factory Forum thread	in debug, no comments, mostly in simulation
	xucpu	https://opencore	alpha	Jurgen Defurne	RISC	16	16	spartan-6-3	James Brakef		356	6		4	187	##	14.7	1.00	1.0	524.8	X	Y	vhdl	25	system_4k					4K	4K						2015	2017		Experimental Unstable CPU	
	xulalx25soc	https://opencore	mature	Dan Gisselquist	RISC	32	32	spartan-6-3	James	Sparta	7936	6	4	25	87	##	14.7	1.00	1.0	11.0	X	Y	verilog		toplevel			N	N	4G	4G	N	20		16	5	2015				uses ZIP CPU
X	yasep	news.yaesp.org	alpha	Yann Guidon	RISC	16	32	kintex-7-3	James	reduc	632	6			215	##	I14.7	1.00	2.0	170.0	AX		vhdl	3	microYAE	Y	asm	N	N	2G	2G		51		16		2005	2014		JavaScript generated VHDL, revisions c	YASEP talk at www.youtube.com/watch?v=bw5
	yfcpu	https://github.co	errors	Cory Walker	RISC	16	16	kintex-7-3	James	degen	18	6				##	14.7	0.67	1.0				verilog	2	yfcpu	Y		N	N	256	256	Y	5	1	16				Colin Mackenzie?	Educational	very simple
W	1 zipcpu	https://github.co	alpha	Dan Gisselquist	RISC	32	32	kintex-7-3	James Brakef		1687	6		2	218	##	14.7	1.00	1.0	128.9	X		verilog	7	zipcpu	Y		N	N	4G	4G	N	20		16	5	2015	2018	www.librecores.org/Z	ISA has chnaged, multiple instruction sequences for many operations	
	reonv	https://github.co	difficult	Lucas Castro	risc-v	32	32	kintex-7-3	James	many files		6				##	14.7	1.00	1.0				vhdl			Y	yes	N		4G	4G	Y			32		2017	2018	https://strijar.livejour	uses Leon infrastructure with risc-v ISA	
	riscv_ariane	https://github.co	stem verilog		risc-v	64	32																system verilog			Y	yes	N				Y			32		2018	2018	https://github.com/p	part of pulp project	simulation only
	riscv_clarvi	https://github.co	stem verilog		risc-v	32	32																system verilog			Y	yes	N		4G	4G	Y			32		2016	2017		educational simple RISC-V implementation in SystemVerilog	
W	1 riscv_GRVI-pha	http://fpga.org/	beta	Jan Gray	risc-v	32	32	virtex-u-2	Jan Gray		320	6		1	375	##	v16.4	1.00	1.0	1171.9	X		proprietary			Y	yes	N		4G	4G	Y	45		32	3	2015	2018	https://www.youtube	uses DSP48, hand fitted & placed	"Hoplite" router, 1680 cores in XCVU9P
	riscv_microsem	https://github.co	proprietary		risc-v	32	32																verilog			Y	yes	N		4G	4G	Y			32		2016	2018	https://www.microse	not much source code provided	runs on igloo2 or polarfire boards
W	1 riscv_orca	https://github.co	beta	VectorBlox	risc-v	32	32	stratix-5	vectorblox		1082	A		?	244	##	14.7	0.98	1.0	221.0	I		vhdl	13	orca	Y	yes	N		4G	4G	Y			32		2016			*, /, fltg-pt all optional	RV32IM
W	1 riscv_picorv32	https://github.co	beta	Clifford Wolf	risc-v	32	32	kintex-U-3	Cliffor	small	725	6			769	##	v16.2	1.00	4.0	265.2	X		verilog	1	picorv32	Y	yes	N		4G	4G	Y			32		2016			mimimal features	designed for minimum LUTs
	riscv_potato	https://github.co	beta	Kristian Skordal	risc-v	32	32	kintex-7-3	James Brakef		2817	6			113	##	14.7	1.00	1.0	40.1	X		vhdl	20	pp_core	Y	yes	N	N	4G	4G	Y	30		32		2014			risc-V interger only, no mult	"rocket-core" version at risc.org
	riscv_pulpino	https://github.co	stem verilog		risc-v	32	32																system verilog			Y	yes	N		4G	4G	Y			32		2015	2018	http://www.pulp-plat	pulpissimo is single core "pulp" with interest in non-riscv ISA expansion	
	riscv_rocket	https://github.co	stem verilog		risc-v	32	32																system verilog			Y	yes	N		4G	4G	Y			32		2016	2017			
	riscv_rv01_core	https://opencore	stable	Stefano Tonello	risc-v	32	32	kintex-7-3	James Brakef		13997	6	4	62	130	##	14.7	1.00	1.0	9.3	X		vhdl	65	rv01_selfi	Y	yes	N		4G	4G	Y			32		2015	2017		all files in one directory	two self test tops
	riscv_rv12	https://github.co	stem verilog		risc-v	32	32																system verilog			Y	yes	N		4G	4G	Y			32				https://roalogic.com		
	riscv_scr1	https://github.co	stem verilog		risc-v	32	32																system verilog			Y	yes	N		4G	4G	Y			32				http://syntacore.com		
	riscv_sifive	https://github.co	proprietar	sifive	risc-v	32	32																scala			Y	yes	N		4G	4G	Y			32			2018	https://www.sifive.co	top files only	provides bit files for FPGA dev kits
	riscv_sodor	https://github.co	scala		risc-v	32	32																scala			Y	yes	N		4G	4G	Y			32					1, 2, 3 and 5 stage pipe versions	
	riscv_taiga	https://gitlab.co	stem veril	Eric Matthews	risc-v	32	32	zynq			1551			1	123			1.00	1.0	79.3	X		system v	46		Y	yes	N		4G	4G	Y			32		2017			TAIGA: A new RISC-V soft-processor fr	33% smaller & 39% faster than LEON3
	riscv_urv-core	https://github.co	error	Tomasz Włostowski	risc-v	32	32	kintex-7-3	James	missing files						##	14.7	1.00	1.0				verilog			Y	yes	N		4G	4G	Y			32		2015	2015			
	riscv_vexriscv	https://github.co	spinalHDL		risc-v	32	32	atrix-7-3			1399				295			1.00	1.0	210.9	X		spinalHDL			Y	yes	N		4G	4G	Y			32			2018		preformance #s for 8 configurations or	VexRiscv full no cache
	riscv_vhdl	https://opencore	errors	Sergey Khabarov	risc-v	64	32	kintex-7-3	James	many files, mi		6				##	14.7	1.00	1.0			Y	vhdl & verilog			Y	yes	N		4G	4G	Y			32		2016	2017	https://github.com/se	System-On-Chip based on bare Rocket	both rocket & river cores
	riscv_zscale	https://github.co	scala		risc-v	32	32																scala			Y	yes	N		4G	4G	Y			32		2015	2017		not maintained & not conformant	
	vexriscv	https://github.co	beta	Charles Papon?	risc-v	32	32	artix-7	Charles Papo		481	6			346			0.52	1.0	374.1	X		spinalHDL		smallest	Y	yes			4M	4M	Y						2018		6 version & four FPGA families	written in "SpinalHDL"
	vscale	https://github.co	stable		risc-v	32	32	kintex-7-3	James Brakef		3072	6			127	##	14.7	1.00	1.0	41.2	X		verilog	23	vscale_core			N							32		2016	2017		risc-v RV32IM vscale processor, depre	not up to date (risc-v)
W	1 yarvi	https://github.co	beta	Tommy Thorn	risc-v	32	32	kintex-7-3	James Brakef		1935	6		35	122	##	14.7	1.00	2.0	31.5			verilog	1	yarvi	Y	yes	N	N	4G	4G				32	3		2014		no multiply or divide	simple implementation of RISC-V
	f32c	https://github.co	beta	zec & vordah	risc-v/MIPS	32	32	atrix-7-3	zec & v	int	1048	6	4	33	185	##	14.7	1.00	1.0	176.5	X		vhdl	50		Y	yes	N	Y	4G	4G	Y	30		32	5	2014	2018	http://www.nxlab.fer	MIPS or RISC-V ISA, Arduino support	
	jcore_aka_sh2	http://www.j-co	difficult	Jeff Dionne	SH2	32	16			need to run make per README file													vhdl	136															https://www.youtube.com/watch?v=l	Americans in Japan	
	fgpu	https://github.co	stable	Muhammed al Kadi	SIMT	32	32	zynq7045	Muhammed		128K	6	192	167		##	v17.2				X		vhdl	34	fgpu	Y	yes	Y		4G	4G	Y			32		2016	2017	https://dl.acm.org/cit	eigth cores, reviews comparable proje	vivado fltg-pt IP, benchmarks, wikipedia: GPGPU
A	erc32	http://www.fpga	untested	Jiri Gaisler	SPARC	32	32					4						1.00	1.0				vhdl			Y	yes	Y		4G	4G	Y			64	7	1993	1999	https://en.wikipedia.(	rad hard SPARCv7 3 chip asic dsgn	Gaisler's 1st efforts
A	leon3	http://www.gais	stable	Jiri Gaisler, Jan Anderss	SPARC	32	32		Jiri Gaisler		3448	4			183			1.00	1.0	53.1	AILX		vhdl	100s	leon3x	Y	yes	Y		4G	4G	Y			64	7	2003	2017	https://en.wikipedia.(	customized for ~50 FPGA boards, conf	have yet to get s sucessful C,P&R
	openpiton	http://parallel.pr	difficult	mmckeown	SPARC	32	32	kintex-7-3	James	too many files		6				##	14.7	1.00	1.0				verilog			Y	yes	Y	N	4G	4G	Y			64		2015	2018	http://parallel.princet	Princeton Un.	both FPGA & ASIC, very many source files

		_uP_all_soft folder	opencores or prmary link	status	author	style / clone	data size	inst size	FPGA	reporter	comment	LUTs ALUT	LUT?	mults	blk ram	F max	date	tool ver	MIPS /inst	clks/ inst	KIPS /LUT	vendor	SOC	src code	# src files	top file	doc	tool chain	fltg pt	Hav'	max data	max inst	byte adrs	# inst	adr mod	# reg	pipe len	start year	last revis	secondary web link	note worthy	comments
A	1	s1_core	https://opencore	stable	Fabrizio Fazzino etal	SPARC	64	32	kintex-7-3	James Brakef		52845	6	8	59	56	##	v14.1	2.00	1.0	2.1	IX		verilog	136	s1_top	Y	yes	Y	N	4G	4G	Y			32		2007	2012	https://en.wikipedia.c	reduced version of OpenSPARC T1	Vivado run
		sparc64soc	https://opencore	alpha	Dmitry Rozhdestvenski	SPARC	64	32	kintex-7-3	James	errors		6				##	14.7	2.00	1.0			Y	verilog	263	W1	N		Y									2009	2010		huge source file count	work in progress with no progress
		temlib	http://temlib.org	stable		SPARC	32	32	kintex-7-3	James Brakef		3730	6	5		111	##	14.7	1.00	1.0	29.8	X		vhdl	48	fpu_simple			Y	N	4G	4G	Y			64		2013	2015	SparcV8 (SparcStation	copywrite: experimental use	options for fltg-pt, pipeline, mul & div configura
		temlib	http://temlib.org	stable		SPARC	32	32	kintex-7-3	James Brakef		2579	6		32	111	##	14.7	1.00	1.0	43.1	X		vhdl	48	mcu_simple			Y	N	4G	4G	Y			64		2013	2015	SparcV8 (SparcStation	copywrite: experimental use	has caches
W	1	hive	https://opencore	stable	Eric Wallin	stack	32	16	arria-2	James Brakef		1420	A	8	24	283	##	q13.1	1.00	1.0	199.4	ILX		verilog		hive_core	Y		N				N	40		10	8	2013	2015		4 symetrical stacks, eight threads via pipeline barrel	
		m17	http://users.ece.	asic	Philip Koopman	stack																		proprietary																	chapter 4.3 in Koopman	6600 gate ASIC
		minicpu	http://www.cs.h	stable	Hirotsugu Nakano	stack	16	5	kintex-7-3	James	lots of	433	6	1	1	128	##	14.7	0.33	1.0	97.7	X		verilog	7	minicpu	Y	yes	N		4K	4K	N	26				2008	2018			**uses Flex, Bison & Perl to create gcc compiler**
		minicpu-s	https://github.co	stable	Michael Morris	stack	16	8	kintex-7-3	James Brakef		147	6			741	##	14.7	0.67	28.0	120.6	X		verilog	2	both	Y		N					33				2012	2013		separate source for each CPLD chip, us	fits (2) XC9500 CPLD
		mproz	http://www.bitli	stable	K. Lee	stack	16	16	kintex-7-3	James	schematic		6				##	14.7	1.00	1.0				schematic			Y	asm	N			32K						1999	2007	https://groups.google	little documentation, CPLD implement	also mproz3
		pancake	https://people.e	stable	Bruce Land	stack	16	5	kintex-7-3	James	bypas	441	6	1	1	128	##	14.7	0.67	1.0	194.8	X		verilog	7	de2_mini	Y	yes	N		4K	4K		31				2010	2014	http://www.cs.hirosh	The Pancake Stack Machine dervied fr	Cornell ECE5760
		tiny_cpu	http://www.cs.h	errors	K. Nakano	stack	16		kintex-7-3	James	multiple assig		6				##	14.7	0.66	3.0		IX		verilog	11	DE2_TINY	Y	yes	N		4K	4K						2007	2009	http://www.cs.hirosh	different from tinycpu	uses Flex, Bison & Perl to create gcc compiler
		the12X_12uP		alpha	James Brakefield	stack/acc	12	12	kintex-7-3	James Brakef		972	6	1	1	123	##	14.7	0.50	1.0	63.3	X		vhdl	2	the12x_1	Y	no	Y	N	4K	4K	N	54		64	1	2015			combo stack/accumulater design	load/store arch, not optimized
A	1	aquarius	https://opencore	stable	Thorn Aitch	SuperH-2	32	16	kintex-7-3	James Brakef		4071	6	2	10	97	##	14.7	1.00	1.0	23.7	ILX		verilog	21	top	Y	yes	N		4G	4G	Y					2003	2012			
X	1	uTTA		stable	Hans Tiggeler	TTA	16	16	kintex-7-3	James Brakef		810	6	1		57	##	14.7	0.67	1.0	47.4	X		vhdl	23	utta_stru	N	asm	N											http://www.ht-lab.co	time triggered arch	bad weblink
A	1	aeMB	https://opencore	beta	Shawn Tan	uBlaze	32	32	kintex-7-3	James Brakef		1018	6	3		131	##	14.7	1.00	1.0	128.5	ILX		verilog	7	aeMB_co	Y	yes	N		4G	4G	Y					2004	2009		not 100% compatable	
		an-noc-mpsoc	https://opencore	mature	Alireza Monemi	uBlaze	32	32	kintex-7-3	James Brakef		1164	6	3	1	192	##	i14.7	1.00	1.0	165.2	X	Y	verilog	90	aeMB	Y	yes	N		4G	4G	Y					2014	2017		uses lm32 or aeMB uP by Shawn Tan	SOC top module generated by JS?
A	1	mblite	https://opencore	beta	Tamar Kranenburg	uBlaze	32	32	kintex-7-3	James Brakef		941	6		2	227	##	14.7	1.00	1.0	240.9	IX		vhdl	18	core_wb	Y	yes	N		4G	4G	Y	86		32		2009	2017		not all instructions implemented	moved everything to work library
		mb-lite_plus	http://www.late	stable	Huib Arriens	uBlaze	32	32	kintex-7-3	James Brakef		260	6		2	323	##	14.7	1.00	1.0	1240.7	X		vhdl	34	tumbl_fsl	Y	yes	N		4G	4G	Y			32		2010	2012		Delft Un. Of Tech. course work	very lite? Should be more LUT RAM?
A	1	microblaze	https://www.xili	proprietar	Xilinx	uBlaze	32	32	kintex-7	Xilinx		546	6		1	320			1.03	1.0	603.7	X		proprietary			Y	yes	opt		4G	4G	Y	86		32	3	2002			MicroBlaze MCS, smallest configuratio	70 configuration options, MMU optional
		mpdma	https://opencore	beta	quickwayne	uBlaze	32	32	kintex-7-3	James Brakefield			6				##	14.7	1.00	1.0			Y	perl			Y	yes	N		4G	4G	Y			32		2006	2009		Soft MultiProcessor on FPGA	Perl gens *.xmp, mhs, mss & ucf files
A		myblaze	https://opencore	mature	Jian Luo	uBlaze	32	32	kintex-7-3	James Brakefield			6				##	14.7	1.00	1.0				myhdl	15	top	Y	yes	N		4G	4G	Y			32		2010	2010	microBlaze data shee	clone, python code generators	
A		myblaze	https://opencore	mature	Jian Luo	uBlaze	32	32	kintex-7-3	James Brakefield			6				##	14.7	1.00	1.0				myhdl			Y	yes	N		4G	4G	Y			32		2010	2010	microBlaze data shee	clone, python code generators	
		openfire_core	https://opencore	alpha	Alex Marschner, Steph	uBlaze	32	32	kintex-7-3	James	empty project		6					14.7	0.33	1.0				verilog	12	openfire_	Y	yes	N	N	4G	4G	Y			32		2007	2009		OpenFire Processor Core	"FPGA Proven"
A	1	openfire2	https://opencore	beta	Antonio Anton	uBlaze	32	32	kintex-7-3	James Brakef		1201	6	3	2	105	##	14.7	1.00	1.0	87.4	X	Y	verilog	27	openfire_	Y	yes	N	N	4G	4G	Y			32		2007	2012		"FPGA Proven"	derived from Stephen Craven's OpenFire
		openscale	http://www.lirm	stable		uBlaze	32	32	spartan-3-4	Lyonel Barthe		1563	4			91		i12.1	1.00	1.0	58.2	X	Y	vhdl	26	sb_core		yes			4G	4G	Y	86		32	5	2010	2012	www.lirmm.fr/ADAC	NoC secretblaze	data is for single secretblaze
A	1	secretblaze	http://www.lirm	beta	Lyonel Barthe	uBlaze	32	32	spartan-3-4	Lyonel Barthe		1563	4			91		i12.1	1.00	1.0	58.2	X		vhdl	26	sb_core		yes			4G	4G	Y	86		32	5	2010	2012	www.lirmm.fr/ADAC		
X	1	lemberg	https://github.co	stable	Wolfgang Puffitsch	VLIW	32	32	cyclone-4-6	James Brakef		37459	4	25	54	43	##	q13.1	1.00	1.0	1.1	I		vhdl	57	core	Y	yes	Y		4G	2M	Y			32	4	2011		http://www2.imm.dtu	upto 4 inst/clock	LPM mem & floating point
		tinyvliw8	https://opencore	alpha	Oliver Stecklina	VLIW	8	32	kintex-7-3	James	hacke	895	6			149	##	14.7	0.33	1.0	55.0	X		vhdl	19	sysarch			N	Y	256	1K	Y					2013	2016		tinyVLIW8 soft-core processor	bare core, Altera LPM for RAMs
A	1	ao486	https://opencore	beta	Aleksander Osman	x86	32	8x	cyclone-4-7	James Brakef		36094	4	4	47	46	##	q13.1	1.00	1.0	1.3	I	Y	system v	85	ao486	Y	yes			4G	4G	Y					2014	2014		complete 486, SoC configuration	non-SoC, no MMU
A	1	cpu86	http://www.ht-la	beta	Hans Tiggeler	x86	8	8x	kintex-7-3	James Brakef		3421	6	1		127	##	14.7	0.17	2.0	3.1	X		vhdl	23	cpu86_to	Y	yes	N	N	1M	1M	Y					2002	2010	http://www.ht-lab.co	8088 clone	
A	1	mcl86	http://www.mic	stable	MicroCore Labs	x86	16	8x	kintex-7-3	MicroCore La		308	6		4	180			0.67	20.0	19.6	X					Y	yes	N	N	1M	1M	Y					2016		http://www.embedde	microcoded, meets original 8088 timing@100MHz	
A	1	next186	https://opencore	stable	Nicolae Dumitrache	x86	16	8x	arria-2	James Brakef		1966	A	2		77	##	q13.1	0.67	2.0	13.1	IX		verilog	4	Next186_	Y	yes	N	N	1M	1M	Y					2012	2013		boots DOS	
		next186_soc_p	https://opencore	stable	Nicolae Dumitrache	x86	16	8x	kintex-7-3	James	translate erro		6	1			##	14.7	0.67	2.0			Y	verilog	40	ddr_186	Y	yes	N	N	1M	1M	Y					2013	2018		SoC version of next186	boots DOS
		next186mp3	https://opencore	stable	Nicolae Dumitrache	x86	16	8x	kintex-7-3				6	1			##	14.7	0.67	2.0			Y	verilog	16	ddr_186	Y	yes	N	N	1M	1M	Y					2013	2014		SoC version of next186	boots DOS, has DSP core, no x86 source
B	1	rtf8088	https://opencore	planning	Robert Finch	x86	16	8x	kintex-7-3	James Brakef		4514	6	4		174	##	14.7	0.67	3.0	8.6	X		verilog	57	rtf8088	Y	yes	N	N	1M	1M	Y					2012	2013	https://github.com/ro	8-bit memory data, e.g. 8088	
		s80186	https://github.co	stem veril	Jamie Iles	x86	16	8	cyclone-V	Jamie Iles		1750	A			60			0.67	2.0	11.5	I	Y	system verilog																https://www.jamieiles.com/80186/		
		sp-i586	https://github.co	stable	Lini Mestar	x86	32	8	kintex-7-3	James Brakef		32144	6	4	28	73	##	14.7	1.00	2.0	1.1	X		verilog	37	top_sys	Y	yes	Y		4G	4G	Y					2016	2016	http://lmeshoo.net/	gate level dsgn, vivado project also	http://img.youtube.com/vi/2W1guyhCJuE/0.jpg
		sub86	https://opencore	alpha	Jose Rissetto	x86	16	8	kintex-7-3	James Brakef		1916	6			172	##	14.7	0.67	3.0	20.1	X		verilog	1	sub86	Y	yes	N	N	64K	64K	Y			7		2012	2013		very small x86 subset core	no segment registers, limited op-codes
A	1	v586	https://opencore	beta	Jose Rissetto	x86	32	8x	kintex-7-3	James Brakef		22282	6	12	16	102	##	14.7	1.00	2.0	2.3	X		verilog	22	v586	Y	yes	N		1M	1M	Y					2014		www.valptek.com/	MMU & caches, branch cache	www.youtube.com/channel/UCNbm8Bah54cwl
A	1	zet86	https://opencore	alpha	Zeus Marmolejo	x86	16	8	kintex-7-3	James Brakef		3642	6	1		68	##	14.7	0.67	2.0	6.2	X		verilog	32	fpga_zet_	Y	yes	N	N	1M	1M	Y					2008	2014	http://zet.aluzina.org	equivalent to 80186, boots MS-DOS	Zet The x86 (IA-32) open implementation
		fpz8	https://opencore	stable	Fabio Pereira	Z8	8	8	cyclone-4	James Brakef		5184	4	1	16		##	14.7	0.33	4.0		I		vhdl	4	fpz8_cpu_	Y		N	Y	2K	16K	Y					2016	2016			Altera megafunctions (mem)
X	1	altium/TSK80x	http://techdocs.	proprietar	Altium	Z80	8	8x	spartan-3-5	Altium		2558	4			50			0.33	3.0	2.2	AILX		proprietary			Y	yes	N	N	64K	64K	Y					2004	2017	CR0140.pdf, CR0117.p	frozen, asm, C, C++, schem, VHDL & Ve	default clock speed is 50MHz
A		a-z80	https://opencore	stable	Goran Devic	Z80	8	8	cyclone-2	Goran Devic		2084	4			20	##	q11.1s	0.33	1.0	3.1	IX		verilog	24	z80_top_	Y	yes	N	N	64K	64K	Y					2014	2018		gate level reverse eng'd Z80	Complete implementation of a Sinclair ZX Spect
A	1	a-z80	https://opencore	stable	Goran Devic	Z80	8	8	kintex-7-3	James Brakef		1186	6			24	##	14.7	0.33	1.0	6.8	IX		verilog	24	z80_top_	Y	yes	N	N	64K	64K	Y					2014	2018		gate level reverse eng'd Z80	Complete implementation of a Sinclair ZX Spect
A	1	nextz80	https://opencore	stable	Nicolae Dumitrache	Z80	8	8x	kintex-7-3	James Brakef		1064	6			106	##	14.7	0.33	1.0	32.7	X		verilog	3	NextZ80C	Y	yes	N	N	64K	64K	Y					2011	2014	z80 data sheets		
		reverse-u16	https://github.co	stable	A.T.	Z80	8	8	cylcone-4	James Brakef		11224	4		60		##	14.7	0.33	4.0		X	Y	vhdl	29	zxpoly	Y	yes	N	N	64K	64K	Y					2015			SOC project using T80, HDMI generato	retro Z80 based on T80 by Daniel Wallner
A	1	socz80	http://sowerbut	stable	Will Sowerbutts	Z80	8	8x	spartan-6-3	James	constr	2568	6		15	93	##	14.7	0.33	3.0	4.0	X		vhdl	25	top_level	Y	yes	N	N	64K	64K	Y					2013	2014	z80 data sheets	based on Daniel Wallner's T80, for Papillio Pro board	
A	1	t80	https://opencore	stable	Daniel Wallner	Z80	8	8x	kintex-7-3	James	Z80 m	1389	6			163	##	14.7	0.33	3.0	12.9	X		vhdl	5	T80a	Y	yes	N	N	64K	64K	Y					2002	2011	z80 data sheets	Z80, 8080 & gameboy inst sets, several usages	
A	1	tv80	https://opencore	mature	Guy Hutchison, Howard	Z80	8	8x	kintex-7-3	James Brakef		1207	6			182	##	14.7	0.33	3.0	16.6	IX		verilog	6	tv80n	Y	yes	N	N	64K	64K	Y					2004	2018	https://github.com/hu	derived from Daniel Wallner's T80, ASIC implementations	
A	1	wb_z80	https://opencore	stable	Brewster Porcella	Z80	8	8x	kintex-7-3	James Brakef		2025	6			144	##	14.7	0.33	3.0	7.8	X		verilog	4	z80_core_	Y	yes	N	N	64K	64K	Y					2004	2012	z80 data sheets	derived from Guy Hutchison TV80	Wishbone High Performance Z80
A		y80e	https://opencore	stable	Sergey Belyashov	Z80	8	8x	kintex-7-3	James	errors		6				##	14.7	1.00	3.0				verilog	15	top_level	Y	yes	N	N	64K	64K	Y					2013	2013	z80 data sheets	Y80e - Z80/Z180 compatible processor	based on Y80 from "Microprocessor Design Usin
		z80control	https://opencore	alpha	Tyler Pohl	Z80	8	8	kintex-7-3	James Brakef		1483	6			189	##	14.7	0.33	3.0	14.0	X	Y	verilog	55	top_de1	Y	yes	N	N	64K	64K	Y					2010	2012		Microprocessor targeting embedded ir	interfaces to DRAM, based on T80 core
A	1	z80soc	https://opencore	stable	Ronivon Costa	Z80	8	8	spartan-3e-	James Brakef		2474	4	2	19	78	##	14.7	0.33	3.0	3.4	IX	Y	vhdl	19	top_s3e	Y	yes	N	N	64K	64K	Y					2008	2016		based on Daniel Wallner's T80	
		complete_8bit	https://www.qu	stable	Van-Lei Le		8	8	kintex-7-3	James	modif	208	6		1	260	##	14.7	0.33	3.0	137.5	X		vhdl	6	computer	N	no	N		96	128	Y					2016				memory_unit uses block RAM, IO ports pruned
		gpu	https://opencore	stable	Diego A. Idarraga				kintex-7-3	James	errors in sourc		6				##	14.7	1.00	1.0				vhdl	21	gpu			Y									2015	2015		graphic processing unit	coding errors
		pycpu	https://pycpu.w	myhdl	Norbert Feurle																			myhdl														2013		https://pycpu.wordpr	python hardware processor	
		reduceron	https://www.cs.	altera dsg	Matthew Naylor/Tommy Thorm						altera project											I		verilog														2008	2018	https://github.com/to	hardware for functional programming	Quartus projects

15 ## ##

71 # usable(beta, st 12 12 45 40 ## ## ## 140 195

49 "B" or "X" of limi 8 486 451 450 216

17

27

MIPS/MHz Pro-rating for data size:

1-bit	0.04	16-bit	0.67	64-bit	2.00
4-bit	0.17	24-bit	0.80	**Silicon Area equivalents**	
8-bit	0.33	32-bit	1.00	LUTS/DSP48	16:1
12-bit	0.40	48-bit	1.50	LUTS/Block RAM	32:1

Under the assumption that the core is capable of one instuction per clock

Web page DMIPS per clock cycle per core en.wikipedia.org/wiki/Instructions_per_s community.freescale. www.eembc.org/coremark/index.php

DMIPS per clock for many microprocessors: http://en.wikipedia.org/wiki/Instructions_per_second

46	_paper_only
23	_weak_start
14	_up_cores
23	in limbo
24	planning
12	simulation
487	main
629	total

215	VHDL
193	Verilog
17	System Verilog
7	Spinal/Scala
6	VHDL & Verilog
3	MyHDL
27	proprietary
2	Schematic
470	total

Column Titles	Details
"A"	A: 1st choice clone, B: 2nd choice clone, W: 1st choice original, X: 2nd choice original
"B"	used to indicate best KIPS/LUT for a given design, usually using fast FPGA family
_uP_cores_test folder	if opencores design is their folder name, otherwise my folder name

_uP_all_soft folder	opencores or prmary link	status	author	style / clone	data size	inst size	FPGA	reporter	comment	LUTs ALUT	LUT?	mults	blk ram	F max	date	tool ver	MIPS /inst	clks/ inst	KIPS /LUT	vendor	SOC	src code	# src files	top file	doc	tool chain	fltg pt	Hav'd	max data	max inst	byte adrs	# inst	adr mod	# reg	pipe len	start year	last revis	secondary web link	note worthy	comments

opencores or primary link	about 200 designs in open cores, about 100 in github
status	ASIC, paper (detailed in), planning (no source), alpha, beta, stable, mature, proprietary, untested; incomplete, educational, <16 instructions, simulation
author	First Name, Last Name
style / clone	part number or "forth", RISC, accumulator, etc
data size	data memory bus word size in bits
inst size	shortest instruction size in bits
FPGA	FPGA family for compile, place, route & timing, usually using fastest part grade
reporter	First Name, Last Name
comments	compile, place, route & timing problems
LUTs ALUT	total number of LUTs, ALUTs or tiles used including route-thrus & otherwise unavailable
LUT?	4-LUT, 6-LUT, Altera ALUT, Actel Tile
mults	total number of multipliers/DSPs used; 9x9 multiplier counts divided by two and rounded up
blk RAM	total # of block RAMs used, Xilinx half block RAM counts divided by two and rounded up
Fmax	maximum primary clock speed from compile, place & route run without clock constraints
date	date of compile, place & route; serves to identify source version
tool ver	Altera (**Q**uartus), Xilinx (ISE, **V**ivado), Lattice Semiconductor(**D**iamond) or MicroSemi(**L**ibero) tool version number
MIPS /inst	prorated DMIPS per instruction, reduced for data word sizes under 32-bits, greater than one for multiple issue processors
clks/ inst	number of clocks per instruction, typically 1.0 for modern pipelined processors, subjective for older uP
KIPS /LUT	figure of merit, does not include effects of memory capacity, floating point or instruction set quality
Vendors	Vendors for which design builds: Actel: Libero, Intel(Altera): Quartus; Latticesemi: Diamond & iCEcube, Xilinx: ISE & Vivado
Prog File	FPGA family build projects present: X: Sn, A7, Kn, Vn, Zn; A: Mn, Arn, Cn, Stn; M: Tn, Pf, Fn; L: En, Mhn, Sbn, Xpn; n is family generation #
SOC	System on a Chip?
src code	VHDL or Verilog or System Verilog or schematic or gates or Proprietary or Scala ect
# src files	number of source files for compile, place, route & timing
top file	top file for compile, place, route & timing run
doc	is documentation provided?
tool chain	is there a compiler or assembler provided or available
fltg pt	does the compile, place, route & timing run include floating point?
Hav'd	H: separate instruction and data memory(s), 2C: # caches, M: MMU, N: von Neuman (single memory bus)
max data	maximum data address
max inst	maximum instruction address
byte adrs	is byte addressing provided
# inst	number of unique instructions, somewhat subjective
adr modes	abs, imm, PC rel, indexed, reg-reg indexed; stack, indir, indir++, --indir; (indir), (indir++), (--indir), (indexed), abs-short/direct page, scaled
# reg	number of registers in register file
pipe len	number of pipeline stages
start year	year of first design activity
last revis	last year for revisions
reference	web address or generic information (for clones), landing page for opencore entries