















_uP_all_soft folder	opencores or primary link	status	author	style / clone	data size	inst size	FPGA	repor ter	com ment	LUTs ALUT	LUT? LUT?	mults	blk ram	F max	date	tool ver	MIPS /inst	clks/ inst	KIPS /LUT	ven dor	SO C	src code	# src files	top file	doc chain	ftg pt	Hav' d	max data	max inst	byte adrs	# inst	adr mod	# reg	pipe len	start year	last revis	secondary web link	note worthy	comments
opencores or primary link		about 200 designs in open cores, about 100 in github																																					
status		ASIC, paper (detailed in), planning (no source), alpha, beta, stable, mature, proprietary, untested; incomplete, educational, <16 instructions, simulation																																					
author		First Name, Last Name																																					
style / clone		part number or "forth", RISC, accumulator, etc																																					
data size		data memory bus word size in bits																																					
inst size		shortest instruction size in bits																																					
FPGA		FPGA family for compile, place, route & timing, usually using fastest part grade																																					
reporter		First Name, Last Name																																					
comments		compile, place, route & timing problems																																					
LUTs ALUT		total number of LUTs, ALUTs or tiles used including route-thrus & otherwise unavailable																																					
LUT?		4-LUT, 6-LUT, Altera ALUT, Actel Tile																																					
mults		total number of multipliers/DSPs used; 9x9 multiplier counts divided by two and rounded up																																					
blk RAM		total # of block RAMs used, Xilinx half block RAM counts divided by two and rounded up																																					
Fmax		maximum primary clock speed from compile, place & route run without clock constraints																																					
date		date of compile, place & route; serves to identify source version																																					
tool ver		Altera (Quartus), Xilinx (ISE, Vivado), Lattice Semiconductor(Diamond) or MicroSemi(Libero) tool version number																																					
MIPS /inst		prorated DMIPS per instruction, reduced for data word sizes under 32-bits, greater than one for multiple issue processors																																					
clks/ inst		number of clocks per instruction, typically 1.0 for modern pipelined processors, subjective for older uP																																					
KIPS /LUT		figure of merit, does not include effects of memory capacity, floating point or instruction set quality																																					
Vendors		Vendors for which design builds: Actel: Libero, intel(Altera): Quartus; Latticesemi: Diamond & iCEcube, Xilinx: ISE & Vivado																																					
Prog File		FPGA family build projects present: X: Sn, A7, Kn, Vn, Zn; A: Mn, Arn, Cn, Stn; M: Tn, Pf, Fn; L: En, Mhn, Sbn, Xpn; n is family generation #																																					
SOC		System on a Chip?																																					
src code		VHDL or Verilog or System Verilog or schematic or gates or Proprietary or Scala ect																																					
# src files		number of source files for compile, place, route & timing																																					
top file		top file for compile, place, route & timing run																																					
doc		is documentation provided?																																					
tool chain		is there a compiler or assembler provided or available																																					
ftg pt		does the compile, place, route & timing run include floating point?																																					
Hav'd		H: separate instruction and data memory(s), 2C: # caches, M: MMU, N: von Neuman (single memory bus)																																					
max data		maximum data address																																					
max inst		maximum instruction address																																					
byte adrs		is byte addressing provided																																					
# inst		number of unique instructions, somewhat subjective																																					
adr modes		abs, imm, PC rel, indexed, reg-reg indexed; stack, indir, indir++, --indir; (indir), (indir++), (--indir), (indexed), abs-short/direct page, scaled																																					
# reg		number of registers in register file																																					
pipe len		number of pipeline stages																																					
start year		year of first design activity																																					
last revis		last year for revisions																																					
reference		web address or generic information (for clones), landing page for opencore entries																																					