ProNoC

RAM

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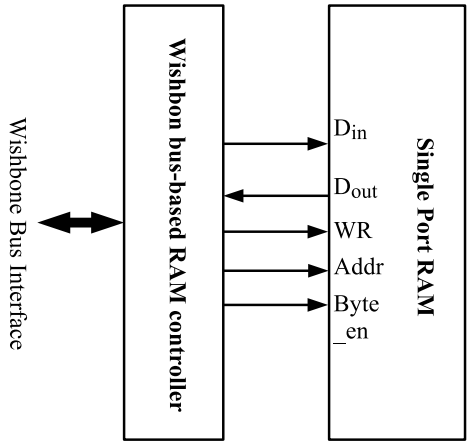
WB Single Port RAM

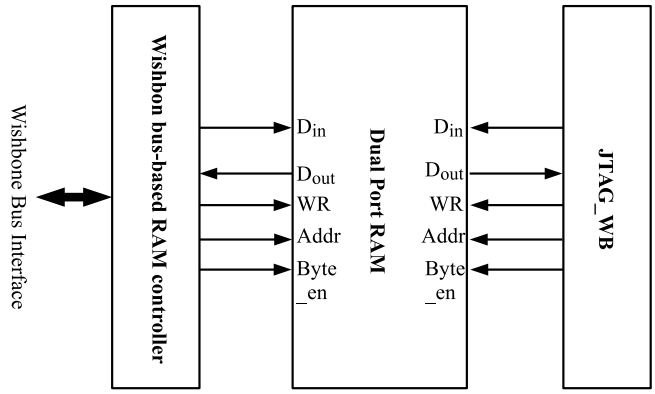
A Wishbone bus-based single port Random Access Memory (RAM).

WB Single Port RAM block diagram:

Figure1 depicts the functional block diagram of single port RAM module.



(a) WB Single port RAM with JTAG_CONNECT configured as "DISABLED".



(b) WB Single port RAM with JTAG_CONNECT configured as "JTAG_WB".

Figure 1: WB Single port RAM

Parameters Description

Table 1: WB single port RAM GUI Parameters.

Name	Description	Permitted values	Default
Dw	RAM Data width in bits	$n \in \mathbb{N}$, $8 \leqslant n \leqslant 1024$	32
Aw	RAM Address width in bits. Total memory size is $2^{Aw} \times Dw$ in bits.	$n \in \mathbb{N}$, $4 \leqslant n \leqslant 31$	12
BYTE_WR_EN	Byte enable	"YES" , "NO"	"YES"
FPGA_VENDOR	The target FPGA vendor. If it is defined as ALTERA, then the altera memory instance (altsyncram) is used in generated Verilog code. Otherwise, the memory RTL code is written completely in Verilog. Note that for some FPGA devices (e.g Cyclone V families) if the byte enable is activated while burst mode is not, the Quartus compiler fail to map the memory into any available FPGA BRMA module.	"ALTERA", "GENERIC"	"ALTERA"
JTAG_CONNECT	Define how the memory is programed at run time using JTAG port: • "DISABLED": The memory cannot be accessed at run time. • "JTAG_WB": The actual memory implements as a dual port BRAM (using altsyncram RAM instance) with the second port is connected to "JTAG_WB" module inside altsyncram. • "ALTERA_IMCE": The actual memory implements as a dual port BRAM with the second port is connected to Altera In-System Memory Content Editor control module.	"DISABLED", "JTAG_WB", "ALTERA_IMCE"	"JTAG_WB"
JTAG_INDEX	A unique index number which will be used for accessing the memory content using JTAG cable. The default value is the processing tile id (CORE_ID) . You can also inter a unique number for each individual memory or any equation with CORE_ID variable . This parameter is valid if the JTAG_CONNECT is not configured as "DISABLED".	$n \in \mathbb{N}$, or $n = f(CORE\_ID)$ $0 \leqslant n \leqslant 127$	CORE_ID
BURST_MODE	Enable the Wishbone bus Incrementing burst mode data transfer. Support Linear burst and 4,8,16-beat wrap burst types.	"DISABLED", "ENABLED"	"ENABLED"

Name	Description	Permitted values	Default
MEM_CONTENT_ FILE_NAME	The memory file name (without file type extension) that is used for writing the memory content either at run time or at initialization time. File Path: • For bus-based SoC the file path is `[ProNoC_work]/SOC/[soc_name]/sw /RAM/[file_type]/MEM_FILE_NAME`. • For NoC-based MPSoC the file path is `[ProNoC_work]/MPSOC/[mpsoc_name] /sw/tile[tile_num]/RAM/ [file_type]/MEM_FILE_NAME` File_type: • **bin:** raw binary format . It will be used by JTAG_WB to change the memory content at runtime. • **memh:** hexadecimal-string format . It will be used for initialing the Generic RAM using $readmemh command. • **mif**: memory initialization file format. This file can be used to initialize Altera FPGA memory. Also if the JTAG_CONECT is selected as ALTERA_IEMC it can be used for changing the memory content at run time.	Any arbitrary name	”ram0”
INITIAL_EN	If selected as ”YES”, the memory content will be initialized at compilation time using MEM_CONTENT_FILE_NAME.	”YES”, ”NO”	”NO”

WB Dual Port RAM

A Wishbone bus-based dual port Random Access Memory (RAM).

WB Dual Port RAM block diagram:

Figure2 depicts the functional block diagram of dual port RAM module.

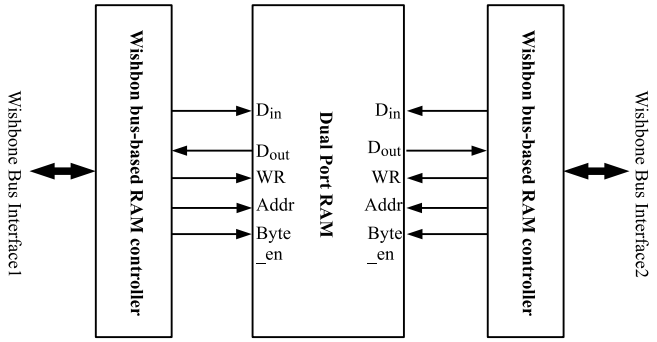


Figure 2: WB Dual Port RAM block diagram

Parameters Description

The WB dual port RAM shares all the WB single port RAM except the JTAG_CONNECT and JTAG_INDEX parameters.