Discrete Cosine Transform (DCT)
IP Core User Manual

Unicore Systems Ltd

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60-A Saksaganskogo St
Office 1
Kiev 01033
Ukraine
Phone:  +38-044-289-87-44
Fax: :  +38-044-289-87-44
E-mail: o.uzenkov@unicore.co.ua
URL:    www.unicore.co.ua
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GENERAL INFORMATION

DCT soft core is the unit to perform the Discrete Cosine Transform (DCT). It performs two-dimensional 8 by 8 point DCT for the period of 64 clock cycles in pipelined mode.

FEATURES

Key features

- more than 300 MHz sampling frequency, 64-cycle calculation period,
- approximately 330 CLBs and 4 DSP48E in Virtex-5 device,
- 2 DSP48E when the scaled output data mode is used,
- 8-bit input data,
- 11-bit coefficients,
- 12 – bit results,
- pipelined mode,
- latent delay from input to output is 132 clock cycles,
- structure optimized for Xilinx Virtex™, Spartan™ FPGA devices.

Design features

- **DCT core intended for transforming data into a format that can be easily compressed**.

The characteristics of the DCT make it extremally suited for image compression algorithms. DCT removes spatial data redundancies in two-dimensional data. Therefore, DCT is used in JPEG and MPEG standards of image compression procedures.

In general, the two-dimensional DCT transforms an nxn data array into an nxn result array. Firstly the n-point DCT transforms the columns, then it transforms the rows.

The 8-point DCT is calculated due to the equations

$$Y(0) = \frac{1}{\sqrt{8}} \sum_{m=0}^{7} X(m), \text{ and } Y(k) = \frac{1}{2} \sum_{m=0}^{7} X(m)\cos\frac{(2m+1)k\pi}{16}, \quad k=1,2,...,7,$$

where $Y(k)$ is k – th DCT coefficient.

The input 8x8 image data block consists of integers in the range from 0 to 255. Before the DCT calculation the mean value 128 is subtracted from input data to minimize the redundancy in the input data block. The core can compute input data in range −128 to 127 as well. Then the mean value 128 is not subtracted.

After the DCT is calculated, the data can be reduced to concentrate the important information into a few DCT results, leaving the remaining coefficients equal to zero. That means that the image energy is concentrated in a few DCT coefficients.

Comparing to the Discrete Fourier Transform, the DCT has the following advantages:

- High image energy compaction
- Lower blocking artifacts
- Real data, coefficients and arithmetic only.
- Effective DCT algorithm

To minimize the amount of calculations, the Arai, Agui, and Nakajama 8-point DCT algorithm is used. This algorithm consists in the following calculations

$$b0:=a(0) + a(7); \quad b1:=a(1)+a(6); \quad b2:=a(3) - a(4); \quad b3:=a(1) - a(6);$$
$$b4:=a(2) + a(5); \quad b5:=a(3) +a(4); \quad b6:=a(2) - a(5); \quad b7:=a(0) - a(7);$$

$$c0:=b0 + b5; \quad c1:=b1 - b4; \quad c2:=b2 + b6; \quad c3:=b1+b4;$$
$$c4:=b0 - b5; \quad c5:=b3 +b7; \quad c6:=b3 + b6; \quad c7:=b7;$$

$$d0:=c0 + c3; \quad d1:=c0 - c3; \quad d2:=c2; \quad d3:=c1+c4;$$
$$d4:=c2 - c5; \quad d5:=c4; \quad d6:=c5; \quad d7:=c6; \quad d8:=c7;$$

$$e0:=d0; \quad e1:=d1; \quad e2:=m3*d2; \quad e3:=m1*d7;$$
$$e4:=m4*d6; \quad e5:=d5; \quad e6:=m1*d3; \quad e7:=m2*d4; \quad e8:=d8;$$

$$f0:=e0; \quad f1:=e1; \quad f2:=e5+e6; \quad f3:=e5 - e6;$$
$$f4:=e3 +e8; \quad f5:=e8 - e3; \quad f6:=e2+e7; \quad f7:=e4+e7;$$

$$sa(0):=f0; \quad sa(1):=f4+ f7; \quad sa(2):=f2; \quad sa(3):= f5 - f6;$$
$$sa(4):=f1; \quad sa(5):=f5+f6; \quad sa(6):=f3; \quad sa(7):=f4 - f7;$$

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for i in 0 to 7 loop
   y(i) := sa(i)*s(i)*4.0;
end loop;
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where
a(i), y(i) are input and output data;
$m1= \cos(\pi/4.0)$; $m2 = \cos(\pi*3/8)$; $m3 = \cos(\pi/8) - \cos(\pi*3/8)$; $m4 = \cos(\pi*/8) + \cos(\pi*3/8)$;
$s(0) = 0.5/\sqrt{2}$, $s(i) = 0.25/\cos(\pi*i/16)$, i=1,2,...,7.

This algorithm has only 13 multiplies. Its 8 rest multiplies can be discarded when the outputs are considered to be scaled ones. In this situation the proper scaling is usually performed in the stage of DCT coefficient dividing to the scale factors before the Huffman coding.

• **Highly pipelined calculations**

The input data arrays 8x8 are loaded in data by data mode with the period which is equal to the clock period. The output data arrays are outputted in the similar manner. Time threscholds between data arrays can be absent, and high maximum clock frequency of the core is achieved due to the pipelined calculations.

The period of calculations of 64 word arrays is equal to 64 clock cycles.

The input and output data have the normal order.

• **Low hardware cost**

Due to the widely used resource sharing the hardware volume is rather small. The multiplier number is equal to 4. When the output results are scaled then the multiplier number is decreased to 2.

The intermediate result arrays are stored and transposed using the FIFO buffers based on the SRL16 elements. Due to that the Block RAMs are not used. Besides, the latent delay between first data input and the first data output is minimized to 132 clock cycles.

• **High precision computations**

The quality of decoded image depends on the computation precision, for example, when photographic picture compression. This core has 12-bit output data width, the maximum error is not succeeded 3 least significant bits (for 12-bit width), which means the maximum MSE 0.25%.

The coefficients s(i) and mi have 11-bit precision (10 significant bits plus sign).

INTERFACE

Symbol

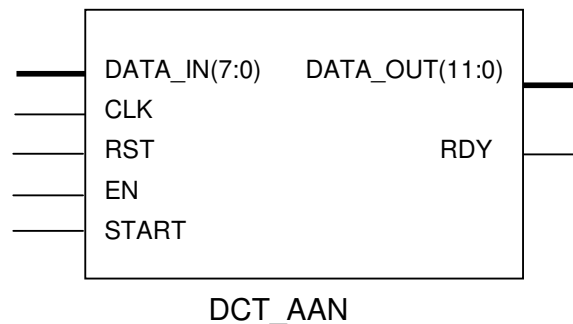Figure1 illustrates DCT_AAN core symbol.

DCT_AAN

Figure 1. DCT_AAN core symbol.

Signal description

The descriptions of the core signals are represented in the table 1.

SIGNAL	TYPE	DESCRIPTION
CLK	input	Global clock
RST	input	Global reset
START	input	DCT start
EN	input	Clock enable
DATAIN[7:0]	input	Input data
DATA_OUT[15:0]	output	Output data
READY	output	Result ready strobe

Table 1. DCT_AAN core signal description.

Data Format

Input data are 8 bit wide two's complement integers. Depending on the generic constant d_signed they can be considered as signed or unsigned ones. When unsigned, from all data the mean value 128 is subtracted.

Output data are 12 bit wide two's complement integers. When the input signal is changed in range –128 to 127 then the output signal is changed in range –1024 to 1016. When the output data are scaled, then they are changed in range –2048 to 2032.

Typical Core Interconnection

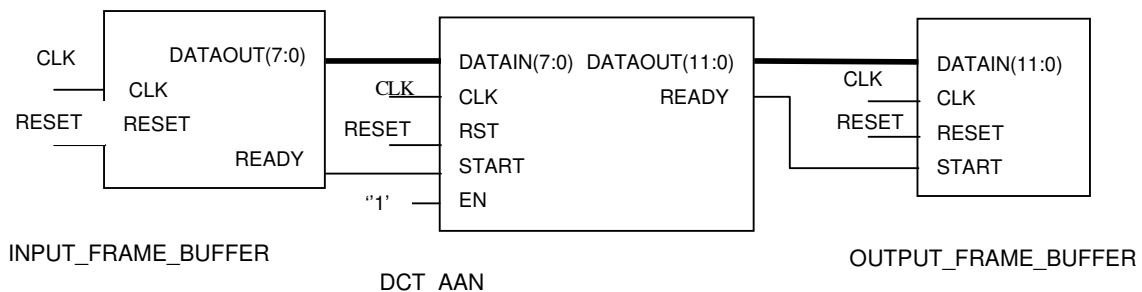Typical core interconnection is shown on figure 2.

Figure 2. Core interconnection

Components:

- DCT_AAN – DCT core
- INPUT_FRAME_BUFFER is RAM buffer which loads 8x8 blocks into DCT core in row by row mode
- OUTPUT_FRAME_BUFFER is RAM buffer which stores 8x8 blocks of DCT coefficients in row by row mode

IMPLEMENTATION DATA

Performance

Tables 2 and 3 illustrate the DCT_AAN core performance in Xilinx devices for normal and scaled output data respectively. The core was synthesized using Xilinx ISE-9.2.

Target device	Spartan3DSP-4	Virtex2P	Virtex4-12	Virtex5-3
Area, CLB, CLB slices	629	742	685	297
System clock, Fmax	155 MHz	210 MHz	310 MHz	370 MHz

Table 2. Implementation data for normal output data and with 4 DSP48 units

Target device	Spartan3DSP-4	Virtex2P	Virtex4-12	Virtex5-3
Area, CLB, CLB slices	630	731	719	311
System clock, Fmax	150 MHz	185 MHz	300 MHz	380 MHz

Table 3. Implementation data for scaled output data and with 2 DSP48 units

Testbench

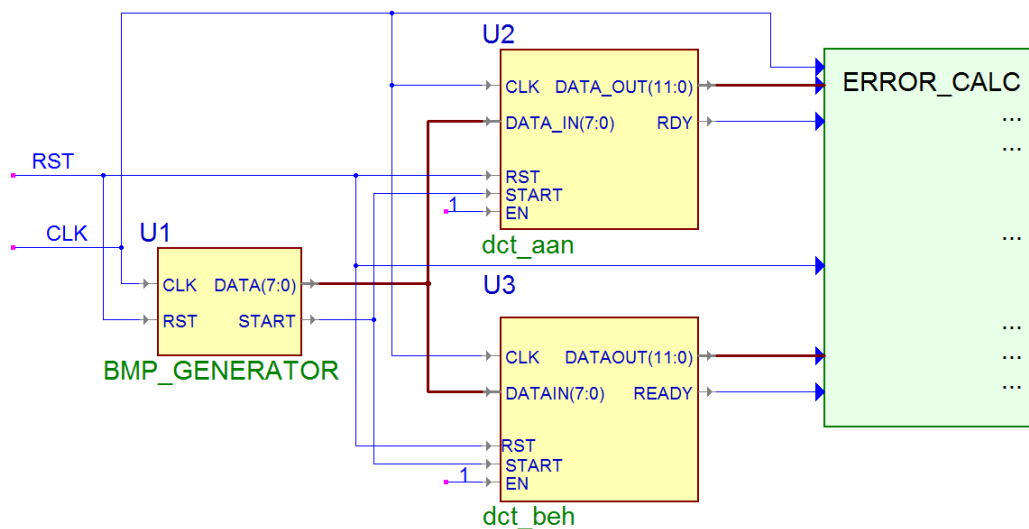The Figure 3 illustrates the testbench for the core

Figure 3. Testbench structure

Component BMP_GENERATOR generates the dataflow of testing arrays. In one mode it generates predefined arrays, in another mode does randomized ones.

The tested instance DCT_AAN and the reference instance DCT_BEH are switched on in parallel to the source BMP_GNERATOR. DCT_BEH is the behavioral model of the DCT processor. It computes 2D DCT using the floating point calculations. Its results are rounded to 12 bits. Therefore, it serves as the standard model.

The process ERROR_CALC calculates differences in the output data of DCT_AAN and DCT_BEH. The resulting signals are ERROR which is result of signal subtraction, SERROR as the sum of squared errors for a single data arrays, and QUADMEAN which is the resultic mean square error value for the current array.