

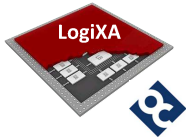
# ESoCL

## Ethernet Switch on Configurable Logic

### Release Bulletin

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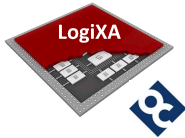
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## 1. LATEST RELEASE

Version: 0x0001

Release: 0x0000

Manufacturer ID: 0x71022

Device ID: 0x001

*Manufacturer ID and Device ID can be read from ESoCL register CTRL\_ID.*

*Version and Release number can be read from ESoCL register CTRL\_VERSION.*

## Changes

#	Changes	Solved	Status
	Initial release of the ESoCL IP		

## Change details

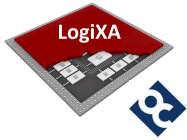
# - CHANGE
Affected files

## Resources

Resources: 8 port ESoCL		Target: EP3CLS100F484I7 (Altera Cyclone 3LS)	
Units	Logic cells	Memory bits	Fmax
Generic (Arbiters, Control)	1217	8192 bits 1 M9K Block	CLK_CTRL ≤ 50MHz CLK_DATA ≤ 140MHz CLK_SEARCH ≤ 100MHz
RGMII Port (MAC, MAL, Storage, Processing)	5904	337328 bits 51 M9K Blocks	
Search engine	945	582400 bits 72 M9K Blocks	
Total	49394	337328 bits 481 M9K Blocks	

## Tools

- Altera Quartus II 10.1
- Modelsim AE 6.6d



## **2. PREVIOUS RELEASES**