Firmware Design Document

Module Name: Management Module

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Revision History

Date	Author	Issue	Comment
14/6/2006	Zheng Cao	1.0	First Version.

Reference

[1] 10G Ethernet Mac System Design Issue 1.0
[2] Xilinx LogiCORE 10-Gigabit Ethernet MAC User Guide
[3] IEEE 802.3ae Media Access Control (MAC) Parameters, Physical Layers, and Management Parameters for 10 Gb/s Operation

Contents

List of Tables

List of Figures

1 Introduction

The document describes the design of the management module used in the Opencores 10-Gigabit Ethernet project. MDIO function of this module part is designed to 10-Gigabit Ethernet IEEE 802.3 ae-2002. Configuration and statistic functions are also implemented.

The MAC design is loosely based on the Xilinx LogiCORE 10-Gigabit Ethernet MAC, where the management function is similar with it too. The management module will be specifically designed to interface the client and the physical layer.

2 Detailed Design

2.1 Module Description

The Management Module provides the manage interface to the client. Client can configure MAC and PHY via this interface. Besides, statistic information is provided too. Figure 2-1 shows a block diagram of Management Module, with the interfaces to the client, physical, transmit engine and receive engine.

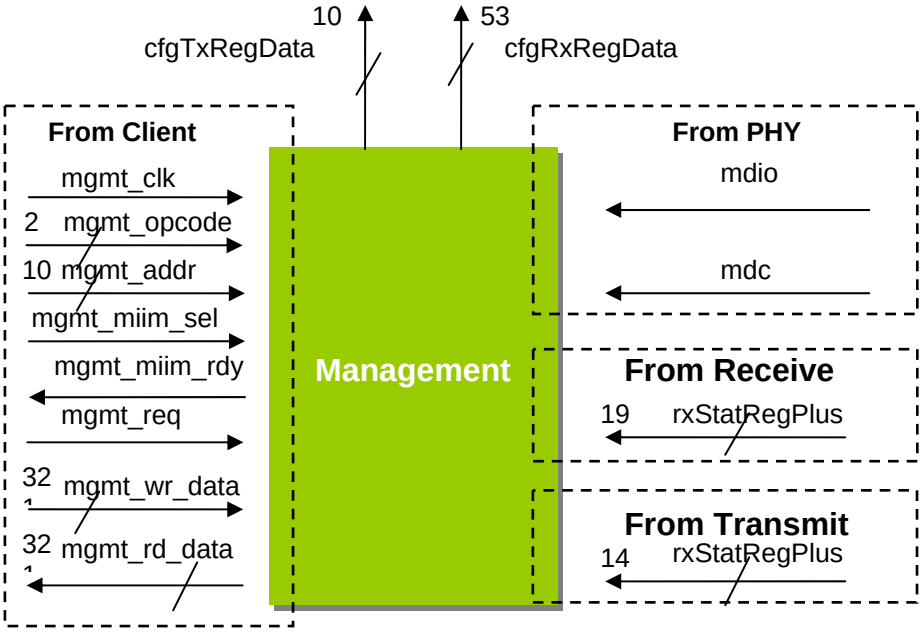

Figure 2-1 Diagram of the Management Block

2.2 Module Ports

Table 2-1 lists the I/Os that interface to the client.

Port Name	Direction	Description
mgmt_clk	Input	Client clock(25MHZ)
mgmt_opcode[1:0]	Input	Define operation (Read, Write or MDIO)
mgmt_addr[9:0]	Input	Address of registers to be operated
mgmt_wr_data[31:0]	Input	Data to be written to register
mgmt_rd_data[31:0]	Output	Data read from register
mgmt_miim_sel	Input	When asserted, MDIO interface is selected
mgmt_miim_rdy	Output	When asserted, the MDIO has completed any pending transaction operation and is ready for new transaction.
mgmt_req	Input	Used to request a MDIO transaction or a read transaction to statistic registers

Table 2-1 Client-side interface

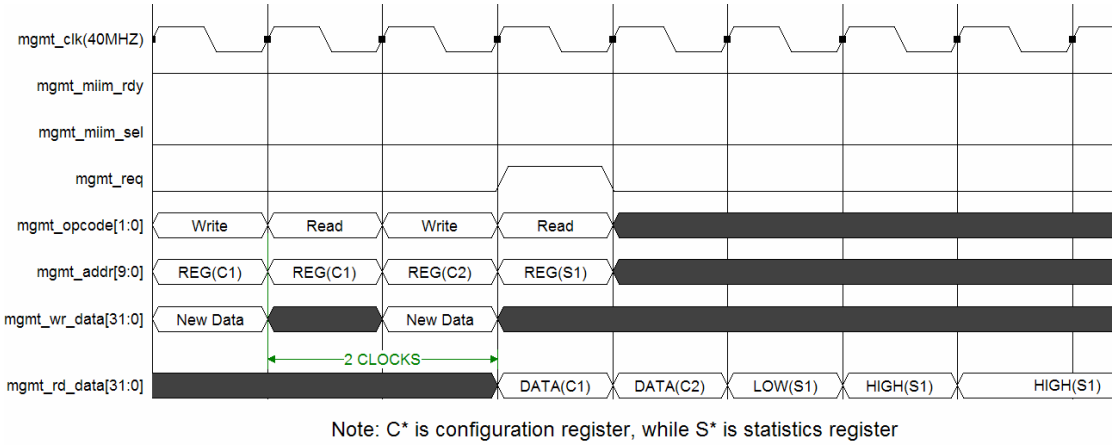

Figure 2-2 Internal Register Operating Timing

Operating Timing of Internal registers (configuration and statistics registers) is shown in Figure 2-2. New value written to internal registers will be valid one clock after the write request. The written value will appear on mgmt_rd_data two cycles after the write request, which is the same as read operation. Statistics registers are 64bit width, so its reading process will take 2 clocks.

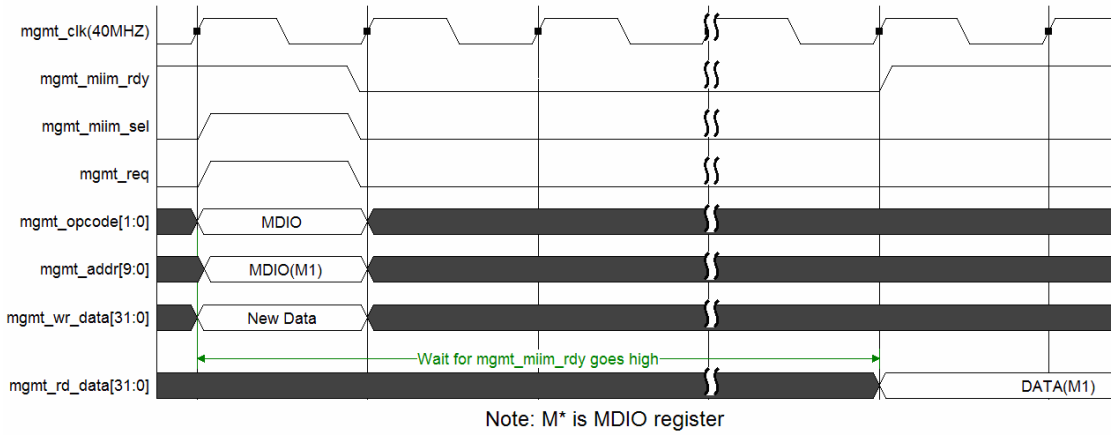

Figure 2-3 MDIO Register Operating Timing

When a MDIO request is send out, mgmt_miim_rdy will be disserted, to indicate that a MDIO operation is being processed. Data read from MDIO register will be valid when mgmt_miim_rdy asserted again.

Commands through client are listed in Table 2-2:

	mgmt_miim_sel	mgmt_req	mgmt_opcode	mgmt_addr[9]
Configuration Read	’0’	‘0’	“11”	‘1’
Configuration Write	‘0’	‘0’	“01”	‘1’
Statistics Read	‘0’	‘1’	“11”	‘0’
MDIO Read	‘1’	‘1’	“10”	X
MDIO Write	‘1’	‘1’	“01”	X

Table 2-2 Client-side interface

Table 2-3 lists the I/Os that interface to PHY.①

Port Name	Direction	Description
Mdio	Inout	Serial data line of MDIO interface
Mdc	Input	MDIO clock (lower than 2.5MHZ)

Table 2-3 PHY-side interface

MDIO timing specification is defined in IEEE 802.3-ae Clause 45. Mdc is the clock signal of MDIO interface, it is generated from mgmt_clk. Its frequency is :

Freq (mdc) = Freq (mgmt_clk) / (manage_config [4:0] * 2)

MDIO read and writing timing are shown in Figure 2-4 and Figure 2-5.

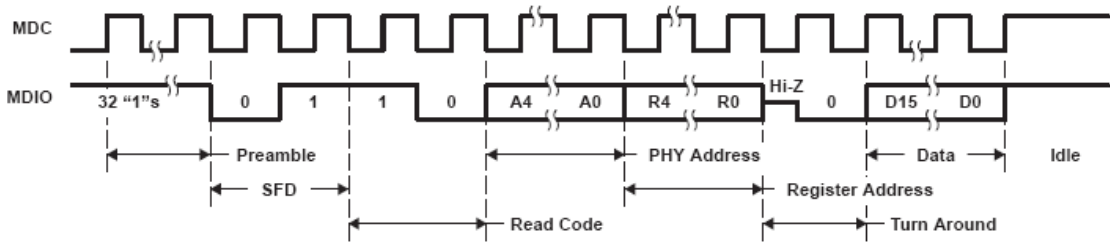

Figure 2-4 MDIO Read Timing

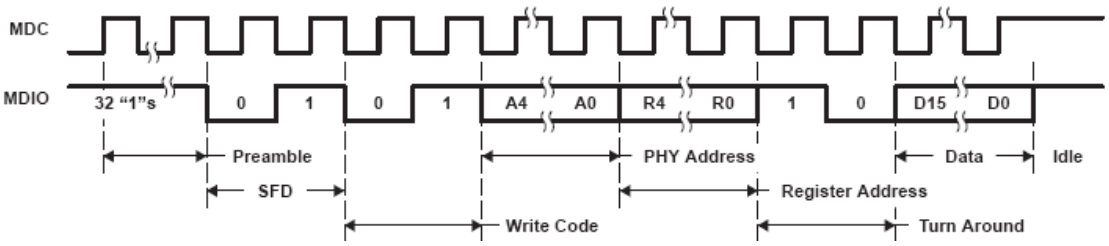

Figure 2-5 MDIO Write Timing

Table 2-3 lists the I/Os that output from management submodule.

Port Name	Direction	Description
cfgRxRegData[52:0]	Output	The value from receive configure registers. Include both receive and part of reconciliation configure information.
cfgTxRegData[9:0]	Output	The value from transmit configure registers.

Table 2-4 Management-side interface

Table 2-4 lists the I/Os that interface from Receive Engine.

Port Name	Direction	Description
rxStatRegPlus [18:0]	Input	Each bit presents an add operation to a statistic register. These signals should only last for one cycle. For example, when rxStatRegPlus [0] is asserted for one cycle, the counter of Control Frames Received OK register in Management Module will plus one.

Table 2-5 Transmit-side interface

Table 2-5 lists the I/Os that interface from Transmit Engine.

Port Name	Direction	Description
txStatRegPlus [14:0]	Input	Each bit presents an add operation to a statistic register. These signals should only last for one cycle. For example, when txStatRegPlus [0] is asserted for one cycle, the counter of total bytes transmitted register in Management Module will plus one.

Table 2-6 Transmit-side interface

2.3 Module Design

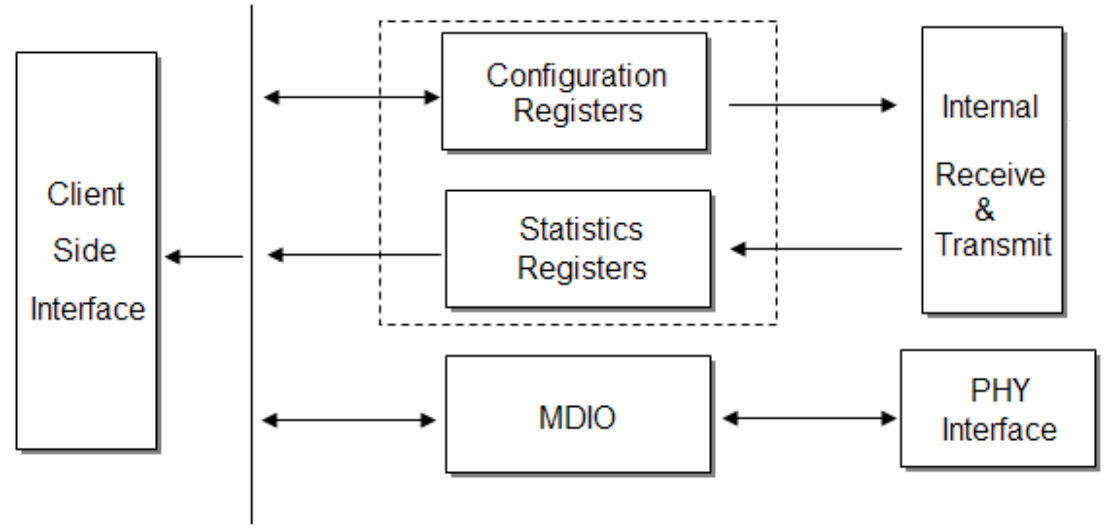

Figure 2-6 internal structure of the Management Module

Management Module is implemented with two sub-modules, which are:

- **Manage registers**

  This sub-module contains configuration and statistics registers. It responds read write requests from client side. Read write requests to MDIO registers will be dispatched to MDIO module.

  Configuration registers are listed below:

mgmt_addr [9:0]	Description
0x200	Receiver Configuration Word 0
0x240	Receiver Configuration Word 1
0x280	Transmitter Configuration
0x2c0	Flow Control Configuration
0x300	Reconciliation Sublayer Configuration
0x340	Management Configuration

Table 2-7 Configuration Registers

Definitions of configuration registers are described below in details:

Bit	Description
31:0	Lower 32bit of MAC Address

Table 2-8 Receiver Configuration Word 0

Bit	Description
15:0	Higher 16bit of MAC Address
26:16	Reserved
27	VLAN Enable
28	Receive Enable
29	In-band FCS Enable. When asserted, FCS filed will be sent to client.
30	Jumbo Frame Enable. In this design, Jumbo length is 9K byte.
31	Receiver reset.

Table 2-9 Receiver Configuration Word 1

Bit	Description
26:0	Reserved
27	VLAN Enable
28	Transmit Enable
29	In-band FCS Enable
30	Jumbo Frame Enable
31	Transmit Reset

Table 2-10 Transmit Configuration Word

Bit	Description
28:0	Reserved
29	Flow Control Enable(Receive Engine)
30	Flow Control Enable(Transmit Engine)
31	Reserved

Table 2-11 Flow Control Configuration Word

Bit	Description
27:0	Reserved
28	Local Fault Received
29	Remote Fault Received
31:30	Reserved

Table 2-12 Reconciliation Sublayer Configuration Word

Bit	Description
4:0	Used to generate MDC signal at 2.5MHZ (or lower)
31:5	Reserved

Table 2-13 Management Configuration Word

Statistics Registers are 64bit wide, they are listed below:

mgmt_addr [9:0]	Description
0x000	Number of error free frames received
0x001	Number of frames that have failed in FCS check
0x002	Number of broadcast frames successfully received
0x003	Number of multicast frames successfully received
0x004	Number of frames successfully received, with length equal to 64
0x005	Number of frames successfully received, with length between 65 and 127

0x006	Number of frames successfully received, with length between 128 and 255
0x007	Number of frames successfully received, with length between 256 and 511
0x008	Number of frames successfully received, with length between 512 and 1023
0x009	Number of frames successfully received, with length between 1024 and MAX length
0x00a	Number of control frames successfully received
0x00b	Number of frames which are longer than MAX
0x00c	Number of tagged frames successfully received
0x00d	Number of pause frames successfully received
0x00e	Number of frames whose type filed haven't been defined in IEEE 802.3*
0x00f	Number of error free frames with large size
0x010	Number of frames whose length are less than 64byte
0x011	Number of fragment frames successfully received.
0x012	Bytes have been received
Transmit Statistics Registers (haven't been supported in transmit engine yet)	
0x013	Bytes have been transmitted.
0x020	Number of error free frames transmitted
0x021	Number of broadcast frames successfully transmitted
0x022	Number of multicast frames successfully transmitted
0x023	Number of frames with underrun error transmitted
0x024	Number of control frames successfully received
0x025	Number of frames successfully transmitted, with length equal to 64
0x026	Number of frames successfully transmitted, with length between 65 and 127
0x027	Number of frames successfully transmitted, with length between 128 and 255
0x028	Number of frames successfully transmitted, with length between 256 and 511
0x029	Number of frames successfully transmitted, with length between 512 and 1023
0x02a	Number of frames successfully transmitted, with length between 1024 and MAX length
0x02c	Number of tagged frames successfully transmitted
0x02d	Number of pause frames successfully transmitted

Table 2-14 Statistics Registers

- **MDIO:** This sub-module implements MDIO logic. MDIO is the interface between MAC and PHY layer. MAC layer can configure PHY and read PHY status through MDIO. MDIO is a serial communication protocol. See Figure 2-4 and Figure 2-5 for details.

2.4 Block Diagram

In this section, diagram of each sub-modules will be listed with some descriptions.

Management Registers

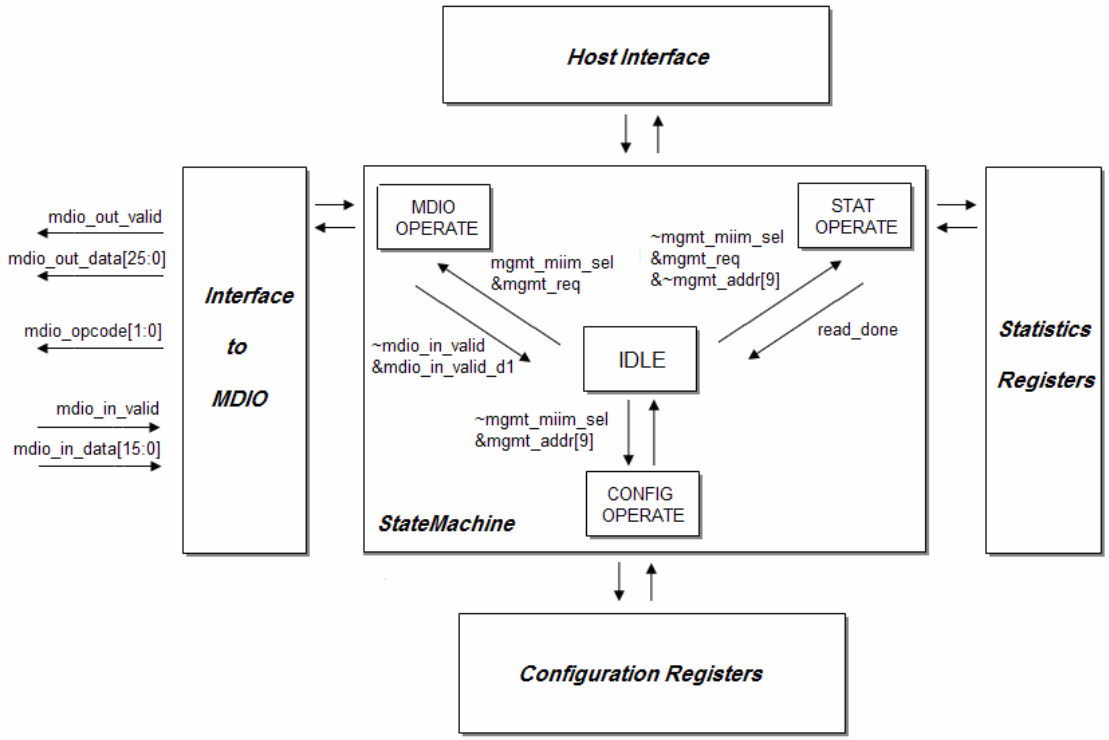

Figure 2-7 block diagram of Management Register Sub-module

MDIO

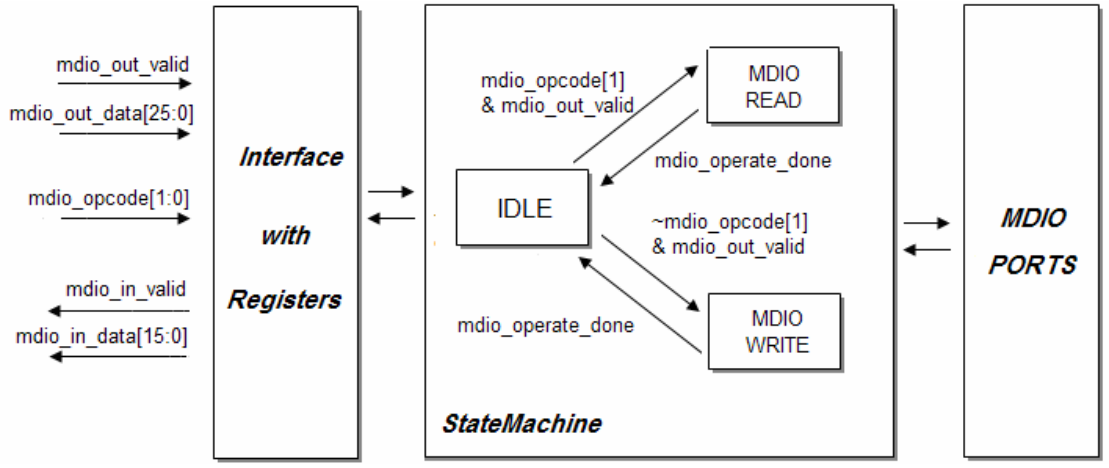

Figure 2-8 block diagram of MDIO Sub-module

2.5 Code Listing

Source Code Name	Version	Date
management_top.v	1.0	
manage_registers.v	1.0	
mdio.v	1.0	

Table 2-15 Code Listing

3 Traceability Matrix

802.3ae Clause	Implemented In
1	

Table 3-1 Traceability Matrix

4 Abbreviation

FPGA	Field Programmable Gate Array
HDL	Hardware Description Language
PHY	Physical
UML	Unified Modelling Language