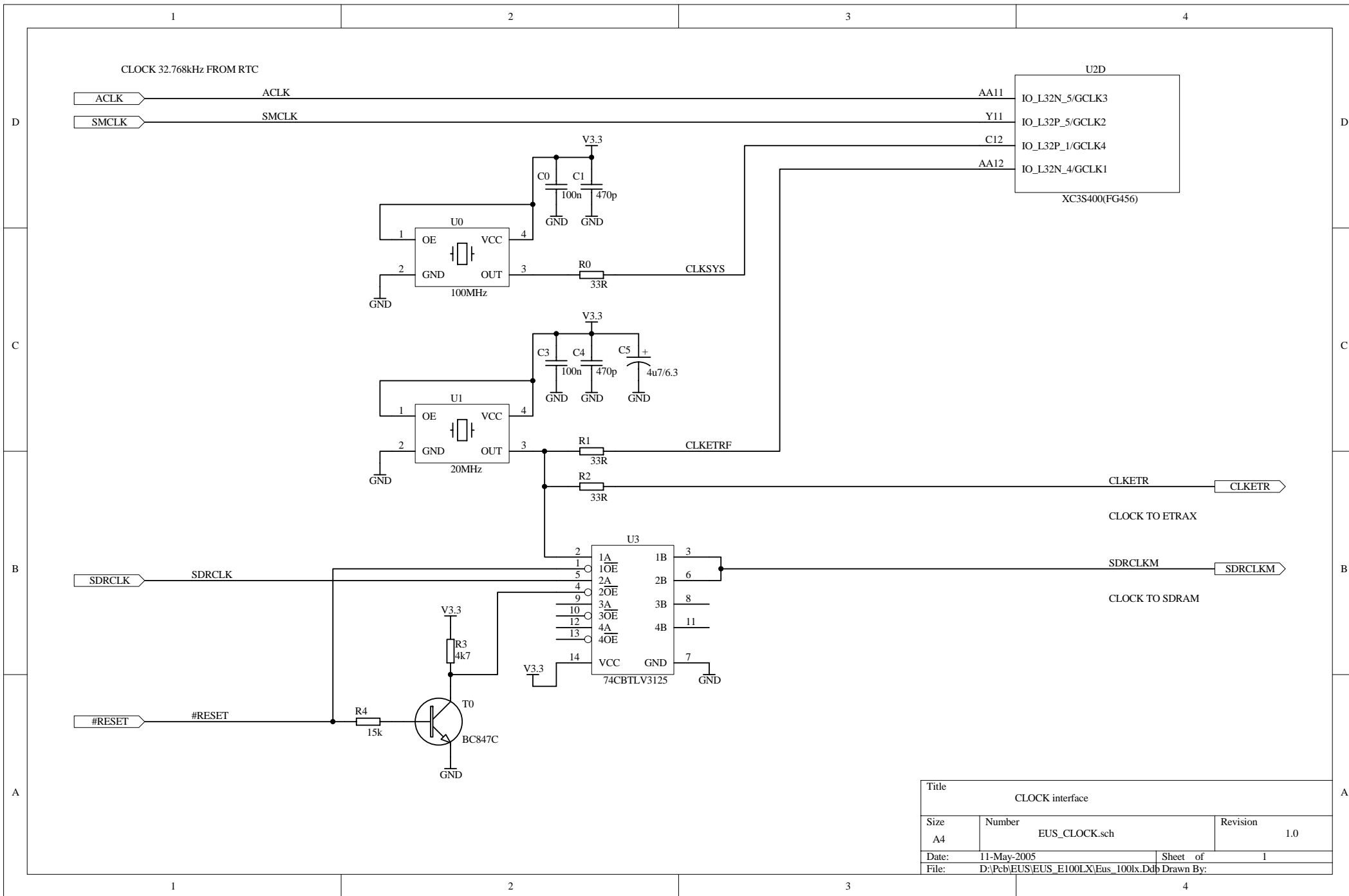
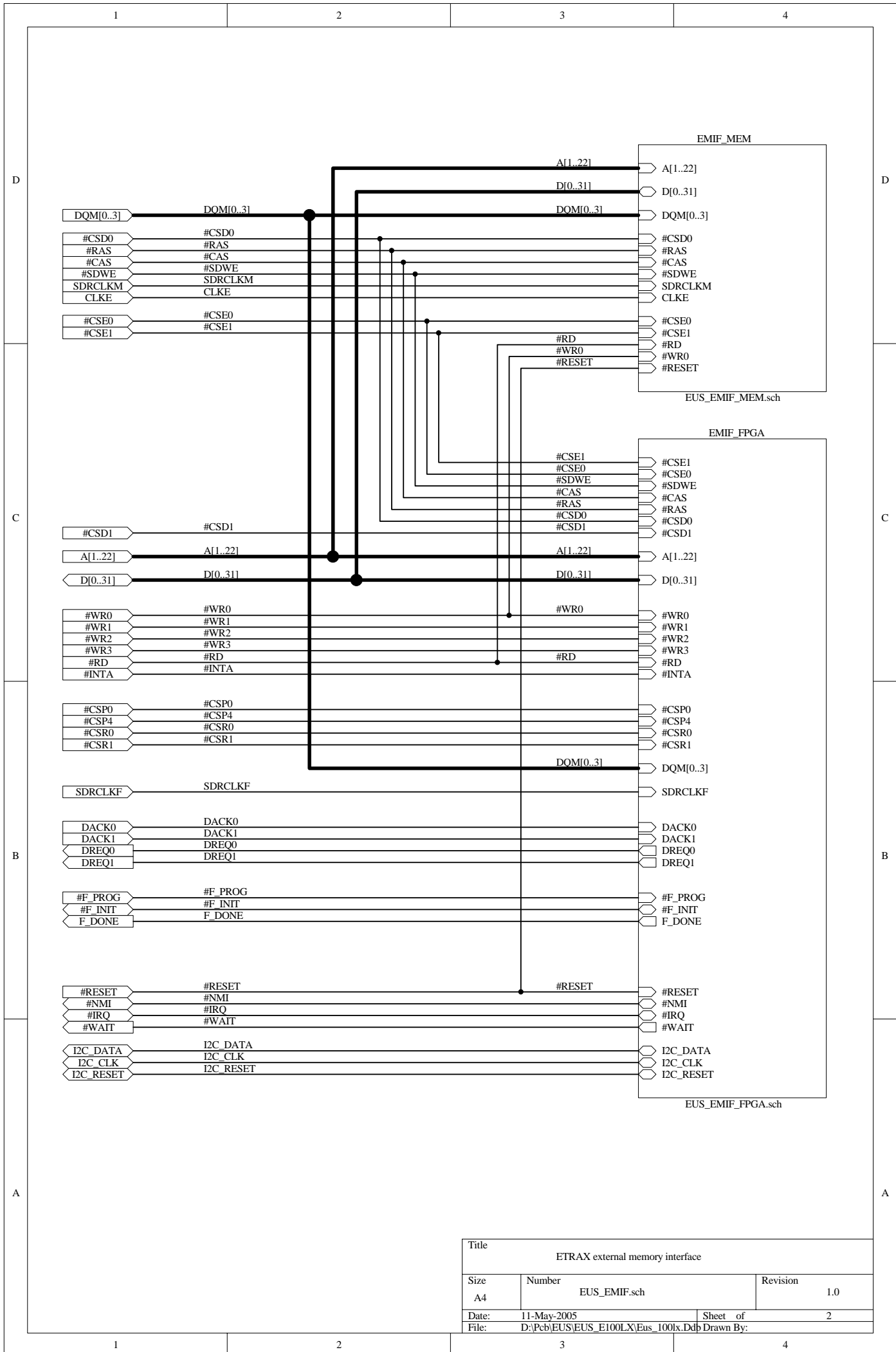


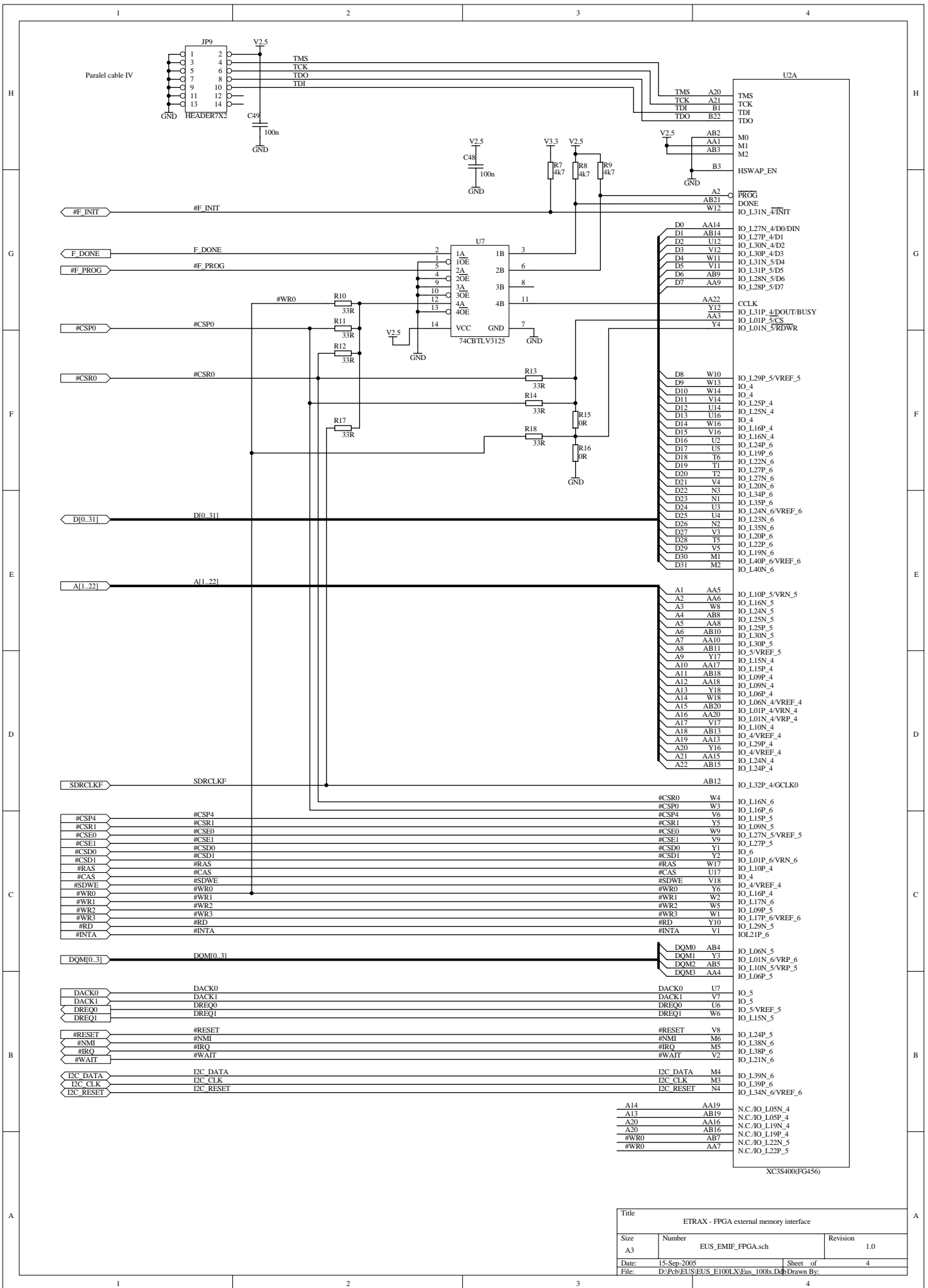
Title			
EUS BOARD			
Size	Number	Revision	1.0
A3	EUS.sch		
Date:	11-May-2005	Sheet of	0
File:	D:\Fcb\EUS\EUS_E100LX\Eus_100LX.Ddb Drawn By:		



Title			
CLOCK interface			
Size	Number	Revision	
A4	EUS_CLOCK.sch	1.0	
Date:	11-May-2005	Sheet of	1
File:	D:\Pcb\EUS\EUS_E100LX\Eus_100lx.Ddb Drawn By:		

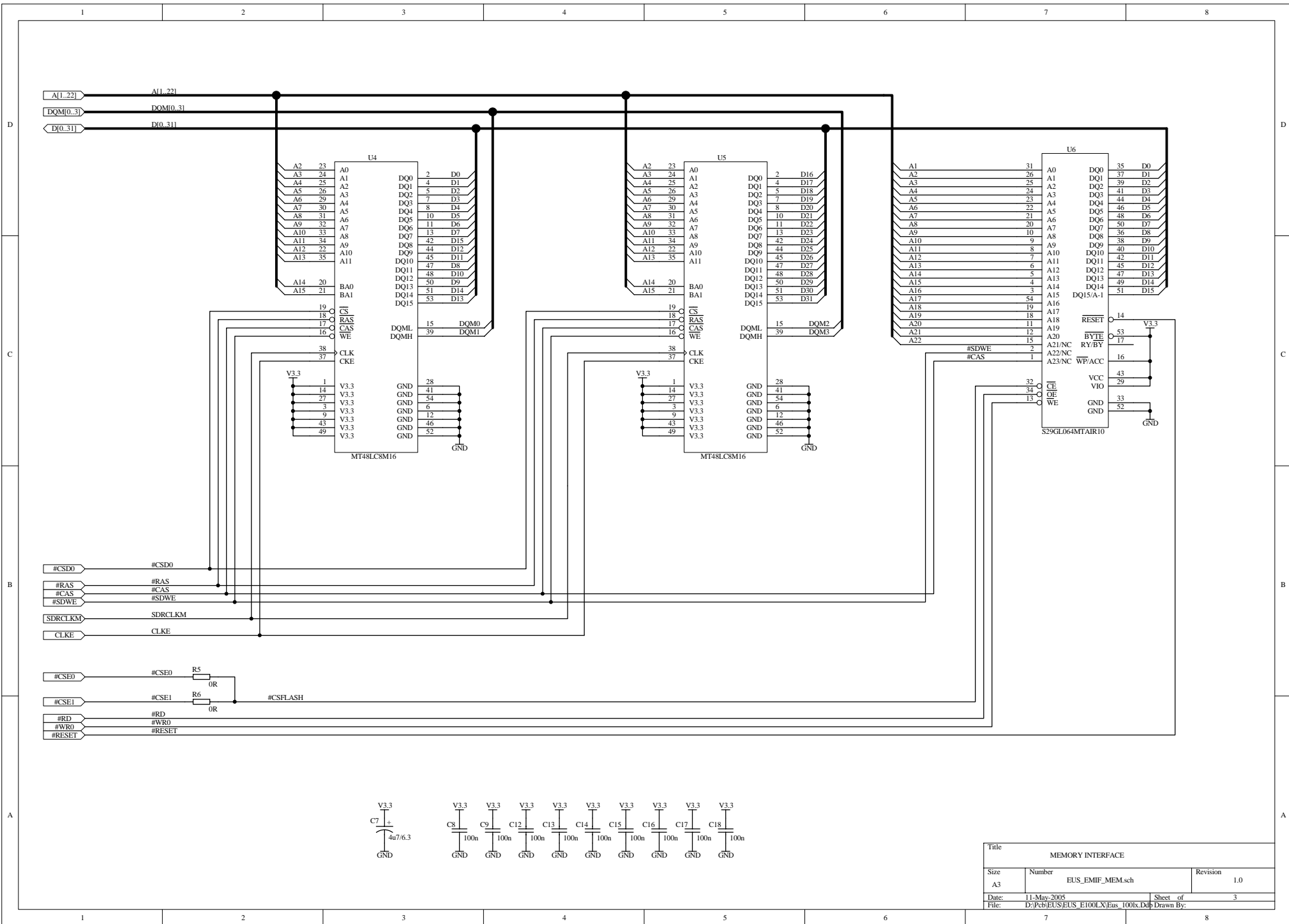


Title			
ETRAX external memory interface			
Size	Number	Revision	
A4	EUS_EMIF.sch	1.0	
Date:	11-May-2005	Sheet of	2
File:	D:\Pcb\EUS\EUS_E100LX\Eus_100lx.Ddb Drawn By:		

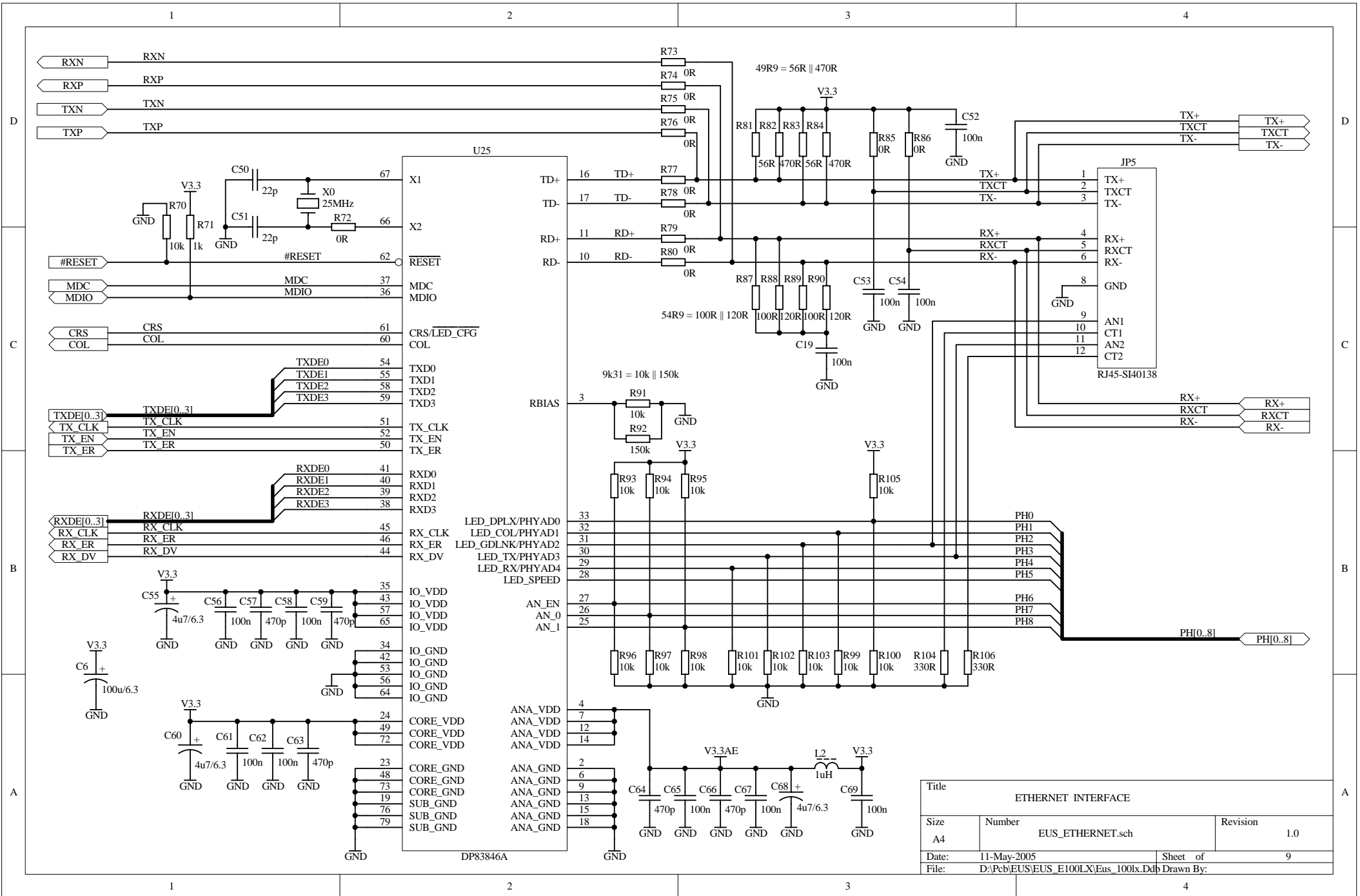


Title			
ETRAX - FPGA external memory interface			
Size	Number	Revision	1.0
A3	EUS_EMIF.FPGA.sch		
Date:	15-Sep-2005	Sheet of	4
File:	D:\Pcb\EUS\EUS_E100LX\Eus_100k.Ddb	Drawn By:	

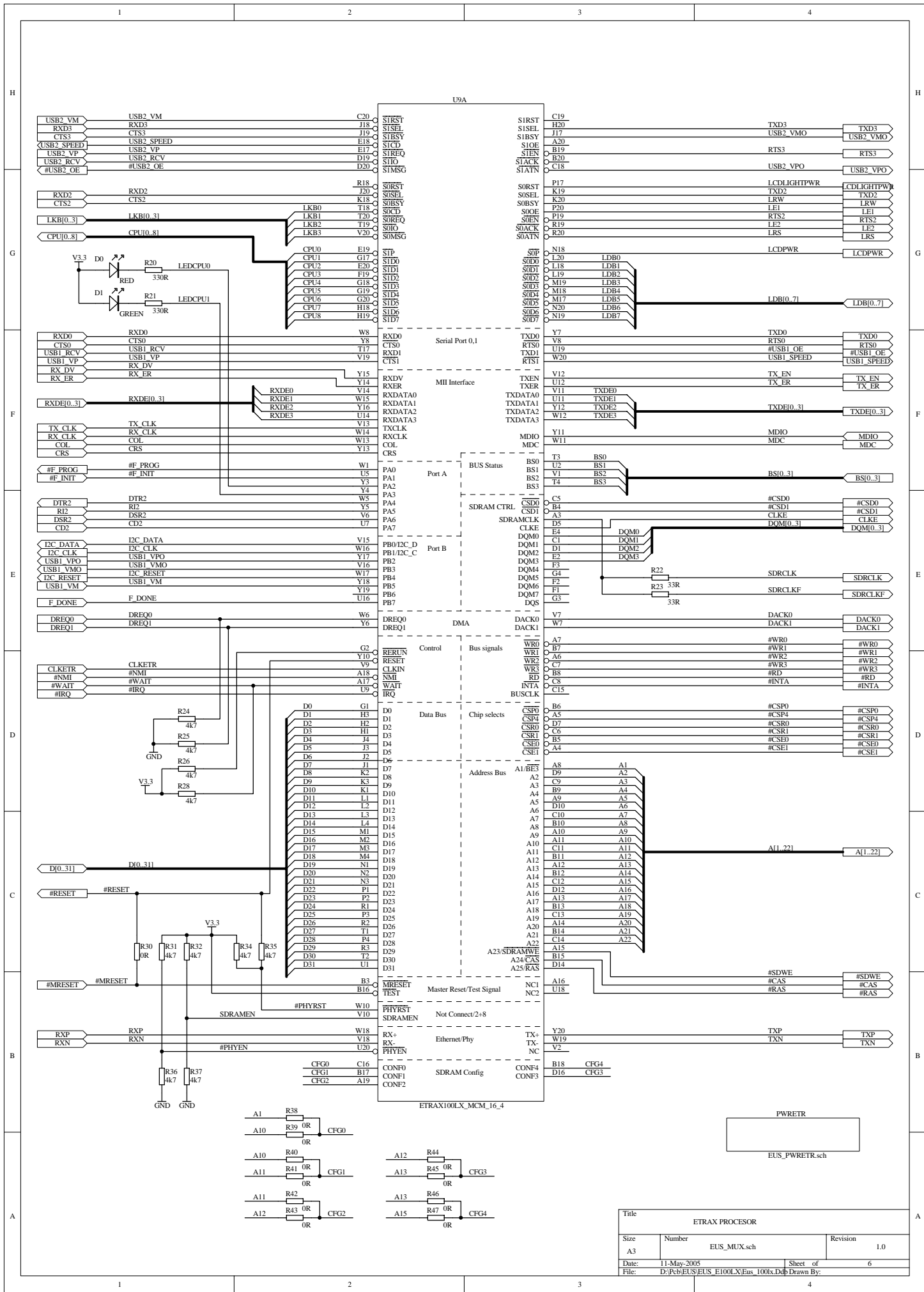
XC3S4000(FG456)



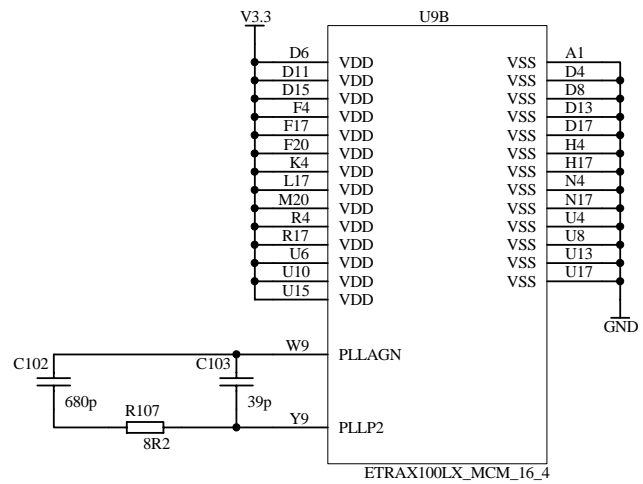
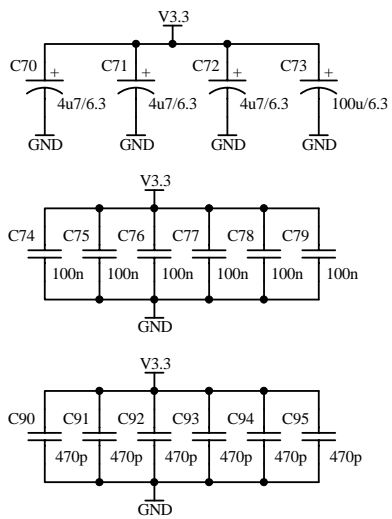
Title		
MEMORY INTERFACE		
Size	Number	Revision
A3	EUS_EMIF_MEM.sch	1.0
Date:	11-May-2005	Sheet of 3
File:	D:\Fcb\EUS\EUS_E100LX\Eus_100LX.Ddb	Drawn By:



Title		
ETHERNET INTERFACE		
Size	Number	Revision
A4	EUS_ETHERNET.sch	1.0
Date:	11-May-2005	Sheet of 9
File:	D:\Pcb\EUS\EUS_E100LX\Eus_100Lx.Ddb Drawn By:	



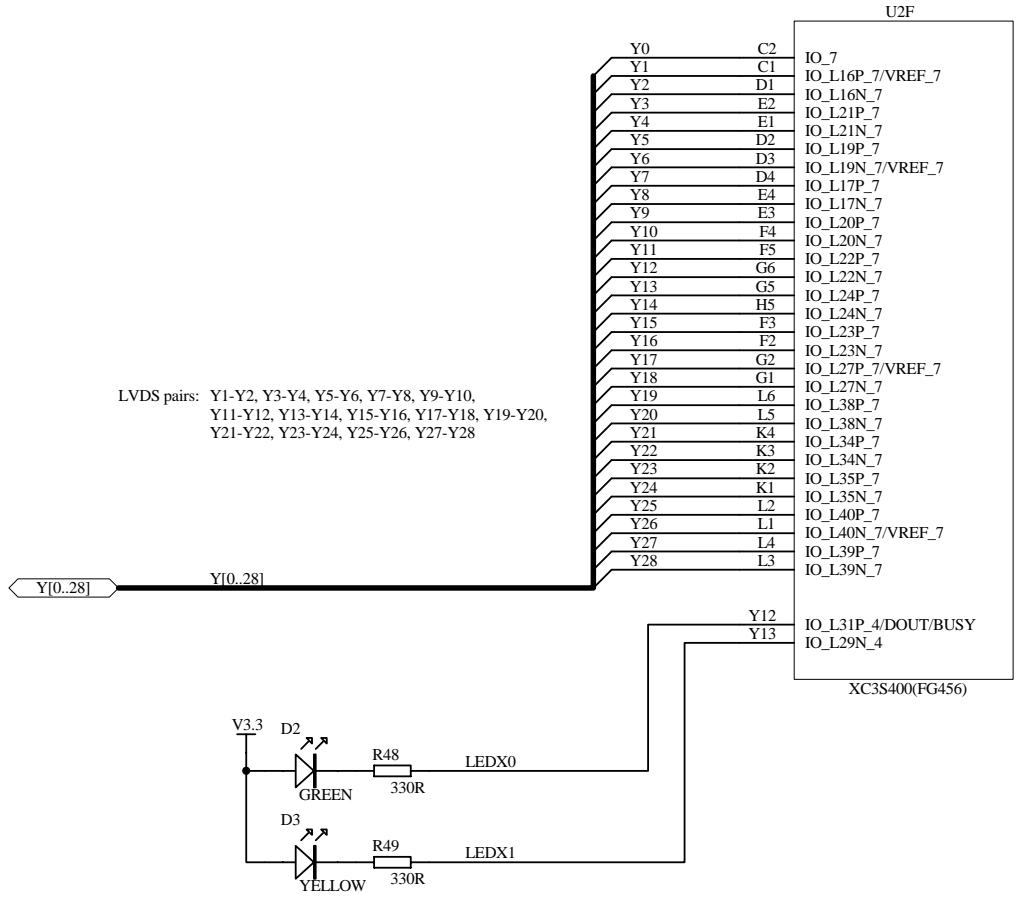
Title			
ET-RAX PROCESSOR			
Size	Number	Revision	
A3	EUS_MUX.sch	1.0	
Date:	11-May-2005	Sheet of	6
File:	D:\Pcb\EUS\EUS_E100LX\Eus_100Lx.Ddb	Drawn By:	



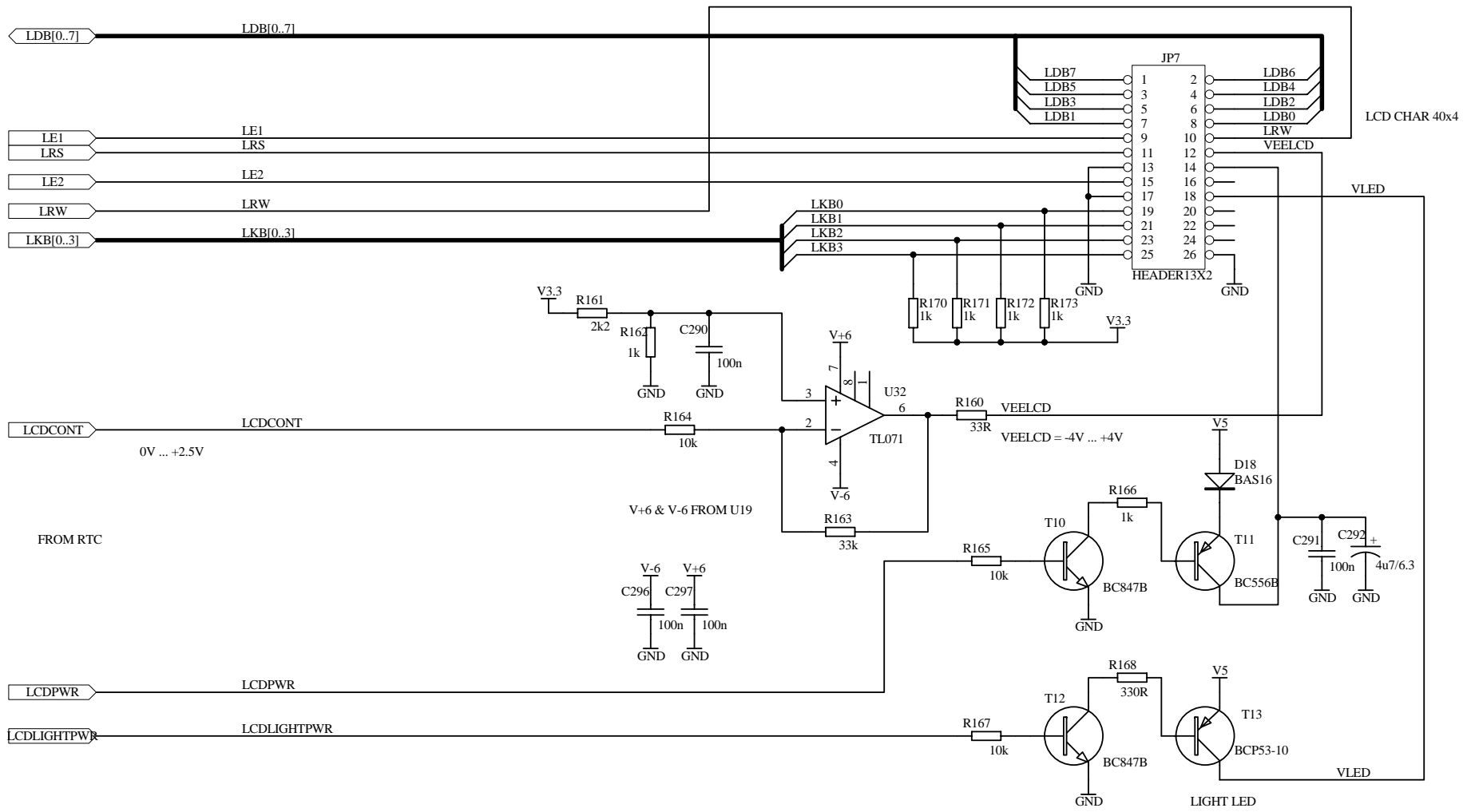
Title		
ETRAX power interface		
Size	Number	Revision
A4	EUS_PWRETR.sch	1.0
Date:	11-May-2005	Sheet of 10
File:	D:\Pcb\EUS\EUS_E100LX\Eus_100lx.Ddb Drawn By:	



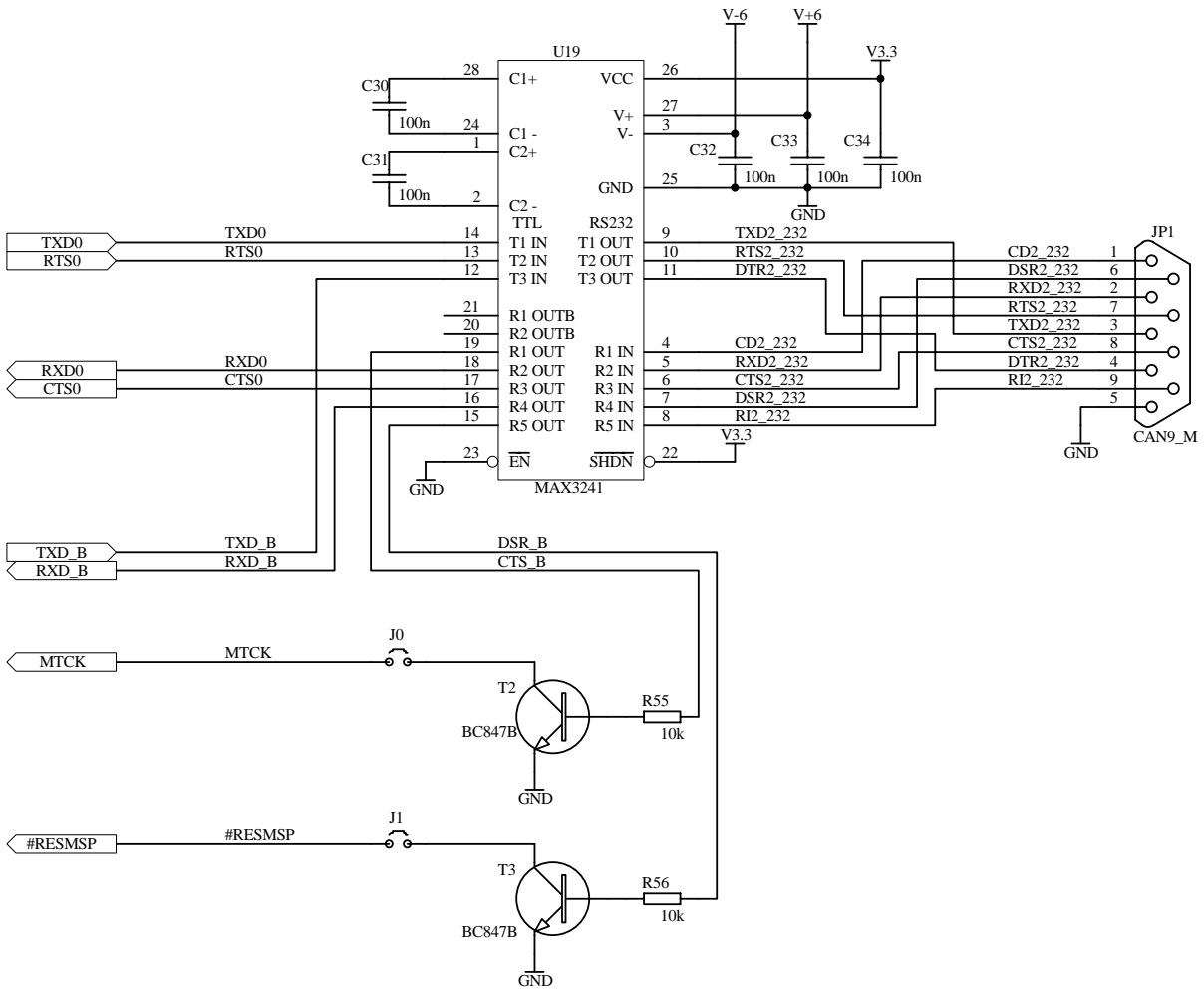
LVDS pairs: Y1-Y2, Y3-Y4, Y5-Y6, Y7-Y8, Y9-Y10,  
 Y11-Y12, Y13-Y14, Y15-Y16, Y17-Y18, Y19-Y20,  
 Y21-Y22, Y23-Y24, Y25-Y26, Y27-Y28



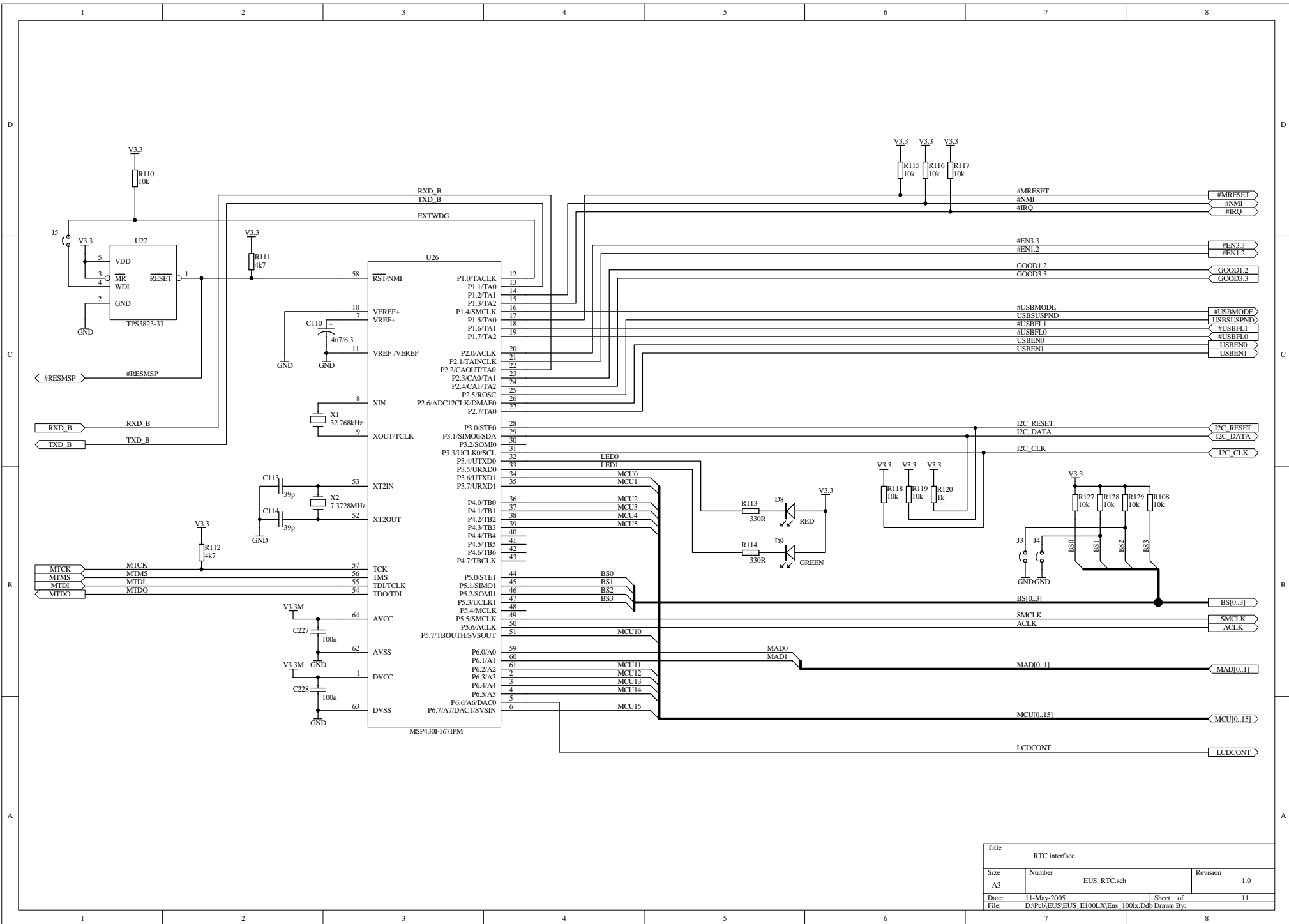
Title			
LCD INTERFACE			
Size	Number	Revision	
A4	EUS_LCD.sch	1.0	
Date:	11-May-2005	Sheet of	20
File:	D:\Pcb\EUS\EUS_E100LX\Eus_100lx.Ddb Drawn By:		



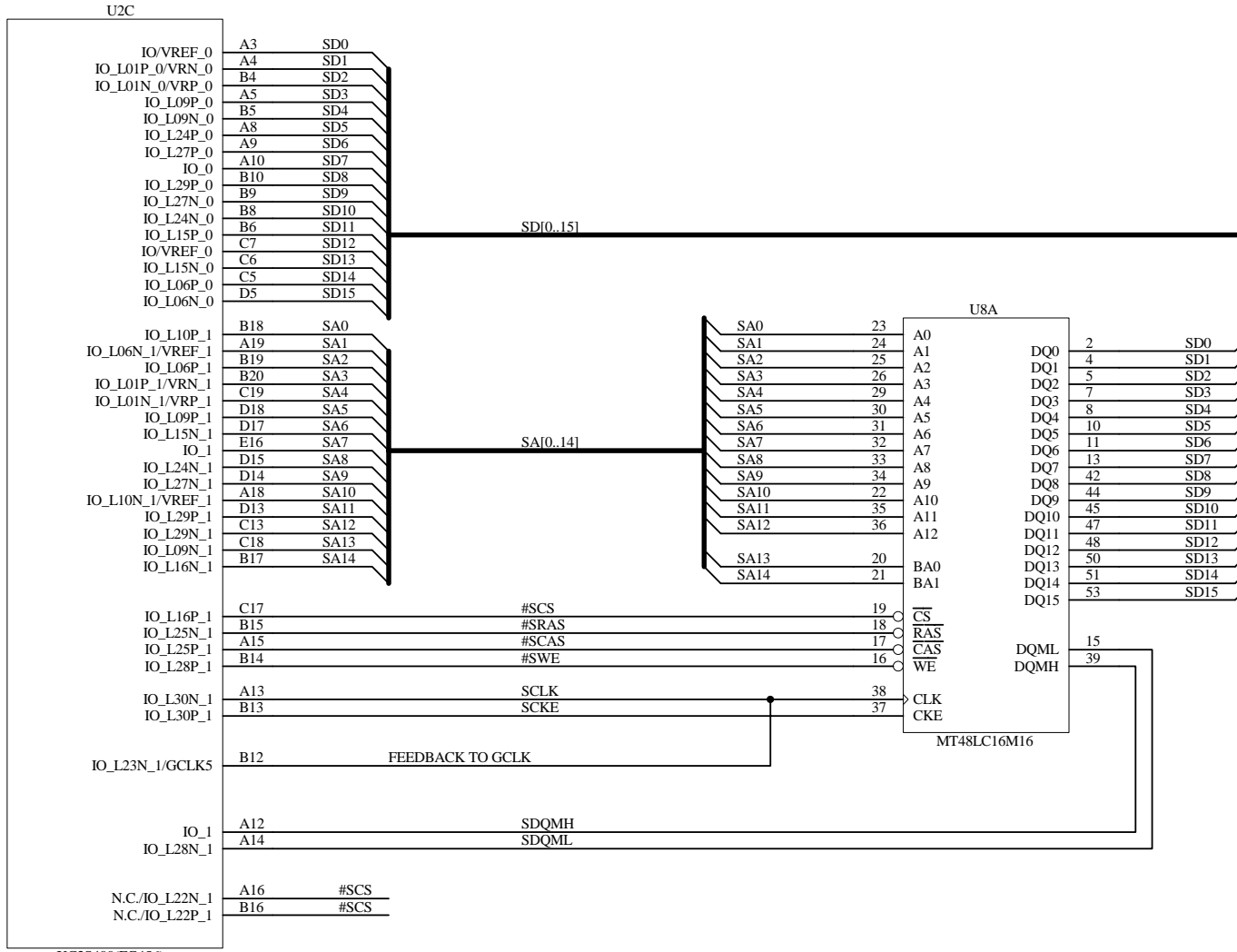
Title			
LCD INTERFACE			
Size	Number	Revision	
A4	EUS_LCD.sch	1.0	
Date:	11-May-2005	Sheet of	14
File:	D:\Pcb\EUS\EUS_E100LX\Eus_100lx.Ddb Drawn By:		



Title			
RS232/RS485 INTERFACE			
Size	Number	Revision	
A4	EUS_RS232.sch	1.0	
Date:	11-May-2005	Sheet of	8
File:	D:\Pcb\EUS\EUS_E100LX\Eus_100lx.Ddb Drawn By:		

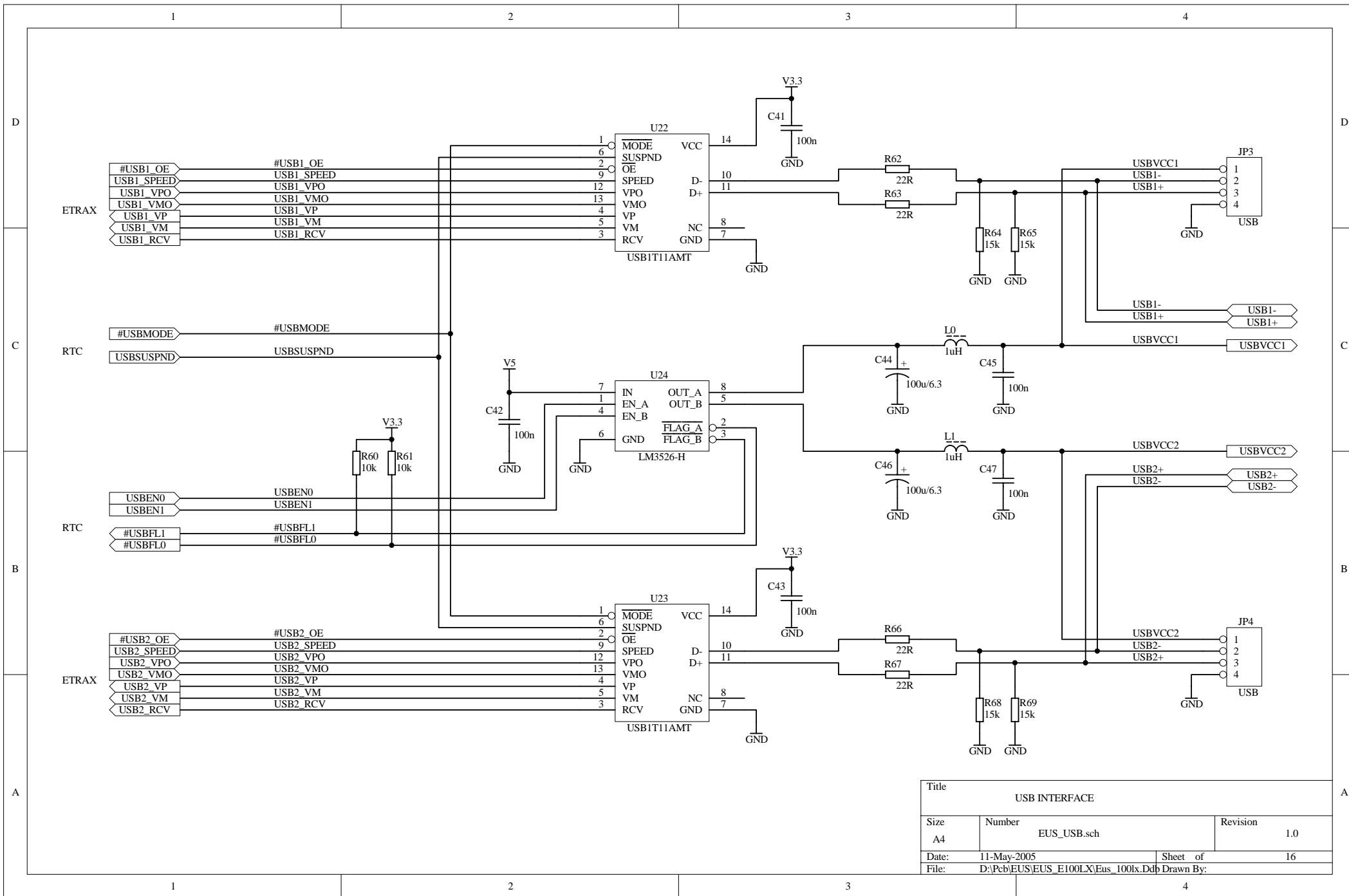


Title			
RTC interface			
Size	Number	Revision	1.0
A3	EUS_RTC.sch		
Date:	11-May-2005	Sheet of	11
File:	D:\Fcb\EUS\EUS_E100LX\Eus_100k.Ddb Drawn By:		

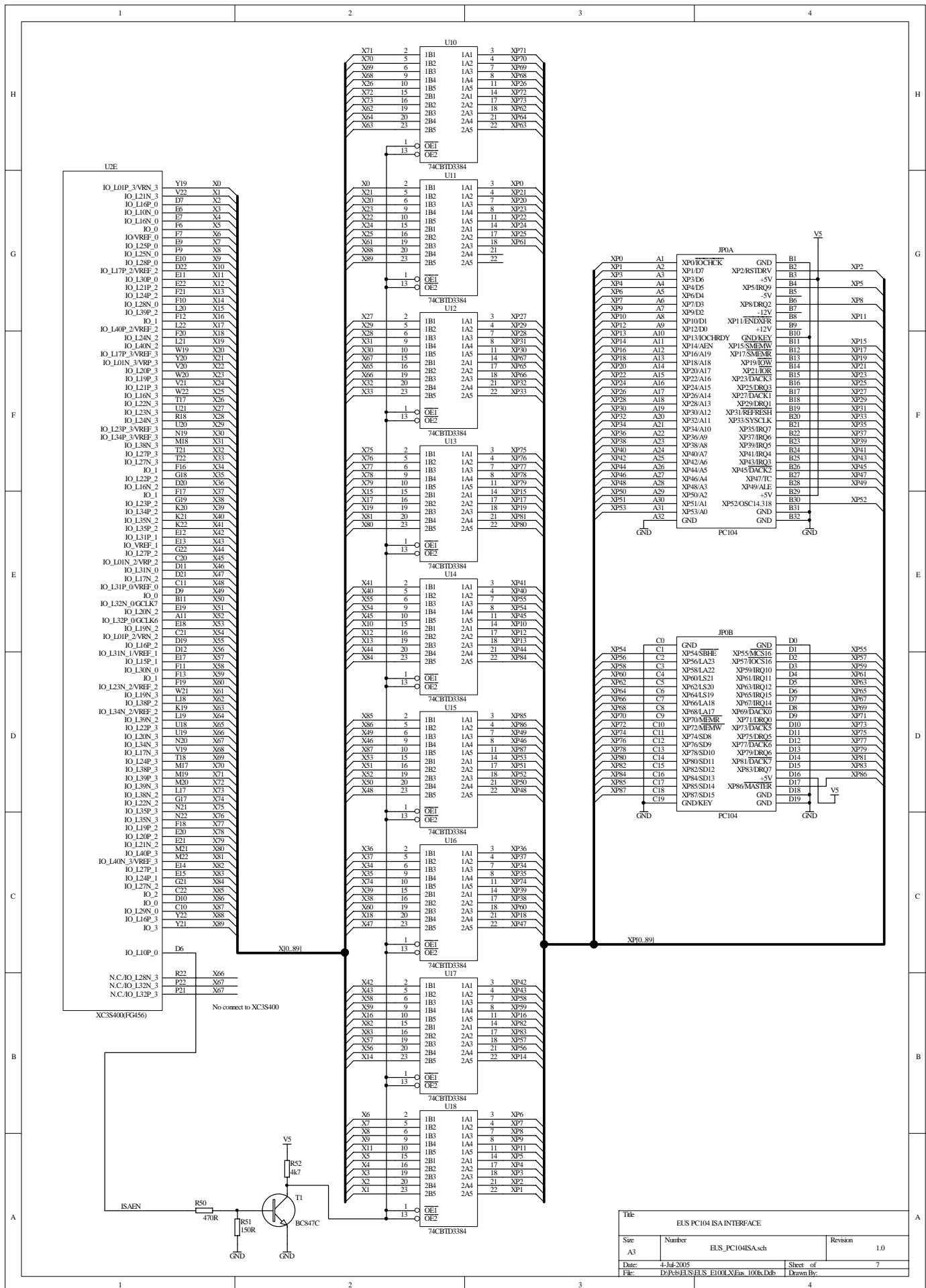


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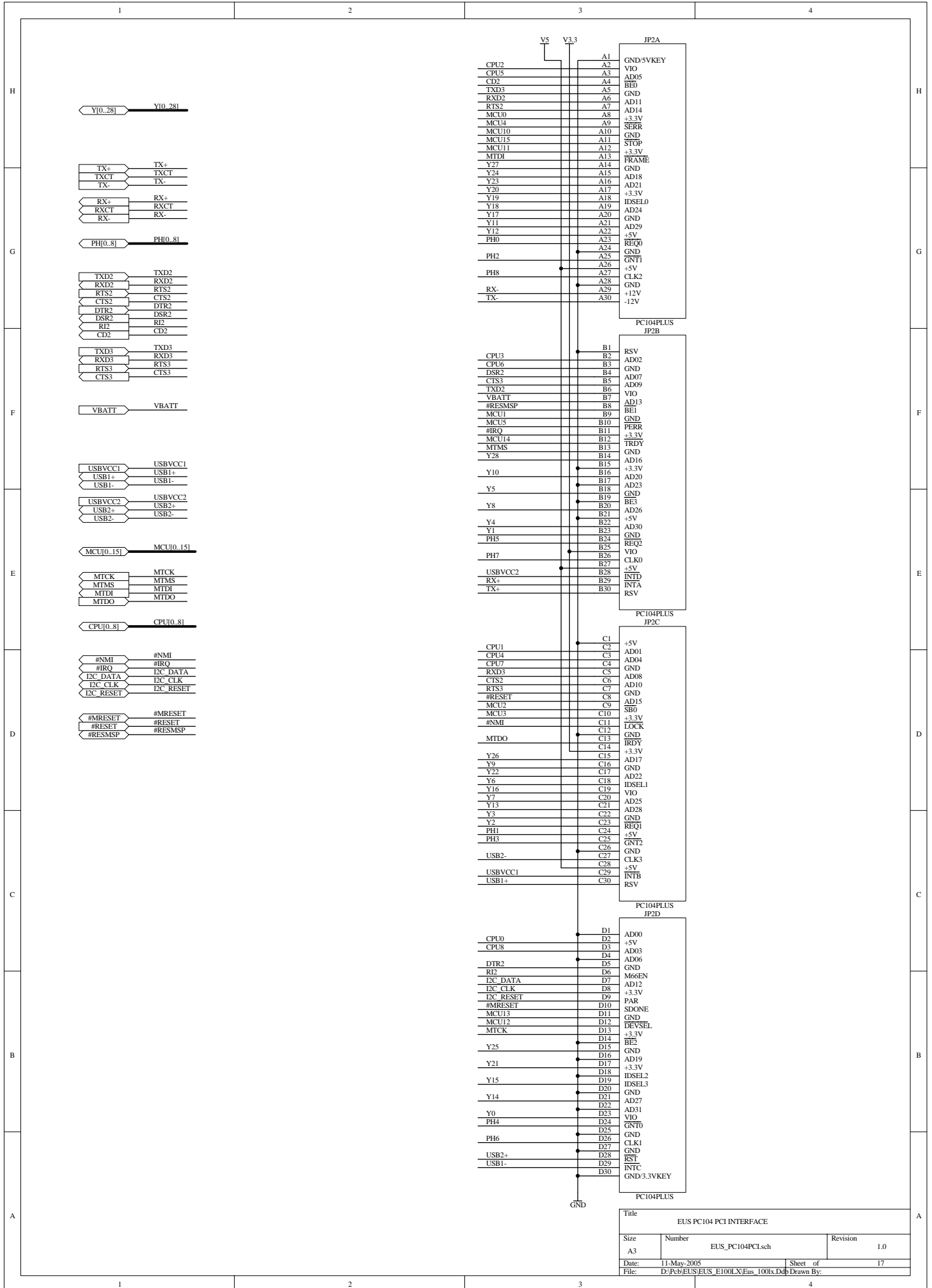
Title			
EUS - SDRAM interface			
Size	Number	Revision	
A4	EUS_SDRAM.sch	1.0	
Date:	11-May-2005	Sheet of	5
File:	D:\Pcb\EUS\EUS_E100LX\Eus_100lx.Ddb Drawn By:		



Title			
USB INTERFACE			
Size	Number	Revision	
A4	EUS_USB.sch	1.0	
Date:	11-May-2005	Sheet of	16
File:	D:\Pcb\EUS\EUS_E100LX\Eus_100Lx.Ddb Drawn By:		

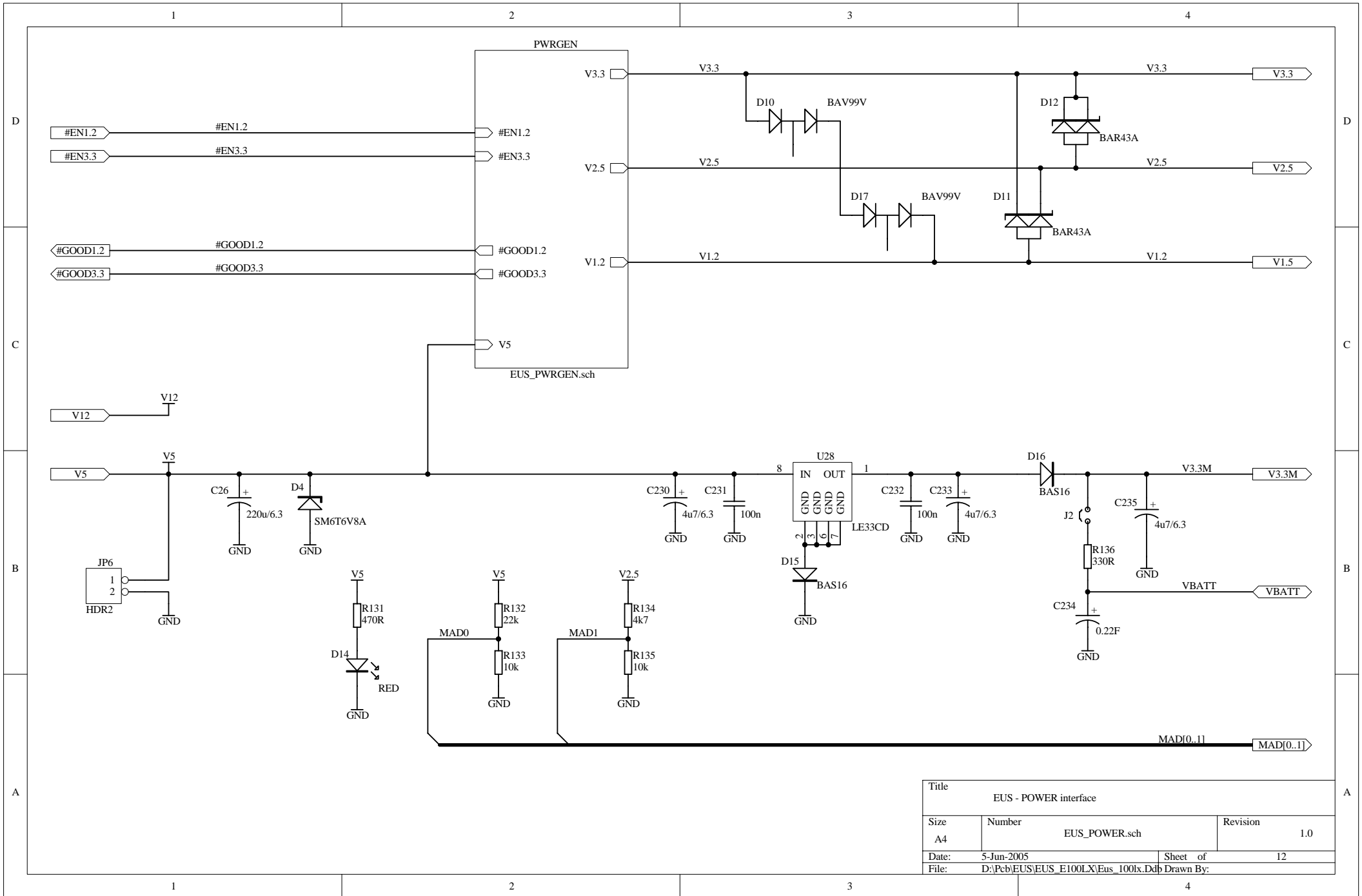


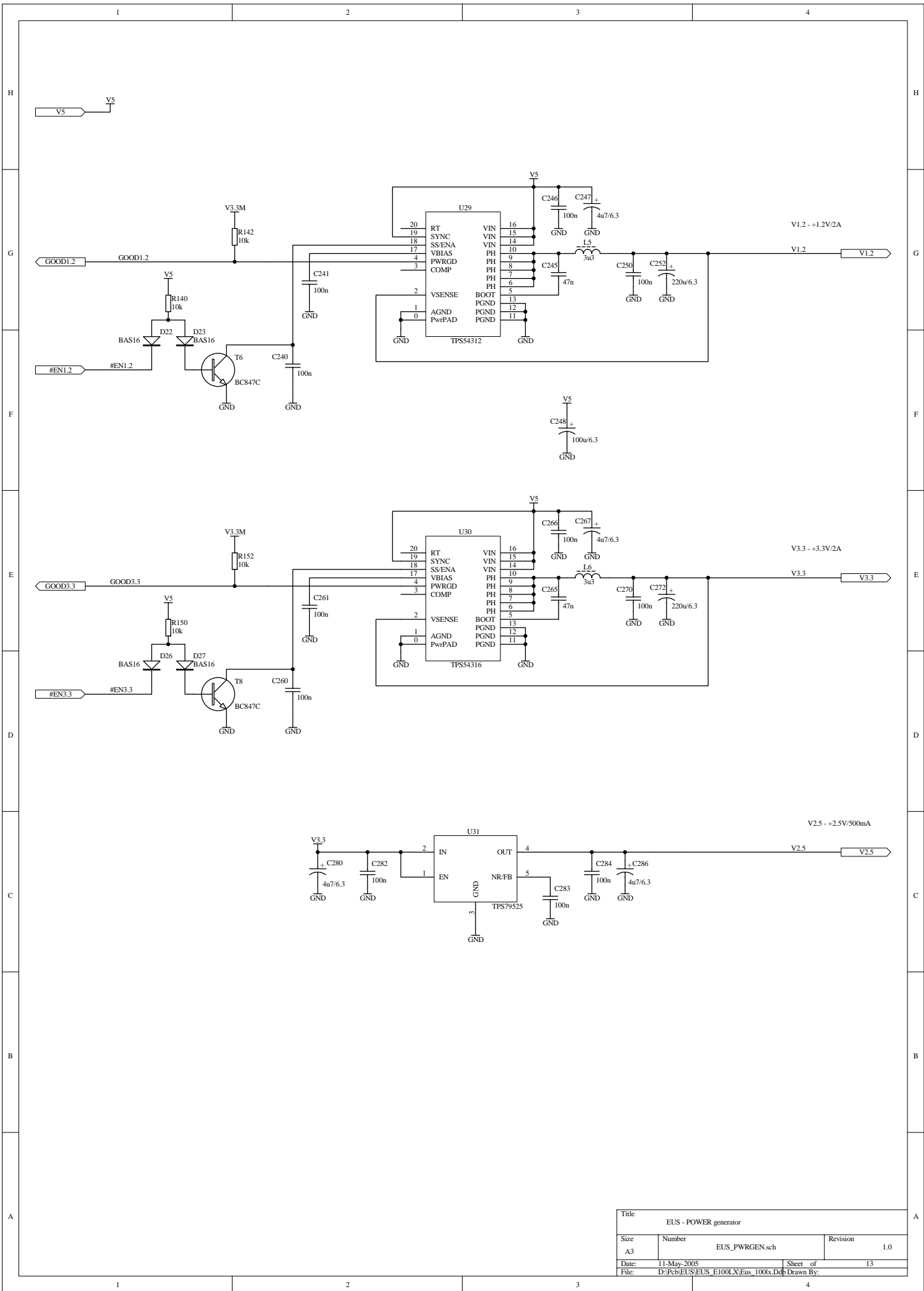
Title			
EUS PC104 ISA INTERFACE			
Size	Number	Revision	1.0
A3	EUS_PC104ISA.sch		
Date	4-Jul-2005	Sheet of	7
File	D:\P3\BUS\BUS_E100LX\Bus_100k.Ddb	Drawn By:	



Title			
EUS PC104 PCI INTERFACE			
Size	Number	Revision	1.0
A3	EUS_PC104PCLsch		
Date:	11-May-2005	Sheet of	17
File:	D:\Pcb\EUS\EUS_E100LX\Eus_100Lx.Ddb Drawn By:		

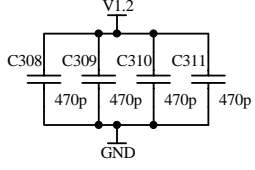
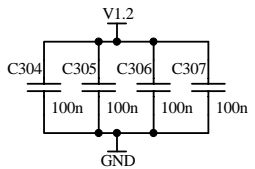
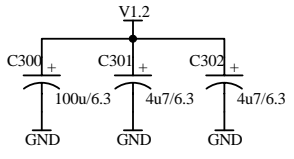




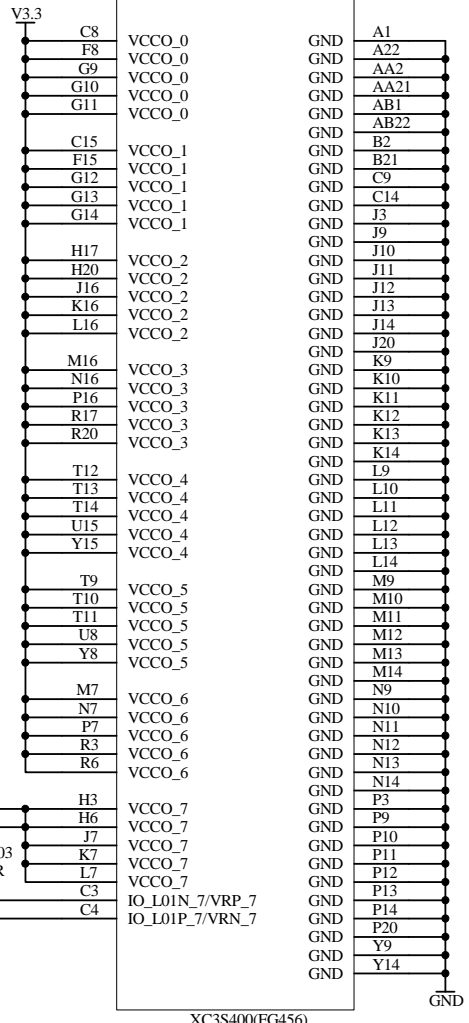
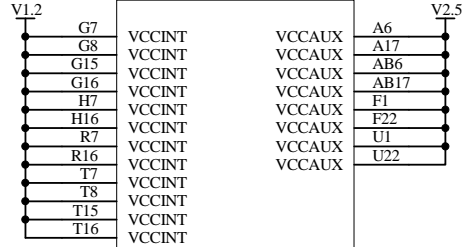
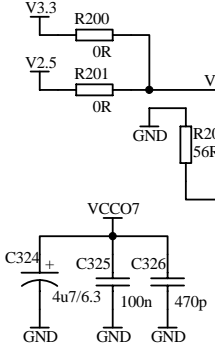
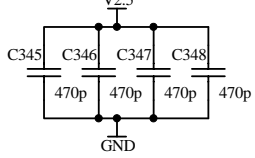
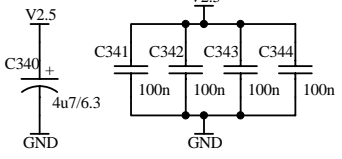
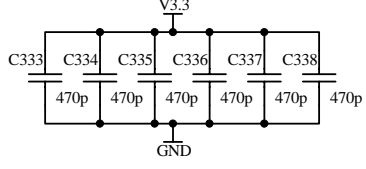
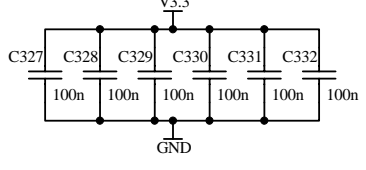
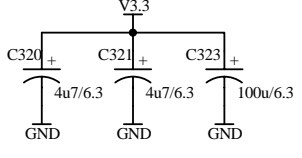


Title			
EUS - POWER generator			
Size	Number	Revision	1.0
A3	EUS_PWRGEN.sch		
Date:	11-May-2005	Sheet of	13
File:	D:\Pcb\EUS\EUS_E100LX\Eus_100Lx.Ddb Drawn By:		

VCC FPGA Internal



VCC FPGA IO



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Title			
FPGA power interface			
Size	Number	Revision	
A4	EUS_PWRFPGA.sch	1.0	
Date:	11-May-2005	Sheet of	15
File:	D:\Pcb\EUS\EUS_E100LX\Eus_100lx.Ddb Drawn By:		