Virtex-5 FPGA Packaging and Pinout Specification

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
04/14/06	1.0	Initial Xilinx release.
05/12/06	1.2	Added UG112 to list of documents. Added units to tables in Chapter 5.
09/05/06	2.0	Added the LXT platform devices throughout document. In Chapter 1, Added a reference to UG112 for package electrical characteristic information in the "Introduction"section. Corrected the description for pin names: CC and GC, removed Note 2, and changed PROGRAM_B_0 to PROGRAM_B (Table 1-7.) In Chapter 2, added Note 1 to each table and added note number to each pin affected by the note content. Added Chapter 6.
10/13/06	2.1	Added system monitor pin information throughout document. Added LX85T devices to appropriate tables. Updated Table 1-3, page 12. Added Note 2 to Table 2-2, Table 2-3, Table 2-4, Table 2-5, Table 2-6, Table 2-8, and Table 2-10.
02/02/07	3.0	Added the SXT devices, added LX220T. Added the "FLOAT" pin and the System Monitor analog inputs to Table 1-7 on page 16. Added RSVD Note 3 to Table 2-2, Table 2-3, Table 2-4, Table 2-5, Table 2-6, Table 2-8, and Table 2-10. Updated No Connect column to add LX110T device in Table 2-8. Replaced all figures in this chapter. Corrected the LX85 data in Table 6-1, page 408, and the LX85T and LX330T in Table 6-2, page 409.
02/08/07	3.0.1	Minor typographical error.
03/21/07	3.1	Added LX220T to Figure 3-22. Fixed MGTTXN and MGTTXP in the legends of Figure 3-5, Figure 3-11, Figure 3-13, Figure 3-21, and Figure 3-25. These legends are now correct and match the pinout tables. Revised all the SelectIO bank diagrams in Chapter 3. Some power pins had been represented as I/O.
08/14/07	3.2	In Table 1-7: ♦ Clarified general purpose I/O descriptions. ♦ Revised the description of RSVD. These pins MUST be tied to ground. ♦ Revised direction of FSn. ♦ Added note 2 to VCCO_#. ♦ Added note 3 to and updated directions for grounding Dedicated System Monitor Pins when not using the System Monitor function. Removed LX30 from the No Connect (NC) column in Table 2-4 for bank 21, pin numbers AC20, AB23, and AE24. Updated the No Connect (NC) column by adding LX110T, LX220T for `MGTAVCC_128` through `MGTAVCC_134` in Table 2-8. Revised the pinout diagrams in Chapter 3 to replace some NC designations with open spaces matching the actual package configuration.

Date	Version	Revision
12/11/07	3.3	Updated the tables in Chapter 1 to include LX20T, LX155, and LX155T devices and the FF323 package. Added center column discussion to description of CC in Table 1-7. Added Table 2-1. Updated Table 2-5 and Table 2-8 to include the LX155T. To avoid confusion, removed some No Connect designations in these tables as well. Updated Table 2-6 and Table 2-10 to include the LX155. Added Figure 3-1 and Figure 3-2. Added LX155 and LX155T to other figures in Chapter 3, "Pinout and SelectIO Bank Diagrams". Updated Figure 3-11 and Figure 3-21. Added Figure 4-1, page 392 to Chapter 4. Updated Table 6-1 to include the LX155, and Table 6-2 to include the LX20T and LX155T as well as the added package FF323.
03/31/08	4.0	Added FXT platform to entire document. To include the GTX serial transceivers, added Table 1-4, page 13 and updated Table 1-6, page 14 and added a note to Table 1-7. Added new devices to Table 2-3, Table 2-5, and Table 2-8. Added Figure 3-24 and Figure 3-25. Updated Figure 4-1 and Figure 4-2 with current JEDEC specification reference. Added new devices to Table 6-2.
04/25/08	4.1	Added XC5VSX240T device to the entire document including Table 1-3, Table 1-6, Table 2-8, Figure 3-25, Figure 3-26, and Table 6-2. Updated ADDRn in Table 1-7. Revised Table 2-8 bank NA, Pin C9 and C15.
05/19/08	4.2	Clarified the direction for Multi-Function Pins, Other Pins, Dedicated System Monitor Pins, and RocketIO Serial Transceiver Pins (GTP_DUAL or GTX_DUAL) in Table 1-7.
06/18/08	4.3	Revised no connect column for MGTAVCC_124 and MGTAVCC_126 in Table 2-5.
09/23/08	4.4	Added TXT platform to entire document.
01/19/09	4.5	Chapter 3: Corrected name of "FF1156 Package—TX150T," page 376. Added Chapter 5, "Recommended PCB Design Rules for BGA Packages". Chapter 6: Added TXT thermal resistance data to Table 6-2, page 409.
05/05/09	4.6	Added Virtex-5Q FPGA package information to Chapter 1, "Packaging Overview," including adding Table 1-5, page 13. Updated legend in Figure 3-11, page 368.
12/11/09	4.7	Changed package availability of XQ5VSX240T and XQ5VFX200T devices from EF1738 to FF1738 in Table 1-5, page 13. Added "EF665 Flip-Chip Fine-Pitch BGA Package Specifications (1.00 mm Pitch)," page 394. Revised dimensions of packages FF665 in Figure 4-4, page 395, FF676 in Figure 4-5, page 396, FF1136 in Figure 4-7, page 398, and FF1153 in Figure 4-8, page 399. Revised package FF1156 in Figure 4-9, page 400 to include the flat lid option. Added EF665, EF676, EF1136, EF1153, and EF1738 to Table 5-1, page 406.

Table of Contents

About This Guide

This guide describes Virtex®-5 FPGA and Virtex-5Q FPGA pinouts and package specifications; it also includes pinout diagrams and thermal data.

Guide Contents

This document is comprised of the following chapters:

- Chapter 1, "Packaging Overview"

  Provides an introduction to the Virtex-5 and Virtex-5Q families with a summary of maximum I/Os available in each device/package combination. Also includes table of pin definitions.
- Chapter 2, "Pinout Tables"

  Provides pinout information for all Virtex-5 and Virtex-5Q devices and packages.
- Chapter 3, "Pinout and SelectIO Bank Diagrams"

  Provides pinout diagrams for all Virtex-5 and Virtex-5Q FPGA package/device combinations.
- Chapter 4, "Mechanical Drawings"

  Provides mechanical drawings of Virtex-5 and Virtex-5Q FPGA packages.
- Chapter 5, "Recommended PCB Design Rules for BGA Packages"

  Provides PCB design rules for BGA packages.
- Chapter 6, "Thermal Specifications"

  Provides thermal data associated with Virtex-5 and Virtex-5Q FPGA packages. Discusses FPGA power management strategy and thermal management options.
- Chapter 7, "Package Marking"

  Provides an example and a description of the marking on top of the package (topmark).

Related Documentation

The following documents are also available for download at http://www.xilinx.com/virtex5.

- Virtex-5 Family Overview or the Virtex-5Q Family Overview
  - The features and product selection of the Virtex-5 family are outlined in this overview.
- Virtex-5 FPGA User Guide

  This guide includes chapters on:
  - Clocking Resources
  - Clock Management Technology (CMT)
  - Phase-Locked Loops (PLLs)
  - Block RAM
  - Configurable Logic Blocks (CLBs)
  - SelectIO™ Resources
  - SelectIO Logic Resources
  - Advanced SelectIO Logic Resources
- Virtex-5 FPGA Data Sheet: DC and Switching Characteristics

  This data sheet contains the DC and Switching Characteristic specifications for the Virtex-5 family.
- Virtex-5 FPGA RocketIO GTP Transceiver User Guide

  This guide describes the RocketIO™ GTP transceivers available in the Virtex-5 LXT and SXT platforms.
- Virtex-5 FPGA RocketIO GTX Transceiver User Guide

  This guide describes the RocketIO GTX transceivers available in the Virtex-5 TXT and FXT platforms.
- Virtex-5 FPGA Embedded Processor Block for Virtex-5 FPGAs

  This reference guide is a description of the embedded processor block available in the Virtex-5 FXT platform.
- Virtex-5 FPGA Embedded Tri-Mode Ethernet MAC User Guide

  This guide describes the dedicated Tri-Mode Ethernet Media Access Controller available in the Virtex-5 LXT, SXT, TXT and FXT platforms.
- Virtex-5 FPGA Integrated Endpoint Block User Guide for PCI Express Designs

  This guide describes the integrated Endpoint blocks in the Virtex-5 LXT, SXT, TXT and FXT platforms used for PCI Express® designs.
- Virtex-5 FPGA XtremeDSP Design Considerations

  This guide describes the XtremeDSP™ slice and includes reference designs for using the DSP48E slice.

- Virtex-5 FPGA Configuration Guide

  This all-encompassing configuration guide includes chapters on configuration interfaces (serial and SelectMAP), bitstream encryption, Boundary-Scan and JTAG configuration, reconfiguration techniques, and readback through the SelectMAP and JTAG interfaces.

- Virtex-5 FPGA System Monitor User Guide

  The System Monitor functionality available in all the Virtex-5 devices is outlined in this guide.

- Virtex-5 FPGA PCB Designer's Guide

  This guide provides information on PCB design for Virtex-5 devices, with a focus on strategies for making design decisions at the PCB and interface level.

Additional Resources

To find additional documentation, see the Xilinx website at:

http://www.xilinx.com/support/documentation/index.htm.

To search the Answer Database of silicon, software, and IP questions and answers, or to create a technical support WebCase, see the Xilinx website at:

http://www.xilinx.com/support/mysupport.htm.

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Chapter 1

Packaging Overview

Summary

This chapter covers the following topics:

- Introduction
- Device/Package Combinations and Maximum I/Os
- Pin Definitions

Introduction

This section describes the pinouts for Virtex®-5 devices in the 1.00 mm pitch flip-chip fine-pitch BGA packages.

Virtex-5 devices are offered exclusively in high performance flip-chip BGA packages that are optimally designed for improved signal integrity and jitter. Package inductance is minimized as a result of optimal placement and even distribution as well as an increased number of Power and GND pins.

All of the devices supported in a particular package are pinout compatible and are listed in the same table (one table per package). Pins that are not available for the smaller devices are listed in the "No Connects" column of each table.

For Virtex-5Q devices, the EF package is offered. The only difference between an EF and an FF package is that the discrete substrate capacitors on the EF package are coated with epoxy. The coating is comprised of an undercoat epoxy that is dispensed under the capacitors and an overcoat epoxy that is dispensed over the top of the capacitors. All other package construction characteristics of the EF matches that of the FF package. The EF package changes are noted in Chapter 4, "Mechanical Drawings."

Each device is split into eight or more I/O banks to allow for flexibility in the choice of I/O standards (see UG190: *Virtex-5 FPGA User Guide*). Global pins, including JTAG, configuration, and power/ground pins, are listed at the end of each table. Table 1-7 provides definitions for all pin types.

For information on package electrical characteristics and how the characteristics are measured, refer to UG112: *Device Package User Guide* found on the Xilinx website.

For the latest Virtex-5 FPGA pinout information, check the Xilinx website for any updates to this document.

Device/Package Combinations and Maximum I/Os

Table 1-1 shows the maximum number of user I/Os possible in Virtex-5 FPGA flip-chip packages. FF denotes flip-chip fine-pitch BGA (1.00 mm pitch).

Table 1-1: **Flip-Chip Packages**

Package Specifications	Packages									
	FF323	FF324	FF665	FF676	FF1136	FF1153	FF1156	FF1738	FF1759	FF1760
Pitch (mm)	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00
Size (mm)	19 x 19	19 x 19	27 x 27	27 x 27	35 x 35	35 x 35	35 x 35	42.5 x 42.5	42.5 x 42.5	42.5 x 42.5
Maximum I/Os	172	220	360	440	640	800	360	960	680	1200

The number of I/Os per package includes all user I/Os *except* the 19 pins listed in Table 1-2.

Table 1-2: **Virtex-5 FPGA I/O Pins in the Dedicated Configuration Bank (Bank0)**

DXP	HSWAPEN	INIT_B_0	M0_0	TDI
DXN	D_IN	CS_B_0	M1_0	D_OUT_BUSY
VBATT	DONE	RDWR_B_0	M2_0	TDO_0
PROGRAM_B	CCLK_0	TCK_0	TMS	

The RocketIO™ GTP transceiver I/O channels for the devices listed in Table 1-3 or the GTX transceiver I/O channels for the devices listed in Table 1-4.

Table 1-3: **Number of GTP Transceiver I/O Channels/Device**

I/O Channels	Device											
	LX20T	LX30T(1)	SX35T	LX50T(2)	SX50T(3)	LX85T	SX95T	LX110T	LX155T	LX220T	SX240T	LX330T
MGTRXP	4	4 or 8	8	8 or 12	8 or 12	12	16	16	16	16	24	24
MGTRXN	4	4 or 8	8	8 or 12	8 or 12	12	16	16	16	16	24	24
MGTTXP	4	4 or 8	8	8 or 12	8 or 12	12	16	16	16	16	24	24
MGTTXN	4	4 or 8	8	8 or 12	8 or 12	12	16	16	16	16	24	24

Notes:

1. The XC5VLX30T has 4 GTP I/O channels in the FF323/FFG323 package and 8 GTP I/O channels in the FF665/FFG665 package.
2. The XC5VLX50T has 8 GTP I/O channels in the FF665/FFG665 package and 12 GTP I/O channels in the FF1136/FFG1136 package.
3. The XC5VSX50T has 8 GTP I/O channels in the FF665/FFG665 package and 12 GTP I/O channels in the FF1136/FFG1136 package.

Table 1-4: **Number of GTX Transceiver I/O Channels/Device**

I/O Channels	Device						
	FX30T	FX70T(1)	FX100T	FX130T	TX150T	FX200T	TX240T
MGTRXP	8	8 or 16	16	20	40	24	48
MGTRXN	8	8 or 16	16	20	40	24	48
MGTTXP	8	8 or 16	16	20	40	24	48
MGTTXN	8	8 or 16	16	20	40	24	48

Notes:

1. The XC5VFX70T has 8 GTX I/O channels in the FF665/FFG665 package and 16 GTX I/O channels in the FF1136/FFG1136 package.

Table 1-5 shows the available EF and FF packages for the Virtex-5Q devices.

Table 1-5: **Available Virtex-5Q Devices with EF and FF Package Types**

Virtex-5Q Device	FF323	EF665	EF676	EF1136	EF1153	EF1738	FF1738
XQ5VLX85			Available				
XQ5VLX110			Available		Available		
XQ5VLX30T(1)	Available						
XQ5VLX110T				Available			
XQ5VLX155T				Available			
XQ5VLX220T						Available	
XQ5VLX330T						Available	
XQ5VSX50T		Available					
XQ5VSX95T				Available			
XQ5VSX240T(2)							Available
XQ5VFX70T		Available		Available			
XQ5VFX100T				Available		Available	
XQ5VFX130T						Available	
XQ5VFX200T(2)							Available

Notes:

1. The XQ5VLX30T is only available in the standard FF323 package and not an epoxy coated capacitor EF version.
2. The XQ5VSX240T and XQ5VFX200T are only available in the FF1738 package.

Table 1-6 shows the number of available I/Os and the number of differential I/O pairs for each Virtex-5 device/package combination.

Table 1-6: **Available I/O Pin/Device/Package Combinations**

Virtex-5 Device	User I/Os Pins	Virtex-5 FPGA Package									
		FF323	FF324	FF665	FF676	FF1136	FF1153	FF1156	FF1738	FF1759	FF1760
XC5VLX20T	Available User I/Os	172	–	–	–	–	–	–	–	–	–
	Differential I/O Pairs	86	–	–	–	–	–	–	–	–	–
XC5VLX30	Available User I/Os	–	220	–	400	–	–	–	–	–	–
	Differential I/O Pairs	–	110	–	200	–	–	–	–	–	–
XC5VLX30T	Available User I/Os	172	–	360	–	–	–	–	–	–	–
	Differential I/O Pairs	86	–	180	–	–	–	–	–	–	–
XC5VFX30T	Available User I/Os	–	–	360	–	–	–	–	–	–	–
	Differential I/O Pairs	–	–	180	–	–	–	–	–	–	–
XC5VSX35T	Available User I/Os	–	–	360	–	–	–	–	–	–	–
	Differential I/O Pairs	–	–	180	–	–	–	–	–	–	–
XC5VLX50	Available User I/Os	–	220	–	440	–	560	–	–	–	–
	Differential I/O Pairs	–	110	–	220	–	280	–	–	–	–
XC5VLX50T	Available User I/Os	–	–	360	–	480	–	–	–	–	–
	Differential I/O Pairs	–	–	180	–	240	–	–	–	–	–
XC5VSX50T	Available User I/Os	–	–	360	–	480	–	–	–	–	–
	Differential I/O Pairs	–	–	180	–	240	–	–	–	–	–
XC5VFX70T	Available User I/Os	–	–	360	–	640	–	–	–	–	–
	Differential I/O Pairs	–	–	180	–	320	–	–	–	–	–
XC5VLX85	Available User I/Os	–	–	–	440	–	560	–	–	–	–
	Differential I/O Pairs	–	–	–	220	–	280	–	–	–	–
XC5VLX85T	Available User I/Os	–	–	–	–	480	–	–	–	–	–
	Differential I/O Pairs	–	–	–	–	240	–	–	–	–	–
XC5VSX95T	Available User I/Os	–	–	–	–	640	–	–	–	–	–
	Differential I/O Pairs	–	–	–	–	320	–	–	–	–	–
XC5VFX100T	Available User I/Os	–	–	–	–	640	–	–	680	–	–
	Differential I/O Pairs	–	–	–	–	320	–	–	340	–	–
XC5VLX110	Available User I/Os	–	–	–	440	–	800	–	–	–	800
	Differential I/O Pairs	–	–	–	220	–	400	–	–	–	400
XC5VLX155	Available User I/Os	–	–	–	–	–	800	–	–	–	800
	Differential I/O Pairs	–	–	–	–	–	400	–	–	–	400
XC5VLX110T	Available User I/Os	–	–	–	–	640	–	–	680	–	–
	Differential I/O Pairs	–	–	–	–	320	–	–	340	–	–

Table 1-6: **Available I/O Pin/Device/Package Combinations *(Continued)***

Virtex-5 Device	User I/Os Pins	Virtex-5 FPGA Package									
		FF323	FF324	FF665	FF676	FF1136	FF1153	FF1156	FF1738	FF1759	FF1760
XC5VFX130T	Available User I/Os	–	–	–	–	–	–	–	840	–	–
	Differential I/O Pairs	–	–	–	–	–	–	–	420	–	–
XC5VTX150T	Available User I/Os	–	–	–	–	–	–	360	–	680	–
	Differential I/O Pairs	–	–	–	–	–	–	180	–	340	–
XC5VLX155T	Available User I/Os	–	–	–	–	640	–	–	680	–	–
	Differential I/O Pairs	–	–	–	–	320	–	–	340	–	–
XC5VFX200T	Available User I/Os	–	–	–	–	–	–	–	960	–	–
	Differential I/O Pairs	–	–	–	–	–	–	–	480	–	–
XC5VLX220	Available User I/Os	–	–	–	–	–	–	–	–	–	800
	Differential I/O Pairs	–	–	–	–	–	–	–	–	–	400
XC5VLX220T	Available User I/Os	–	–	–	–	–	–	–	680	–	–
	Differential I/O Pairs	–	–	–	–	–	–	–	340	–	–
XC5VSX240T	Available User I/Os	–	–	–	–	–	–	–	960	–	–
	Differential I/O Pairs	–	–	–	–	–	–	–	480	–	–
XC5VTX240T	Available User I/Os	–	–	–	–	–	–	–	–	680	–
	Differential I/O Pairs	–	–	–	–	–	–	–	–	340	–
XC5VLX330	Available User I/Os	–	–	–	–	–	–	–	–	–	1200
	Differential I/O Pairs	–	–	–	–	–	–	–	–	–	600
XC5VLX330T	Available User I/Os	–	–	–	–	–	–	–	960	–	–
	Differential I/O Pairs	–	–	–	–	–	–	–	480	–	–

Pin Definitions

Table 1-7 lists the pin definitions used in Virtex-5 FPGA packages.

Table 1-7: **Virtex-5 FPGA Pin Definitions**

Pin Name	Direction	Description
User I/O Pins		
IO_LXXY_#	Input/ Output	All user I/O pins are capable of differential signaling and can implement pairs. Each user I/O is labeled "**IO_LXXY_#**", where: **IO** indicates a user I/O pin. **LXXY** indicates a differential pair, with **XX** a unique pair in the bank and **Y = [P|N]** for the positive/negative sides of the differential pair.
Multi-Function Pins		
IO_LXXY_ZZZ_#		Multi-function pins are labelled "**IO_LXXY_ZZZ_#**", where **ZZZ** represents one or more of the following functions in addition to being general purpose user I/O. If not used for their special function, these pins can be user I/O.
Dn	Input	In SelectMAP mode, D0 through D31 are configuration data pins. These pins become user I/Os after configuration, unless the SelectMAP port is retained.
ADDRn	Output	ADDR0–ADDR25 BPI address output. These pins become user I/O after configuration.
RSn	Output	RS0 and RS1 revision select output.
FCS_B	Output	BPI and SPI flash chip select.
FOE_B	Output	BPI flash output enable.
FWE_B	Output	BPI flash write enable.
MOSI	Output	SPI flash data output enable.
CSO_B	Output	Parallel daisy chain chip select.
FSn	Input	FS0–FS2 SPI Flash vendor selection.
CC	Input	These clock pins connect to Clock Capable I/Os. These pins become regular user I/Os when not needed for clocks. If a single-ended clock is connected to the differential CC pair of pins, it must be connected to the positive (P) side of the pair. Clock capable I/Os in the center column can not drive BUFRs.
GC	Input	These clock pins connect to Global Clock Buffers. These pins become regular user I/Os when not needed for clocks. If a single-ended clock is connected to the differential GC pair of pins, it must be connected to the positive (P) side of the pair.
SMnP/SMnN	Input	System Monitor analog inputs.
VREF	N/A	These are input threshold voltage pins. They become user I/Os when an external threshold voltage is not needed (per bank).
VRN	N/A	This pin is for the DCI voltage reference resistor of N transistor (per bank, to be pulled High with reference resistor).
VRP	N/A	This pin is for the DCI voltage reference resistor of P transistor (per bank, to be pulled Low with reference resistor).

Table 1-7: **Virtex-5 FPGA Pin Definitions *(Continued)***

Pin Name	Direction	Description
Dedicated Configuration Pins[1]		
CCLK_0	Input/ Output	Configuration clock. Output and input in Master mode or Input in Slave mode.
CS_B_0	Input	In SelectMAP mode, this is the active-low Chip Select signal.
D_IN_0	Input	In bit-serial modes, D_IN is the single-data input.
DONE_0	Input/ Output	DONE is a bidirectional signal with an optional internal pull-up resistor. As an output, this pin indicates completion of the configuration process. As an input, a Low level on DONE can be configured to delay the start-up sequence.
D_OUT_BUSY_0	Output	In SelectMAP mode, BUSY controls the rate at which configuration data is loaded. In bit-serial modes, DOUT gives preamble and configuration data to down-stream devices in a daisy chain.
HSWAPEN_0	Input	Enable I/O pullups during configuration
INIT_B_0	Bidirectional (open-drain)	When Low, this pin indicates that the configuration memory is being cleared. When held Low, the start of configuration is delayed. During configuration, a Low on this output indicates that a configuration data error has occurred.
M0_0, M1_0, M2_0	Input	Configuration mode selection
PROGRAM_B	Input	Active Low asynchronous reset to configuration logic. This pin has a permanent weak pull-up resistor.
RDWR_B_0	Input	In SelectMAP mode, this is the active-low Write Enable signal.
TCK_0	Input	Boundary-Scan Clock.
TDI_0	Input	Boundary-Scan Data Input.
TDO_0	Output	Boundary-Scan Data Output.
TMS_0	Input	Boundary-Scan Mode Select.
DXP_0, DXN_0	N/A	Temperature-sensing diode pins (Anode: DXP; Cathode: DXN).
Reserved Pins		
RSVD	N/A	Reserved pins—must be tied to ground.
FLOAT	N/A	Do not connect this pin to the board. Leave floating.
Other Pins		
GND	N/A	Ground.
VBATT_0	N/A	Decryptor key memory backup supply; this pin should be tied to V_{CC} or GND.
VCCAUX	N/A	Power-supply pins for auxiliary circuits.
VCCINT	N/A	Power-supply pins for the internal core logic.
VCCO_#[2]	N/A	Power-supply pins for the output drivers (per bank).

Table 1-7: **Virtex-5 FPGA Pin Definitions *(Continued)***

Pin Name	Direction	Description
Dedicated System Monitor Pins		
AVDD_0(3)	N/A	System Monitor's ADC analog positive supply voltage.
AVSS_0(3)	N/A	System Monitor's ADC analog ground reference.
VP_0(3)	Input	System Monitor dedicated differential analog input (positive side).
VN_0(3)	Input	System Monitor dedicated differential analog input (negative side).
VREFP_0(3)	N/A	External System Monitor 2.5V positive reference voltage.
VREFN_ 0(3)	N/A	External System Monitor 2.5V ground reference voltage.
RocketIO Serial Transceiver Pins (GTP_DUAL or GTX_DUAL)		
MGTAVCC	N/A	Power-supply pin for transceiver mixed-signal circuitry.
MGTAVCCPLL	N/A	Power-supply pin for PLL.(4)
MGTAVTTRX	N/A	Power-supply pin for RX circuitry.
MGTAVTTRXC	N/A	Power-supply pin for the resistor calibration circuit.
MGTAVTTTX	N/A	Power-supply pin for TX circuitry.
MGTREFCLKP	Input	Positive differential reference clock.
MGTREFCLKN	Input	Negative differential reference clock (negative).
MGTRREF	Input	Precision reference resistor pin for internal calibration termination.
MGTRXP	Input	Positive differential receive port.
MGTRXN	Input	Negative differential receive port.
MGTTXP	Output	Positive differential transmit port.
MGTTXN	Output	Negative differential transmit port.

Notes:

1. All dedicated pins (JTAG and configuration) are powered by V_{CC_CONFIG}.
2. V_{CCO} pins in unbonded banks must be connected to the V_{CCO} for that bank for package migration. Do NOT connect unbonded V_{CCO} pins to different supplies. Without a package migration requirement, V_{CCO} pins in unbonded banks can be left unconnected or tied to a common supply (V_{CCO} or ground).
3. When not using System Monitor, these pins must be grounded. See "Disabling the System Monitor" in UG192: *Virtex-5 FPGA System Monitor User Guide*.
4. MGTAVCCPLL voltage for GTP transceivers is not the same as the MGTAVCCPLL voltage for GTX transceivers, see DS202: *Virtex-5 FPGA Data Sheet*. UG196: *Virtex-5 FPGA RocketIO GTP Transceiver User Guide* and UG198: *Virtex-5 FPGA RocketIO GTX Transceiver User Guide* contain board design guidelines for these transceivers.

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Chapter 2

Pinout Tables

Summary

This chapter includes the pinout information tables for the following packages:

FF323 Package—LX20T and LX30T

Table 2-1: **FF323 Package—LX20T and LX30T**

Bank	Pin Description	Pin Number	No Connect (NC)
0	DXP_0	K10	
0	DXN_0	K9	
0	AVDD_0	G10	
0	AVSS_0	G9	
0	VP_0	H10	
0	VN_0	J9	
0	VREFP_0	J10	
0	VREFN_0	H9	
0	VBATT_0	D5	
0	PROGRAM_B_0	E11	

Table 2-1: **FF323 Package—LX20T and LX30T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
0	HSWAPEN_0	F11	
0	D_IN_0	F6	
0	DONE_0	F9	
0	CCLK_0	E10	
0	INIT_B_0	B5	
0	CS_B_0	A4	
0	RDWR_B_0	E6	
0	RSVD(3)	L9	
0	RSVD(3)	L10	
0	TCK_0	M6	
0	M0_0	G6	
0	M2_0	M9	
0	M1_0	H5	
0	TMS_0	N1	
0	TDI_0	M5	
0	D_OUT_BUSY_0	N3	
0	TDO_0	N5	
1	IO_L0P_A19_1	A7	
1	IO_L0N_A18_1	A6	
1	IO_L1P_A17_1	E9	
1	IO_L1N_A16_1	D8	
1	IO_L2P_A15_D31_1	D10	
1	IO_L2N_A14_D30_1	D9	
1	IO_L3P_A13_D29_1	C8	
1	IO_L3N_A12_D28_1	C7	
1	IO_L4P_A11_D27_1	B9	
1	IO_L4N_VREF_A10_D26_1	B8	
1	IO_L5P_A9_D25_1	B6	
1	IO_L5N_A8_D24_1	C6	
1	IO_L6P_A7_D23_1	A8	
1	IO_L6N_A6_D22_1	A9	
1	IO_L7P_A5_D21_1	D7	
1	IO_L7N_A4_D20_1	E7	

Table 2-1: **FF323 Package—LX20T and LX30T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
1	IO_L8P_CC_A3_D19_1	B10	
1	IO_L8N_CC_A2_D18_1 (2)	C10	
1	IO_L9P_CC_A1_D17_1	F8	
1	IO_L9N_CC_A0_D16_1 (2)	F7	
2	IO_L0P_CC_RS1_2	R1	
2	IO_L0N_CC_RS0_2 (2)	T1	
2	IO_L1P_CC_A25_2	V1	
2	IO_L1N_CC_A24_2 (2)	U1	
2	IO_L2P_A23_2	P2	
2	IO_L2N_A22_2	P3	
2	IO_L3P_A21_2	V2	
2	IO_L3N_A20_2	V3	
2	IO_L4P_FCS_B_2	R2	
2	IO_L4N_VREF_FOE_B_MOSI_2	T2	
2	IO_L5P_FWE_B_2	U4	
2	IO_L5N_CSO_B_2	U3	
2	IO_L6P_D7_2	P4	
2	IO_L6N_D6_2	R4	
2	IO_L7P_D5_2	U5	
2	IO_L7N_D4_2	V5	
2	IO_L8P_D3_2	P5	
2	IO_L8N_D2_FS2_2	R5	
2	IO_L9P_D1_FS1_2	T4	
2	IO_L9N_D0_FS0_2	T3	
4	IO_L0P_GC_D15_4	R9	
4	IO_L0N_GC_D14_4 (1)	P9	
4	IO_L1P_GC_D13_4	N7	
4	IO_L1N_GC_D12_4 (1)	N6	
4	IO_L2P_GC_D11_4	T9	
4	IO_L2N_GC_D10_4 (1)	U9	
4	IO_L3P_GC_D9_4	T6	
4	IO_L3N_GC_D8_4 (1)	R6	
4	IO_L4P_GC_4	T8	

Table 2-1: **FF323 Package—LX20T and LX30T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
4	IO_L4N_GC_VREF_4 (1)	U8	
4	IO_L5P_GC_4	V6	
4	IO_L5N_GC_4 (1)	U6	
4	IO_L6P_GC_4	V8	
4	IO_L6N_GC_4 (1)	V7	
4	IO_L7P_GC_VRN_4	N8	
4	IO_L7N_GC_VRP_4 (1)	M8	
4	IO_L8P_CC_GC_4	T7	
4	IO_L8N_CC_GC_4 (1)(2)	R7	
4	IO_L9P_CC_GC_4	P8	
4	IO_L9N_CC_GC_4 (1)(2)	P7	
11	IO_L0P_11	D13	
11	IO_L0N_11	D14	
11	IO_L1P_11	E15	
11	IO_L1N_11	D15	
11	IO_L2P_11	E14	
11	IO_L2N_11	F14	
11	IO_L3P_11	A11	
11	IO_L3N_11	A12	
11	IO_L4P_11	C12	
11	IO_L4N_VREF_11	C13	
11	IO_L5P_11	B13	
11	IO_L5N_11	A13	
11	IO_L6P_11	G14	
11	IO_L6N_11	G15	
11	IO_L7P_11	B14	
11	IO_L7N_11	A14	
11	IO_L8P_CC_11	G13	
11	IO_L8N_CC_11 (2)	F13	
11	IO_L9P_CC_11	C15	
11	IO_L9N_CC_11 (2)	B15	
11	IO_L10P_CC_SM15P_11	B16	
11	IO_L10N_CC_SM15N_11 (2)	A16	

Table 2-1: **FF323 Package—LX20T and LX30T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
11	IO_L11P_CC_SM14P_11	F16	
11	IO_L11N_CC_SM14N_11 (2)	G16	
11	IO_L12P_VRN_11	A18	
11	IO_L12N_VRP_11	A17	
11	IO_L13P_11	E17	
11	IO_L13N_11	E16	
11	IO_L14P_11	C17	
11	IO_L14N_VREF_11	C16	
11	IO_L15P_SM13P_11	D12	
11	IO_L15N_SM13N_11	E12	
11	IO_L16P_SM12P_11	C18	
11	IO_L16N_SM12N_11	B18	
11	IO_L17P_SM11P_11	F18	
11	IO_L17N_SM11N_11	F17	
11	IO_L18P_SM10P_11	D18	
11	IO_L18N_SM10N_11	D17	
11	IO_L19P_SM9P_11	B11	
11	IO_L19N_SM9N_11	C11	
13	IO_L0P_SM8P_13	H13	
13	IO_L0N_SM8N_13	J14	
13	IO_L1P_SM7P_13	H17	
13	IO_L1N_SM7N_13	G18	
13	IO_L2P_SM6P_13	J15	
13	IO_L2N_SM6N_13	K15	
13	IO_L3P_SM5P_13	H18	
13	IO_L3N_SM5N_13	J18	
13	IO_L4P_13	K12	
13	IO_L4N_VREF_13	L12	
13	IO_L5P_SM4P_13	J17	
13	IO_L5N_SM4N_13	K17	
13	IO_L6P_SM3P_13	H15	
13	IO_L6N_SM3N_13	H16	
13	IO_L7P_SM2P_13	L18	

Table 2-1: **FF323 Package—LX20T and LX30T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
13	IO_L7N_SM2N_13	L17	
13	IO_L8P_CC_SM1P_13	N12	
13	IO_L8N_CC_SM1N_13 (2)	M11	
13	IO_L9P_CC_SM0P_13	K16	
13	IO_L9N_CC_SM0N_13 (2)	L16	
13	IO_L10P_CC_13	N18	
13	IO_L10N_CC_13 (2)	M18	
13	IO_L11P_CC_13	M14	
13	IO_L11N_CC_13 (2)	L13	
13	IO_L12P_VRN_13	P18	
13	IO_L12N_VRP_13	N17	
13	IO_L13P_13	L14	
13	IO_L13N_13	K14	
13	IO_L14P_13	R17	
13	IO_L14N_VREF_13	P17	
13	IO_L15P_13	N13	
13	IO_L15N_13	M13	
13	IO_L16P_13	R15	
13	IO_L16N_13	R16	
13	IO_L17P_13	P14	
13	IO_L17N_13	P15	
13	IO_L18P_13	N16	
13	IO_L18N_13	M16	
13	IO_L19P_13	N15	
13	IO_L19N_13	M15	
17	IO_L4P_17	M10	
17	IO_L4N_VREF_17	N11	
17	IO_L5P_17	T17	
17	IO_L5N_17	T16	
17	IO_L6P_17	T12	
17	IO_L6N_17	R12	
17	IO_L7P_17	T18	
17	IO_L7N_17	U18	

Table 2-1: **FF323 Package—LX20T and LX30T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
17	IO_L8P_CC_17	P10	
17	IO_L8N_CC_17 (2)	N10	
17	IO_L9P_CC_17	U16	
17	IO_L9N_CC_17 (2)	U15	
17	IO_L10P_CC_17	V18	
17	IO_L10N_CC_17 (2)	V17	
17	IO_L11P_CC_17	R10	
17	IO_L11N_CC_17 (2)	R11	
17	IO_L12P_VRN_17	V16	
17	IO_L12N_VRP_17	V15	
17	IO_L13P_17	T11	
17	IO_L13N_17	U11	
17	IO_L14P_17	R14	
17	IO_L14N_VREF_17	T14	
17	IO_L15P_17	V10	
17	IO_L15N_17	U10	
17	IO_L16P_17	U14	
17	IO_L16N_17	T13	
17	IO_L17P_17	P12	
17	IO_L17N_17	P13	
17	IO_L18P_17	U13	
17	IO_L18N_17	V13	
17	IO_L19P_17	V12	
17	IO_L19N_17	V11	
NA	MGTTXP0_112	A2	
NA	MGTAVTTTX_112	F3	
NA	MGTTXN0_112	B2	
NA	MGTRXP0_112	B1	
NA	MGTAVTTRX_112	B3	
NA	MGTRXN0_112	C1	
NA	MGTAVCCPLL_112	E4	
NA	MGTRXN1_112	D1	
NA	MGTREFCLKN_112	C4	

Table 2-1: **FF323 Package—LX20T and LX30T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	MGTRXP1_112	E1	
NA	MGTREFCLKP_112	C3	
NA	MGTTXN1_112	E2	
NA	MGTTXP1_112	F2	
NA	MGTRREF_112	F5	
NA	MGTTXP0_114	G2	
NA	MGTAVTTTX_114	M3	
NA	MGTTXN0_114	H2	
NA	MGTRXP0_114	H1	
NA	MGTAVTTRX_114	H3	
NA	MGTRXN0_114	J1	
NA	MGTAVCCPLL_114	L4	
NA	MGTRXN1_114	K1	
NA	MGTREFCLKN_114	J4	
NA	MGTRXP1_114	L1	
NA	MGTREFCLKP_114	J3	
NA	MGTTXN1_114	L2	
NA	MGTTXP1_114	M2	
NA	MGTAVTTRXC	G4	
NA	GND	A1	
NA	GND	A3	
NA	GND	A5	
NA	GND	B17	
NA	GND	B4	
NA	GND	C14	
NA	GND	C2	
NA	GND	C5	
NA	GND	C9	
NA	GND	D11	
NA	GND	D2	
NA	GND	D4	
NA	GND	D6	
NA	GND	E18	

Table 2-1: **FF323 Package—LX20T and LX30T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	E3	
NA	GND	E5	
NA	GND	F1	
NA	GND	F10	
NA	GND	F12	
NA	GND	F15	
NA	GND	F4	
NA	GND	G1	
NA	GND	G11	
NA	GND	G17	
NA	GND	G3	
NA	GND	G5	
NA	GND	G7	
NA	GND	H12	
NA	GND	H4	
NA	GND	H6	
NA	GND	H8	
NA	GND	J11	
NA	GND	J16	
NA	GND	J2	
NA	GND	J5	
NA	GND	J7	
NA	GND	K13	
NA	GND	K2	
NA	GND	K4	
NA	GND	K6	
NA	GND	K8	
NA	GND	L11	
NA	GND	L3	
NA	GND	L5	
NA	GND	L7	
NA	GND	M1	
NA	GND	M12	

Table 2-1: **FF323 Package—LX20T and LX30T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	M17	
NA	GND	M4	
NA	GND	N14	
NA	GND	N2	
NA	GND	N9	
NA	GND	P1	
NA	GND	P6	
NA	GND	R18	
NA	GND	T10	
NA	GND	T15	
NA	GND	U12	
NA	GND	U7	
NA	GND	V4	
NA	VCCAUX	G12	
NA	VCCAUX	J13	
NA	VCCAUX	K7	
NA	VCCAUX	L6	
NA	VCCAUX	L8	
NA	VCCINT	G8	
NA	VCCINT	H11	
NA	VCCINT	H7	
NA	VCCINT	J12	
NA	VCCINT	J6	
NA	VCCINT	J8	
NA	VCCINT	K11	
0	VCCO_0	K5	
0	VCCO_0	N4	
1	VCCO_1	A10	
1	VCCO_1	B7	
1	VCCO_1	E8	
2	VCCO_2	R3	
2	VCCO_2	T5	
2	VCCO_2	U2	

Table 2-1: **FF323 Package—LX20T and LX30T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
4	VCCO_4	R8	
4	VCCO_4	V9	
4	VCCO_4	M7	
11	VCCO_11	A15	
11	VCCO_11	B12	
11	VCCO_11	D16	
11	VCCO_11	E13	
13	VCCO_13	H14	
13	VCCO_13	K18	
13	VCCO_13	L15	
13	VCCO_13	P16	
17	VCCO_17	P11	
17	VCCO_17	R13	
17	VCCO_17	U17	
17	VCCO_17	V14	
NA	MGTAVCC_112	D3	
NA	MGTAVCC_114	K3	

Notes:

1. Do not connect a single-ended clock to the N-side of the differential clock pair of pins, for example, IO_L3N_GC_3.
2. Do not connect a single-ended clock to the N-side of clock capable pins, for example, IO_L8N_CC_11.
3. RSVD pins must be tied to GND (logic 0).

FF324 Package—LX30 and LX50

Table 2-2: **FF324 Package—LX30 and LX50**

Bank	Pin Description	Pin Number	No Connect (NC)
0	DXP_0	L10	
0	DXN_0	L9	
0	AVDD_0	H10	
0	AVSS_0	H9	
0	VP_0	J10	
0	VN_0	K9	
0	VREFP_0	K10	
0	VREFN_0	J9	
0	VBATT_0	T18	
0	PROGRAM_B_0	U18	
0	HSWAPEN_0	T17	
0	D_IN_0	R7	
0	DONE_0	P8	
0	CCLK_0	N8	
0	INIT_B_0	M8	
0	CS_B_0	R16	
0	RDWR_B_0	P15	
0	RSVD(3)	R14	
0	RSVD(3)	P14	
0	TCK_0	M9	
0	M0_0	N12	
0	M2_0	N13	
0	M1_0	L11	
0	TMS_0	V5	
0	TDI_0	U5	
0	D_OUT_BUSY_0	T6	
0	TDO_0	U6	
1	IO_L0P_A19_1	F11	
1	IO_L0N_A18_1	G11	
1	IO_L1P_A17_1	G10	
1	IO_L1N_A16_1	F9	

Table 2-2: **FF324 Package—LX30 and LX50 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
1	IO_L2P_A15_D31_1	E12	
1	IO_L2N_A14_D30_1	D12	
1	IO_L3P_A13_D29_1	F8	
1	IO_L3N_A12_D28_1	G9	
1	IO_L4P_A11_D27_1	C12	
1	IO_L4N_VREF_A10_D26_1	D13	
1	IO_L5P_A9_D25_1	G8	
1	IO_L5N_A8_D24_1	F7	
1	IO_L6P_A7_D23_1	F12	
1	IO_L6N_A6_D22_1	F13	
1	IO_L7P_A5_D21_1	D8	
1	IO_L7N_A4_D20_1	E7	
1	IO_L8P_CC_A3_D19_1	G13	
1	IO_L8N_CC_A2_D18_1 (2)	H13	
1	IO_L9P_CC_A1_D17_1	D7	
1	IO_L9N_CC_A0_D16_1 (2)	C6	
2	IO_L0P_CC_RS1_2	T8	
2	IO_L0N_CC_RS0_2 (2)	T7	
2	IO_L1P_CC_A25_2	R15	
2	IO_L1N_CC_A24_2 (2)	T16	
2	IO_L2P_A23_2	R9	
2	IO_L2N_A22_2	T9	
2	IO_L3P_A21_2	V18	
2	IO_L3N_A20_2	V17	
2	IO_L4P_FCS_B_2	P10	
2	IO_L4N_VREF_FOE_B_MOSI_2	P9	
2	IO_L5P_FWE_B_2	U16	
2	IO_L5N_CSO_B_2	V16	
2	IO_L6P_D7_2	N10	
2	IO_L6N_D6_2	M10	
2	IO_L7P_D5_2	T14	
2	IO_L7N_D4_2	T13	
2	IO_L8P_D3_2	N11	

Table 2-2: **FF324 Package—LX30 and LX50 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
2	IO_L8N_D2_FS2_2	M11	
2	IO_L9P_D1_FS1_2	P13	
2	IO_L9N_D0_FS0_2	P12	
3	IO_L0P_CC_GC_3	A8	
3	IO_L0N_CC_GC_3 (1)(2)	A9	
3	IO_L1P_CC_GC_3	B9	
3	IO_L1N_CC_GC_3 (1)(2)	B10	
3	IO_L2P_GC_VRN_3	E9	
3	IO_L2N_GC_VRP_3 (1)	D9	
3	IO_L3P_GC_3	E10	
3	IO_L3N_GC_3 (1)	E11	
3	IO_L4P_GC_3	C8	
3	IO_L4N_GC_VREF_3 (1)	B8	
3	IO_L5P_GC_3	D10	
3	IO_L5N_GC_3 (1)	C10	
3	IO_L6P_GC_3	A6	
3	IO_L6N_GC_3 (1)	A7	
3	IO_L7P_GC_3	B11	
3	IO_L7N_GC_3 (1)	C11	
3	IO_L8P_GC_3	B6	
3	IO_L8N_GC_3 (1)	C7	
3	IO_L9P_GC_3	A11	
3	IO_L9N_GC_3 (1)	A12	
4	IO_L0P_GC_D15_4	U15	
4	IO_L0N_GC_D14_4 (1)	V15	
4	IO_L1P_GC_D13_4	V7	
4	IO_L1N_GC_D12_4 (1)	V6	
4	IO_L2P_GC_D11_4	V13	
4	IO_L2N_GC_D10_4 (1)	V12	
4	IO_L3P_GC_D9_4	V8	
4	IO_L3N_GC_D8_4 (1)	U8	
4	IO_L4P_GC_4	U14	
4	IO_L4N_GC_VREF_4 (1)	U13	

Table 2-2: **FF324 Package—LX30 and LX50 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
4	IO_L5P_GC_4	U10	
4	IO_L5N_GC_4 (1)	U9	
4	IO_L6P_GC_4	R12	
4	IO_L6N_GC_4 (1)	T12	
4	IO_L7P_GC_VRN_4	V11	
4	IO_L7N_GC_VRP_4 (1)	V10	
4	IO_L8P_CC_GC_4	U11	
4	IO_L8N_CC_GC_4 (1)(2)	T11	
4	IO_L9P_CC_GC_4	R11	
4	IO_L9N_CC_GC_4 (1)(2)	R10	
11	IO_L0P_11	C15	
11	IO_L0N_11	C16	
11	IO_L1P_11	A13	
11	IO_L1N_11	A14	
11	IO_L2P_11	B14	
11	IO_L2N_11	B15	
11	IO_L3P_11	B16	
11	IO_L3N_11	A16	
11	IO_L4P_11	D14	
11	IO_L4N_VREF_11	E14	
11	IO_L5P_11	A17	
11	IO_L5N_11	A18	
11	IO_L6P_11	C13	
11	IO_L6N_11	B13	
11	IO_L7P_11	B18	
11	IO_L7N_11	C17	
11	IO_L8P_CC_11	F14	
11	IO_L8N_CC_11 (2)	G14	
11	IO_L9P_CC_11	F16	
11	IO_L9N_CC_11 (2)	E16	
11	IO_L10P_CC_SM15P_11	E17	
11	IO_L10N_CC_SM15N_11 (2)	D17	
11	IO_L11P_CC_SM14P_11	D15	

Table 2-2: **FF324 Package—LX30 and LX50 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
11	IO_L11N_CC_SM14N_11 (2)	E15	
11	IO_L12P_VRN_11	D18	
11	IO_L12N_VRP_11	C18	
11	IO_L13P_11	H15	
11	IO_L13N_11	G15	
11	IO_L14P_11	F18	
11	IO_L14N_VREF_11	F17	
11	IO_L15P_SM13P_11	H16	
11	IO_L15N_SM13N_11	G16	
11	IO_L16P_SM12P_11	H18	
11	IO_L16N_SM12N_11	G18	
11	IO_L17P_SM11P_11	H17	
11	IO_L17N_SM11N_11	J17	
11	IO_L18P_SM10P_11	K17	
11	IO_L18N_SM10N_11	J18	
11	IO_L19P_SM9P_11	J15	
11	IO_L19N_SM9N_11	J14	
12	IO_L0P_12	E6	
12	IO_L0N_12	F6	
12	IO_L1P_12	B5	
12	IO_L1N_12	C5	
12	IO_L2P_12	D5	
12	IO_L2N_12	D4	
12	IO_L3P_12	B4	
12	IO_L3N_12	A4	
12	IO_L4P_12	E5	
12	IO_L4N_VREF_12	E4	
12	IO_L5P_12	A3	
12	IO_L5N_12	B3	
12	IO_L6P_12	G5	
12	IO_L6N_12	G6	
12	IO_L7P_12	C3	
12	IO_L7N_12	D3	

Table 2-2: **FF324 Package—LX30 and LX50 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
12	IO_L8P_CC_12	H6	
12	IO_L8N_CC_12 (2)	H5	
12	IO_L9P_CC_12	D2	
12	IO_L9N_CC_12 (2)	C2	
12	IO_L10P_CC_12	A1	
12	IO_L10N_CC_12 (2)	A2	
12	IO_L11P_CC_12	G4	
12	IO_L11N_CC_12 (2)	F4	
12	IO_L12P_VRN_12	C1	
12	IO_L12N_VRP_12	B1	
12	IO_L13P_12	G3	
12	IO_L13N_12	F3	
12	IO_L14P_12	F1	
12	IO_L14N_VREF_12	E1	
12	IO_L15P_12	J5	
12	IO_L15N_12	J4	
12	IO_L16P_12	H3	
12	IO_L16N_12	J3	
12	IO_L17P_12	H2	
12	IO_L17N_12	J2	
12	IO_L18P_12	E2	
12	IO_L18N_12	F2	
12	IO_L19P_12	G1	
12	IO_L19N_12	H1	
13	IO_L0P_SM8P_13	K15	
13	IO_L0N_SM8N_13	L16	
13	IO_L1P_SM7P_13	L17	
13	IO_L1N_SM7N_13	K16	
13	IO_L2P_SM6P_13	K14	
13	IO_L2N_SM6N_13	L14	
13	IO_L3P_SM5P_13	M18	
13	IO_L3N_SM5N_13	L18	
13	IO_L4P_13	L13	

Table 2-2: **FF324 Package—LX30 and LX50 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
13	IO_L4N_VREF_13	M13	
13	IO_L5P_SM4P_13	P18	
13	IO_L5N_SM4N_13	N18	
13	IO_L6P_SM3P_13	M14	
13	IO_L6N_SM3N_13	N15	
13	IO_L7P_SM2P_13	P17	
13	IO_L7N_SM2N_13	R17	
13	IO_L8P_CC_SM1P_13	M15	
13	IO_L8N_CC_SM1N_13 (2)	M16	
13	IO_L9P_CC_SM0P_13	N16	
13	IO_L9N_CC_SM0N_13 (2)	N17	
18	IO_L0P_18	K5	
18	IO_L0N_18	K4	
18	IO_L1P_18	K2	
18	IO_L1N_18	K1	
18	IO_L2P_18	L6	
18	IO_L2N_18	M6	
18	IO_L3P_18	L2	
18	IO_L3N_18	L1	
18	IO_L4P_18	L4	
18	IO_L4N_VREF_18	L3	
18	IO_L5P_18	N1	
18	IO_L5N_18	M1	
18	IO_L6P_18	M4	
18	IO_L6N_18	M3	
18	IO_L7P_18	N2	
18	IO_L7N_18	N3	
18	IO_L8P_CC_18	N5	
18	IO_L8N_CC_18 (2)	M5	
18	IO_L9P_CC_18	P2	
18	IO_L9N_CC_18 (2)	P3	
18	IO_L10P_CC_18	R2	
18	IO_L10N_CC_18 (2)	R1	

Table 2-2: **FF324 Package—LX30 and LX50 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
18	IO_L11P_CC_18	N6	
18	IO_L11N_CC_18 (2)	P5	
18	IO_L12P_VRN_18	T2	
18	IO_L12N_VRP_18	T1	
18	IO_L13P_18	N7	
18	IO_L13N_18	P7	
18	IO_L14P_18	V1	
18	IO_L14N_VREF_18	U1	
18	IO_L15P_18	P4	
18	IO_L15N_18	R4	
18	IO_L16P_18	V2	
18	IO_L16N_18	V3	
18	IO_L17P_18	R5	
18	IO_L17N_18	R6	
18	IO_L18P_18	U3	
18	IO_L18N_18	T3	
18	IO_L19P_18	T4	
18	IO_L19N_18	U4	
NA	GND	D1	
NA	GND	J1	
NA	GND	P1	
NA	GND	B2	
NA	GND	M2	
NA	GND	U2	
NA	GND	E3	
NA	GND	R3	
NA	GND	H4	
NA	GND	V4	
NA	GND	A5	
NA	GND	L5	
NA	GND	D6	
NA	GND	K6	
NA	GND	P6	

Table 2-2: **FF324 Package—LX30 and LX50 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	G7	
NA	GND	J7	
NA	GND	L7	
NA	GND	U7	
NA	GND	H8	
NA	GND	K8	
NA	GND	C9	
NA	GND	N9	
NA	GND	F10	
NA	GND	T10	
NA	GND	J11	
NA	GND	B12	
NA	GND	H12	
NA	GND	K12	
NA	GND	M12	
NA	GND	E13	
NA	GND	J13	
NA	GND	R13	
NA	GND	H14	
NA	GND	V14	
NA	GND	A15	
NA	GND	L15	
NA	GND	D16	
NA	GND	P16	
NA	GND	B17	
NA	GND	G17	
NA	GND	U17	
NA	GND	E18	
NA	GND	K18	
NA	VCCAUX	J6	
NA	VCCAUX	H7	
NA	VCCAUX	M7	
NA	VCCAUX	G12	

Table 2-2: **FF324 Package—LX30 and LX50 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	VCCAUX	K13	
NA	VCCINT	K7	
NA	VCCINT	J8	
NA	VCCINT	L8	
NA	VCCINT	H11	
NA	VCCINT	K11	
NA	VCCINT	J12	
NA	VCCINT	L12	
0	VCCO_0	R18	
0	VCCO_0	T15	
1	VCCO_1	B7	
1	VCCO_1	E8	
2	VCCO_2	R8	
2	VCCO_2	V9	
3	VCCO_3	A10	
3	VCCO_3	D11	
4	VCCO_4	P11	
4	VCCO_4	U12	
11	VCCO_11	C14	
11	VCCO_11	F15	
11	VCCO_11	J16	
12	VCCO_12	C4	
12	VCCO_12	F5	
12	VCCO_12	G2	
13	VCCO_13	M17	
13	VCCO_13	N14	
18	VCCO_18	K3	
18	VCCO_18	N4	
18	VCCO_18	T5	

Notes:

1. Do not connect a single-ended clock to the N-side of the differential clock pair of pins, for example, IO_L3N_GC_3.
2. Do not connect a single-ended clock to the N-side of clock capable pins, for example, IO_L8N_CC_11.
3. RSVD pins must be tied to GND (logic 0).

FF665 Package—LX30T, FX30T, LX50T, SX35T, SX50T, and FX70T

Table 2-3: **FF665 Package—LX30T, FX30T, LX50T, SX35T, SX50T, and FX70T**

Bank	Pin Description	Pin Number	No Connect (NC)
0	DXP_0	R15	
0	DXN_0	R14	
0	AVDD_0	M15	
0	AVSS_0	M14	
0	VP_0	N15	
0	VN_0	P14	
0	VREFP_0	P15	
0	VREFN_0	N14	
0	VBATT_0	J19	
0	PROGRAM_B_0	J20	
0	HSWAPEN_0	K20	
0	D_IN_0	J10	
0	DONE_0	K11	
0	CCLK_0	J11	
0	INIT_B_0	H12	
0	CS_B_0	L20	
0	RDWR_B_0	M20	
0	RSVD(3)	P20	
0	RSVD(3)	R20	
0	TCK_0	V11	
0	M0_0	T20	
0	M2_0	U20	
0	M1_0	W20	
0	TMS_0	W13	
0	TDI_0	V13	
0	D_OUT_BUSY_0	U12	
0	TDO_0	V12	
1	IO_L0P_A19_1	G15	
1	IO_L0N_A18_1	G16	
1	IO_L1P_A17_1	H13	
1	IO_L1N_A16_1	G14	

Table 2-3: **FF665 Package—LX30T, FX30T, LX50T, SX35T, SX50T, and FX70T**

Bank	Pin Description	Pin Number	No Connect (NC)
1	IO_L2P_A15_D31_1	G17	
1	IO_L2N_A14_D30_1	F17	
1	IO_L3P_A13_D29_1	F15	
1	IO_L3N_A12_D28_1	F14	
1	IO_L4P_A11_D27_1	F18	
1	IO_L4N_VREF_A10_D26_1	G19	
1	IO_L5P_A9_D25_1	F13	
1	IO_L5N_A8_D24_1	G12	
1	IO_L6P_A7_D23_1	H18	
1	IO_L6N_A6_D22_1	H19	
1	IO_L7P_A5_D21_1	G11	
1	IO_L7N_A4_D20_1	H11	
1	IO_L8P_CC_A3_D19_1	G20	
1	IO_L8N_CC_A2_D18_1 (2)	H21	
1	IO_L9P_CC_A1_D17_1 (2)	G10	
1	IO_L9N_CC_A0_D16_1 (2)	H9	
2	IO_L0P_CC_RS1_2	W11	
2	IO_L0N_CC_RS0_2 (2)	Y10	
2	IO_L1P_CC_A25_2	Y20	
2	IO_L1N_CC_A24_2 (2)	AA19	
2	IO_L2P_A23_2	AA10	
2	IO_L2N_A22_2	Y11	
2	IO_L3P_A21_2	AA18	
2	IO_L3N_A20_2	Y18	
2	IO_L4P_FCS_B_2	Y12	
2	IO_L4N_VREF_FOE_B_MOSI_2	AA12	
2	IO_L5P_FWE_B_2	AA17	
2	IO_L5N_CSO_B_2	Y17	
2	IO_L6P_D7_2	AA13	
2	IO_L6N_D6_2	AA14	
2	IO_L7P_D5_2	Y16	
2	IO_L7N_D4_2	W16	
2	IO_L8P_D3_2	Y13	

Table 2-3: **FF665 Package—LX30T, FX30T, LX50T, SX35T, SX50T, and FX70T**

Bank	Pin Description	Pin Number	No Connect (NC)
2	IO_L8N_D2_FS2_2	W14	
2	IO_L9P_D1_FS1_2	Y15	
2	IO_L9N_D0_FS0_2	AA15	
3	IO_L0P_CC_GC_3	D15	
3	IO_L0N_CC_GC_3 (1)(2)	E15	
3	IO_L1P_CC_GC_3	D16	
3	IO_L1N_CC_GC_3 (1)(2)	E16	
3	IO_L2P_GC_VRN_3	D14	
3	IO_L2N_GC_VRP_3 (1)	D13	
3	IO_L3P_GC_3	E17	
3	IO_L3N_GC_3 (1)	D18	
3	IO_L4P_GC_3	E13	
3	IO_L4N_GC_VREF_3 (1)	E12	
3	IO_L5P_GC_3	E18	
3	IO_L5N_GC_3 (1)	F19	
3	IO_L6P_GC_3	F12	
3	IO_L6N_GC_3 (1)	E11	
3	IO_L7P_GC_3	E20	
3	IO_L7N_GC_3 (1)	E21	
3	IO_L8P_GC_3	E10	
3	IO_L8N_GC_3 (1)	F10	
3	IO_L9P_GC_3	F20	
3	IO_L9N_GC_3 (1)	G21	
4	IO_L0P_GC_D15_4	Y21	
4	IO_L0N_GC_D14_4 (1)	AA20	
4	IO_L1P_GC_D13_4	AB10	
4	IO_L1N_GC_D12_4 (1)	AB11	
4	IO_L2P_GC_D11_4	AB21	
4	IO_L2N_GC_D10_4 (1)	AB20	
4	IO_L3P_GC_D9_4	AC11	
4	IO_L3N_GC_D8_4 (1)	AB12	
4	IO_L4P_GC_4	AB19	
4	IO_L4N_GC_VREF_4 (1)	AC19	

Table 2-3: **FF665 Package—LX30T, FX30T, LX50T, SX35T, SX50T, and FX70T**

Bank	Pin Description	Pin Number	No Connect (NC)
4	IO_L5P_GC_4	AC12	
4	IO_L5N_GC_4 (1)	AC13	
4	IO_L6P_GC_4	AC18	
4	IO_L6N_GC_4 (1)	AB17	
4	IO_L7P_GC_VRN_4	AB14	
4	IO_L7N_GC_VRP_4 (1)	AC14	
4	IO_L8P_CC_GC_4	AC17	
4	IO_L8N_CC_GC_4 (1)(2)	AB16	
4	IO_L9P_CC_GC_4	AB15	
4	IO_L9N_CC_GC_4 (1)(2)	AC16	
11	IO_L0P_11	E26	
11	IO_L0N_11	E25	
11	IO_L1P_11	F25	
11	IO_L1N_11	G26	
11	IO_L2P_11	H26	
11	IO_L2N_11	G25	
11	IO_L3P_11	F24	
11	IO_L3N_11	G24	
11	IO_L4P_11	E23	
11	IO_L4N_VREF_11	E22	
11	IO_L5P_11	F23	
11	IO_L5N_11	F22	
11	IO_L6P_11	G22	
11	IO_L6N_11	H22	
11	IO_L7P_11	H23	
11	IO_L7N_11	J23	
11	IO_L8P_CC_11	J21	
11	IO_L8N_CC_11 (2)	K21	
11	IO_L9P_CC_11	K22	
11	IO_L9N_CC_11 (2)	K23	
11	IO_L10P_CC_SM15P_11	L23	
11	IO_L10N_CC_SM15N_11 (2)	L22	
11	IO_L11P_CC_SM14P_11	M21	

Table 2-3: **FF665 Package—LX30T, FX30T, LX50T, SX35T, SX50T, and FX70T**

Bank	Pin Description	Pin Number	No Connect (NC)
11	IO_L11N_CC_SM14N_11 (2)	N21	
11	IO_L12P_VRN_11	H24	
11	IO_L12N_VRP_11	J24	
11	IO_L13P_11	J25	
11	IO_L13N_11	J26	
11	IO_L14P_11	K26	
11	IO_L14N_VREF_11	L25	
11	IO_L15P_SM13P_11	L24	
11	IO_L15N_SM13N_11	K25	
11	IO_L16P_SM12P_11	N26	
11	IO_L16N_SM12N_11	M26	
11	IO_L17P_SM11P_11	M25	
11	IO_L17N_SM11N_11	M24	
11	IO_L18P_SM10P_11	N24	
11	IO_L18N_SM10N_11	N23	
11	IO_L19P_SM9P_11	N22	
11	IO_L19N_SM9N_11	M22	
12	IO_L0P_12	Y6	
12	IO_L0N_12	Y5	
12	IO_L1P_12	G6	
12	IO_L1N_12	H6	
12	IO_L2P_12	Y4	
12	IO_L2N_12	W4	
12	IO_L3P_12	G5	
12	IO_L3N_12	F5	
12	IO_L4P_12	W5	
12	IO_L4N_VREF_12	W6	
12	IO_L5P_12	G4	
12	IO_L5N_12	H4	
12	IO_L6P_12	V6	
12	IO_L6N_12	V7	
12	IO_L7P_12	J5	
12	IO_L7N_12	J6	

Table 2-3: **FF665 Package—LX30T, FX30T, LX50T, SX35T, SX50T, and FX70T**

Bank	Pin Description	Pin Number	No Connect (NC)
12	IO_L8P_CC_12	U7	
12	IO_L8N_CC_12 (2)	T8	
12	IO_L9P_CC_12	K5	
12	IO_L9N_CC_12 (2)	L5	
12	IO_L10P_CC_12	K6	
12	IO_L10N_CC_12 (2)	K7	
12	IO_L11P_CC_12	U6	
12	IO_L11N_CC_12 (2)	U5	
12	IO_L12P_VRN_12	K8	
12	IO_L12N_VRP_12	L7	
12	IO_L13P_12	T5	
12	IO_L13N_12	R5	
12	IO_L14P_12	M7	
12	IO_L14N_VREF_12	L8	
12	IO_L15P_12	R6	
12	IO_L15N_12	T7	
12	IO_L16P_12	P6	
12	IO_L16N_12	N6	
12	IO_L17P_12	M6	
12	IO_L17N_12	N7	
12	IO_L18P_12	N8	
12	IO_L18N_12	P8	
12	IO_L19P_12	R8	
12	IO_L19N_12	R7	
13	IO_L0P_SM8P_13	P26	
13	IO_L0N_SM8N_13	R26	
13	IO_L1P_SM7P_13	P25	
13	IO_L1N_SM7N_13	R25	
13	IO_L2P_SM6P_13	P24	
13	IO_L2N_SM6N_13	P23	
13	IO_L3P_SM5P_13	R23	
13	IO_L3N_SM5N_13	R22	
13	IO_L4P_13	U26	

Table 2-3: **FF665 Package—LX30T, FX30T, LX50T, SX35T, SX50T, and FX70T**

Bank	Pin Description	Pin Number	No Connect (NC)
13	IO_L4N_VREF_13	V26	
13	IO_L5P_SM4P_13	U25	
13	IO_L5N_SM4N_13	T25	
13	IO_L6P_SM3P_13	T24	
13	IO_L6N_SM3N_13	T23	
13	IO_L7P_SM2P_13	U24	
13	IO_L7N_SM2N_13	V24	
13	IO_L8P_CC_SM1P_13	W26	
13	IO_L8N_CC_SM1N_13 (2)	W25	
13	IO_L9P_CC_SM0P_13	W24	
13	IO_L9N_CC_SM0N_13 (2)	V23	
13	IO_L10P_CC_13	AA22	
13	IO_L10N_CC_13 (2)	Y22	
13	IO_L11P_CC_13	Y23	
13	IO_L11N_CC_13 (2)	W23	
13	IO_L12P_VRN_13	Y26	
13	IO_L12N_VRP_13	Y25	
13	IO_L13P_13	AA25	
13	IO_L13N_13	AB26	
13	IO_L14P_13	AB25	
13	IO_L14N_VREF_13	AA24	
13	IO_L15P_13	AB24	
13	IO_L15N_13	AA23	
13	IO_L16P_13	P21	
13	IO_L16N_13	R21	
13	IO_L17P_13	T22	
13	IO_L17N_13	U22	
13	IO_L18P_13	U21	
13	IO_L18N_13	V22	
13	IO_L19P_13	V21	
13	IO_L19N_13	W21	
15	IO_L0P_15	C13	
15	IO_L0N_15	C14	

Table 2-3: **FF665 Package—LX30T, FX30T, LX50T, SX35T, SX50T, and FX70T**

Bank	Pin Description	Pin Number	No Connect (NC)
15	IO_L1P_15	B14	
15	IO_L1N_15	A13	
15	IO_L2P_15	A14	
15	IO_L2N_15	A15	
15	IO_L3P_15	B15	
15	IO_L3N_15	C16	
15	IO_L4P_15	B16	
15	IO_L4N_VREF_15	C17	
15	IO_L5P_15	B17	
15	IO_L5N_15	A17	
15	IO_L6P_15	A18	
15	IO_L6N_15	A19	
15	IO_L7P_15	B19	
15	IO_L7N_15	C18	
15	IO_L8P_CC_15	A20	
15	IO_L8N_CC_15 (2)	B20	
15	IO_L9P_CC_15	C19	
15	IO_L9N_CC_15 (2)	D19	
15	IO_L10P_CC_15	D21	
15	IO_L10N_CC_15 (2)	D20	
15	IO_L11P_CC_15	B21	
15	IO_L11N_CC_15 (2)	C21	
15	IO_L12P_VRN_15	D23	
15	IO_L12N_VRP_15	C22	
15	IO_L13P_15	B22	
15	IO_L13N_15	A22	
15	IO_L14P_15	A23	
15	IO_L14N_VREF_15	A24	
15	IO_L15P_15	B24	
15	IO_L15N_15	C23	
15	IO_L16P_15	D24	
15	IO_L16N_15	C24	
15	IO_L17P_15	B25	

Table 2-3: **FF665 Package—LX30T, FX30T, LX50T, SX35T, SX50T, and FX70T**

Bank	Pin Description	Pin Number	No Connect (NC)
15	IO_L17N_15	A25	
15	IO_L18P_15	B26	
15	IO_L18N_15	C26	
15	IO_L19P_15	D26	
15	IO_L19N_15	D25	
16	IO_L0P_16	H7	
16	IO_L0N_16	G7	
16	IO_L1P_16	F7	
16	IO_L1N_16	F8	
16	IO_L2P_16	F9	
16	IO_L2N_16	G9	
16	IO_L3P_16	H8	
16	IO_L3N_16	J8	
16	IO_L4P_16	A9	
16	IO_L4N_VREF_16	A8	
16	IO_L5P_16	E8	
16	IO_L5N_16	E7	
16	IO_L6P_16	B9	
16	IO_L6N_16	C8	
16	IO_L7P_16	E6	
16	IO_L7N_16	D6	
16	IO_L8P_CC_16	C9	
16	IO_L8N_CC_16 (2)	D8	
16	IO_L9P_CC_16	C7	
16	IO_L9N_CC_16 (2)	C6	
16	IO_L10P_CC_16	A7	
16	IO_L10N_CC_16 (2)	B7	
16	IO_L11P_CC_16	D9	
16	IO_L11N_CC_16 (2)	D10	
16	IO_L12P_VRN_16	B6	
16	IO_L12N_VRP_16	A5	
16	IO_L13P_16	B10	
16	IO_L13N_16	A10	

Table 2-3: **FF665 Package—LX30T, FX30T, LX50T, SX35T, SX50T, and FX70T**

Bank	Pin Description	Pin Number	No Connect (NC)
16	IO_L14P_16	A4	
16	IO_L14N_VREF_16	A3	
16	IO_L15P_16	B11	
16	IO_L15N_16	A12	
16	IO_L16P_16	B4	
16	IO_L16N_16	B5	
16	IO_L17P_16	B12	
16	IO_L17N_16	C12	
16	IO_L18P_16	D5	
16	IO_L18N_16	E5	
16	IO_L19P_16	C11	
16	IO_L19N_16	D11	
17	IO_L0P_17	AC26	
17	IO_L0N_17	AD26	
17	IO_L1P_17	AD25	
17	IO_L1N_17	AD24	
17	IO_L2P_17	AE25	
17	IO_L2N_17	AE26	
17	IO_L3P_17	AF25	
17	IO_L3N_17	AF24	
17	IO_L4P_17	AF23	
17	IO_L4N_VREF_17	AE23	
17	IO_L5P_17	AE22	
17	IO_L5N_17	AD23	
17	IO_L6P_17	AC24	
17	IO_L6N_17	AC23	
17	IO_L7P_17	AC22	
17	IO_L7N_17	AB22	
17	IO_L8P_CC_17	AF22	
17	IO_L8N_CC_17 (2)	AE21	
17	IO_L9P_CC_17	AF20	
17	IO_L9N_CC_17 (2)	AE20	
17	IO_L10P_CC_17	AD19	

Table 2-3: **FF665 Package—LX30T, FX30T, LX50T, SX35T, SX50T, and FX70T**

Bank	Pin Description	Pin Number	No Connect (NC)
17	IO_L10N_CC_17 (2)	AD20	
17	IO_L11P_CC_17	AC21	
17	IO_L11N_CC_17 (2)	AD21	
17	IO_L12P_VRN_17	AF19	
17	IO_L12N_VRP_17	AF18	
17	IO_L13P_17	AE18	
17	IO_L13N_17	AD18	
17	IO_L14P_17	AE17	
17	IO_L14N_VREF_17	AF17	
17	IO_L15P_17	AE16	
17	IO_L15N_17	AD16	
17	IO_L16P_17	AD15	
17	IO_L16N_17	AE15	
17	IO_L17P_17	AF15	
17	IO_L17N_17	AF14	
17	IO_L18P_17	AF13	
17	IO_L18N_17	AE13	
17	IO_L19P_17	AD13	
17	IO_L19N_17	AD14	
18	IO_L0P_18	AF12	
18	IO_L0N_18	AE12	
18	IO_L1P_18	V8	
18	IO_L1N_18	V9	
18	IO_L2P_18	AE11	
18	IO_L2N_18	AD11	
18	IO_L3P_18	W9	
18	IO_L3N_18	W8	
18	IO_L4P_18	AD10	
18	IO_L4N_VREF_18	AE10	
18	IO_L5P_18	Y7	
18	IO_L5N_18	Y8	
18	IO_L6P_18	AF9	
18	IO_L6N_18	AF10	

Table 2-3: **FF665 Package—LX30T, FX30T, LX50T, SX35T, SX50T, and FX70T**

Bank	Pin Description	Pin Number	No Connect (NC)
18	IO_L7P_18	AA7	
18	IO_L7N_18	AA8	
18	IO_L8P_CC_18	AF7	
18	IO_L8N_CC_18 (2)	AF8	
18	IO_L9P_CC_18	AA5	
18	IO_L9N_CC_18 (2)	AB5	
18	IO_L10P_CC_18	AB6	
18	IO_L10N_CC_18 (2)	AB7	
18	IO_L11P_CC_18	AE8	
18	IO_L11N_CC_18 (2)	AE7	
18	IO_L12P_VRN_18	AC6	
18	IO_L12N_VRP_18	AD5	
18	IO_L13P_18	AE6	
18	IO_L13N_18	AF5	
18	IO_L14P_18	AE5	
18	IO_L14N_VREF_18	AD4	
18	IO_L15P_18	AF4	
18	IO_L15N_18	AF3	
18	IO_L16P_18	AD6	
18	IO_L16N_18	AC7	
18	IO_L17P_18	AC8	
18	IO_L17N_18	AD8	
18	IO_L18P_18	AD9	
18	IO_L18N_18	AC9	
18	IO_L19P_18	AB9	
18	IO_L19N_18	AA9	
NA	MGTTXP0_112	H2	
NA	MGTAVTTTX_112	H3	
NA	MGTTXN0_112	J2	
NA	MGTRXP0_112	J1	
NA	MGTAVTTRX_112	J3	
NA	MGTRXN0_112	K1	
NA	MGTAVCCPLL_112	M3	

Table 2-3: **FF665 Package—LX30T, FX30T, LX50T, SX35T, SX50T, and FX70T**

Bank	Pin Description	Pin Number	No Connect (NC)
NA	MGTRXN1_112	L1	
NA	MGTREFCLKN_112	K3	
NA	MGTRXP1_112	M1	
NA	MGTREFCLKP_112	K4	
NA	MGTTXN1_112	M2	
NA	MGTAVTTTX_112	N3	
NA	MGTTXP1_112	N2	
NA	MGTAVTTRXC	P5	
NA	MGTRREF_112	P4	
NC	NC	M5	LX30T, FX30T, LX50T, SX35T, SX50T, FX70T
NA	MGTTXP0_114	P2	
NA	MGTAVTTTX_114	P3	
NA	MGTTXN0_114	R2	
NA	MGTRXP0_114	R1	
NA	MGTAVTTRX_114	R3	
NA	MGTRXN0_114	T1	
NA	MGTAVCCPLL_114	V3	
NA	MGTRXN1_114	U1	
NA	MGTREFCLKN_114	T3	
NA	MGTRXP1_114	V1	
NA	MGTREFCLKP_114	T4	
NA	MGTTXN1_114	V2	
NA	MGTAVTTTX_114	W3	
NA	MGTTXP1_114	W2	
NA	MGTTXP0_116	B2	
NA	MGTAVTTTX_116	B3	
NA	MGTTXN0_116	C2	
NA	MGTRXP0_116	C1	
NA	MGTAVTTRX_116	C3	
NA	MGTRXN0_116	D1	
NA	MGTAVCCPLL_116	F3	
NA	MGTRXN1_116	E1	

Table 2-3: **FF665 Package—LX30T, FX30T, LX50T, SX35T, SX50T, and FX70T**

Bank	Pin Description	Pin Number	No Connect (NC)
NA	MGTREFCLKN_116	D3	
NA	MGTRXP1_116	F1	
NA	MGTREFCLKP_116	D4	
NA	MGTTXN1_116	F2	
NA	MGTAVTTTX_116	G3	
NA	MGTTXP1_116	G2	
NA	MGTTXP0_118	Y2	
NA	MGTAVTTTX_118	Y3	
NA	MGTTXN0_118	AA2	
NA	MGTRXP0_118	AA1	
NA	MGTAVTTRX_118	AA3	
NA	MGTRXN0_118	AB1	
NA	MGTAVCCPLL_118	AD3	
NA	MGTRXN1_118	AC1	
NA	MGTREFCLKN_118	AB3	
NA	MGTRXP1_118	AD1	
NA	MGTREFCLKP_118	AB4	
NA	MGTTXN1_118	AD2	
NA	MGTAVTTTX_118	AE3	
NA	MGTTXP1_118	AE2	
NA	GND	A2	
NA	GND	D2	
NA	GND	E2	
NA	GND	K2	
NA	GND	L2	
NA	GND	T2	
NA	GND	U2	
NA	GND	AB2	
NA	GND	AC2	
NA	GND	AF2	
NA	GND	C4	
NA	GND	F4	
NA	GND	J4	

Table 2-3: **FF665 Package—LX30T, FX30T, LX50T, SX35T, SX50T, and FX70T**

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	M4	
NA	GND	R4	
NA	GND	V4	
NA	GND	AA4	
NA	GND	AE4	
NA	GND	C5	
NA	GND	N5	
NA	GND	V5	
NA	GND	AC5	
NA	GND	A6	
NA	GND	F6	
NA	GND	T6	
NA	GND	AF6	
NA	GND	J7	
NA	GND	W7	
NA	GND	B8	
NA	GND	M8	
NA	GND	AB8	
NA	GND	E9	
NA	GND	L9	
NA	GND	N9	
NA	GND	R9	
NA	GND	U9	
NA	GND	Y9	
NA	GND	AE9	
NA	GND	H10	
NA	GND	K10	
NA	GND	M10	
NA	GND	P10	
NA	GND	T10	
NA	GND	V10	
NA	GND	A11	
NA	GND	L11	

Table 2-3: **FF665 Package—LX30T, FX30T, LX50T, SX35T, SX50T, and FX70T**

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	N11	
NA	GND	R11	
NA	GND	U11	
NA	GND	AA11	
NA	GND	AF11	
NA	GND	D12	
NA	GND	K12	
NA	GND	M12	
NA	GND	P12	
NA	GND	T12	
NA	GND	W12	
NA	GND	AD12	
NA	GND	G13	
NA	GND	J13	
NA	GND	L13	
NA	GND	N13	
NA	GND	R13	
NA	GND	U13	
NA	GND	H14	
NA	GND	K14	
NA	GND	T14	
NA	GND	V14	
NA	GND	Y14	
NA	GND	C15	
NA	GND	J15	
NA	GND	L15	
NA	GND	U15	
NA	GND	W15	
NA	GND	AC15	
NA	GND	A16	
NA	GND	F16	
NA	GND	H16	
NA	GND	K16	

Table 2-3: **FF665 Package—LX30T, FX30T, LX50T, SX35T, SX50T, and FX70T**

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	M16	
NA	GND	P16	
NA	GND	T16	
NA	GND	V16	
NA	GND	AF16	
NA	GND	J17	
NA	GND	L17	
NA	GND	N17	
NA	GND	R17	
NA	GND	U17	
NA	GND	W17	
NA	GND	B18	
NA	GND	K18	
NA	GND	M18	
NA	GND	P18	
NA	GND	T18	
NA	GND	V18	
NA	GND	AB18	
NA	GND	E19	
NA	GND	L19	
NA	GND	N19	
NA	GND	R19	
NA	GND	U19	
NA	GND	W19	
NA	GND	AE19	
NA	GND	C20	
NA	GND	H20	
NA	GND	V20	
NA	GND	A21	
NA	GND	L21	
NA	GND	T21	
NA	GND	AA21	
NA	GND	AF21	

Table 2-3: **FF665 Package—LX30T, FX30T, LX50T, SX35T, SX50T, and FX70T**

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	D22	
NA	GND	P22	
NA	GND	AD22	
NA	GND	G23	
NA	GND	U23	
NA	GND	K24	
NA	GND	Y24	
NA	GND	C25	
NA	GND	N25	
NA	GND	AC25	
NA	GND	A26	
NA	GND	F26	
NA	GND	L26	
NA	GND	T26	
NA	GND	AA26	
NA	GND	AF26	
NA	VCCAUX	U8	
NA	VCCAUX	K9	
NA	VCCAUX	M9	
NA	VCCAUX	P9	
NA	VCCAUX	T9	
NA	VCCAUX	W10	
NA	VCCAUX	M19	
NA	VCCAUX	P19	
NA	VCCAUX	T19	
NA	VCCAUX	V19	
NA	VCCAUX	Y19	
NA	VCCAUX	N20	
NA	VCCINT	L10	
NA	VCCINT	N10	
NA	VCCINT	R10	
NA	VCCINT	U10	
NA	VCCINT	M11	

Table 2-3: **FF665 Package—LX30T, FX30T, LX50T, SX35T, SX50T, and FX70T**

Bank	Pin Description	Pin Number	No Connect (NC)
NA	VCCINT	P11	
NA	VCCINT	T11	
NA	VCCINT	L12	
NA	VCCINT	N12	
NA	VCCINT	R12	
NA	VCCINT	K13	
NA	VCCINT	M13	
NA	VCCINT	P13	
NA	VCCINT	T13	
NA	VCCINT	J14	
NA	VCCINT	L14	
NA	VCCINT	U14	
NA	VCCINT	H15	
NA	VCCINT	K15	
NA	VCCINT	T15	
NA	VCCINT	V15	
NA	VCCINT	J16	
NA	VCCINT	L16	
NA	VCCINT	N16	
NA	VCCINT	R16	
NA	VCCINT	U16	
NA	VCCINT	H17	
NA	VCCINT	K17	
NA	VCCINT	M17	
NA	VCCINT	P17	
NA	VCCINT	T17	
NA	VCCINT	V17	
NA	VCCINT	J18	
NA	VCCINT	L18	
NA	VCCINT	N18	
NA	VCCINT	R18	
NA	VCCINT	U18	
NA	VCCINT	W18	

Table 2-3: **FF665 Package—LX30T, FX30T, LX50T, SX35T, SX50T, and FX70T**

Bank	Pin Description	Pin Number	No Connect (NC)
NA	VCCINT	K19	
0	VCCO_0	F11	
0	VCCO_0	J12	
1	VCCO_1	B13	
1	VCCO_1	E14	
2	VCCO_2	AA16	
2	VCCO_2	AD17	
3	VCCO_3	D17	
3	VCCO_3	G18	
4	VCCO_4	AB13	
4	VCCO_4	AE14	
11	VCCO_11	J22	
11	VCCO_11	M23	
11	VCCO_11	H25	
12	VCCO_12	H5	
12	VCCO_12	L6	
12	VCCO_12	P7	
13	VCCO_13	W22	
13	VCCO_13	R24	
13	VCCO_13	V25	
15	VCCO_15	F21	
15	VCCO_15	B23	
15	VCCO_15	E24	
16	VCCO_16	D7	
16	VCCO_16	G8	
16	VCCO_16	C10	
17	VCCO_17	AC20	
17	VCCO_17	AB23	
17	VCCO_17	AE24	
18	VCCO_18	AA6	
18	VCCO_18	AD7	
18	VCCO_18	AC10	
NA	MGTAVCC_112	L3	

Table 2-3: **FF665 Package—LX30T, FX30T, LX50T, SX35T, SX50T, and FX70T**

Bank	Pin Description	Pin Number	No Connect (NC)
NA	MGTAVCC_112	L4	
NA	MGTAVCC_114	U3	
NA	MGTAVCC_114	U4	
NA	MGTAVCC_116	E3	
NA	MGTAVCC_116	E4	
NA	MGTAVCC_118	AC3	
NA	MGTAVCC_118	AC4	
NA	FLOAT	N4	

Notes:

1. Do not connect a single-ended clock to the N-side of the differential clock pair of pins, for example, IO_L3N_GC_3.
2. Do not connect a single-ended clock to the N-side of clock capable pins, for example, IO_L8N_CC_11.
3. RSVD pins must be tied to GND (logic 0).

FF676 Package—LX30, LX50, LX85, and LX110

Table 2-4: **FF676 Package—LX30, LX50, LX85, and LX110**

Bank	Pin Description	Pin Number	No Connect (NC)
0	DXP_0	R14	
0	DXN_0	R13	
0	AVDD_0	M14	
0	AVSS_0	M13	
0	VP_0	N14	
0	VN_0	P13	
0	VREFP_0	P14	
0	VREFN_0	N13	
0	VBATT_0	K18	
0	PROGRAM_B_0	J18	
0	HSWAPEN_0	L18	
0	D_IN_0	K11	
0	DONE_0	K10	
0	CCLK_0	J10	
0	INIT_B_0	J11	
0	CS_B_0	N18	
0	RDWR_B_0	P18	
0	RSVD(3)	R18	
0	RSVD(3)	T18	
0	TCK_0	U11	
0	M0_0	W18	
0	M2_0	V18	
0	M1_0	Y17	
0	TMS_0	V12	
0	TDI_0	V11	
0	D_OUT_BUSY_0	W11	
0	TDO_0	W10	
1	IO_L0P_A19_1	G14	
1	IO_L0N_A18_1	F13	
1	IO_L1P_A17_1	H14	
1	IO_L1N_A16_1	H13	

Table 2-4: **FF676 Package—LX30, LX50, LX85, and LX110 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
1	IO_L2P_A15_D31_1	F15	
1	IO_L2N_A14_D30_1	G15	
1	IO_L3P_A13_D29_1	G12	
1	IO_L3N_A12_D28_1	H12	
1	IO_L4P_A11_D27_1	G16	
1	IO_L4N_VREF_A10_D26_1	H16	
1	IO_L5P_A9_D25_1	H11	
1	IO_L5N_A8_D24_1	G11	
1	IO_L6P_A7_D23_1	H17	
1	IO_L6N_A6_D22_1	G17	
1	IO_L7P_A5_D21_1	G10	
1	IO_L7N_A4_D20_1	G9	
1	IO_L8P_CC_A3_D19_1	G19	
1	IO_L8N_CC_A2_D18_1 (2)	H18	
1	IO_L9P_CC_A1_D17_1	H9	
1	IO_L9N_CC_A0_D16_1 (2)	H8	
2	IO_L0P_CC_RS1_2	Y10	
2	IO_L0N_CC_RS0_2 (2)	Y11	
2	IO_L1P_CC_A25_2	AA18	
2	IO_L1N_CC_A24_2 (2)	Y18	
2	IO_L2P_A23_2	Y8	
2	IO_L2N_A22_2	AA8	
2	IO_L3P_A21_2	AA17	
2	IO_L3N_A20_2	AB17	
2	IO_L4P_FCS_B_2	AA10	
2	IO_L4N_VREF_FOE_B_MOSI_2	AA9	
2	IO_L5P_FWE_B_2	AB15	
2	IO_L5N_CSO_B_2	AB16	
2	IO_L6P_D7_2	Y12	
2	IO_L6N_D6_2	Y13	
2	IO_L7P_D5_2	AA15	
2	IO_L7N_D4_2	AB14	
2	IO_L8P_D3_2	AA12	

Table 2-4: **FF676 Package—LX30, LX50, LX85, and LX110 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
2	IO_L8N_D2_FS2_2	AB11	
2	IO_L9P_D1_FS1_2	AA13	
2	IO_L9N_D0_FS0_2	AA14	
3	IO_L0P_CC_GC_3	F14	
3	IO_L0N_CC_GC_3 (1)(2)	E13	
3	IO_L1P_CC_GC_3	D13	
3	IO_L1N_CC_GC_3 (1)(2)	D14	
3	IO_L2P_GC_VRN_3	E12	
3	IO_L2N_GC_VRP_3 (1)	F12	
3	IO_L3P_GC_3	D15	
3	IO_L3N_GC_3 (1)	E15	
3	IO_L4P_GC_3	E10	
3	IO_L4N_GC_VREF_3 (1)	E11	
3	IO_L5P_GC_3	E16	
3	IO_L5N_GC_3 (1)	E17	
3	IO_L6P_GC_3	F9	
3	IO_L6N_GC_3 (1)	F10	
3	IO_L7P_GC_3	E18	
3	IO_L7N_GC_3 (1)	F19	
3	IO_L8P_GC_3	F8	
3	IO_L8N_GC_3 (1)	E8	
3	IO_L9P_GC_3	F18	
3	IO_L9N_GC_3 (1)	F17	
4	IO_L0P_GC_D15_4	AD18	
4	IO_L0N_GC_D14_4 (1)	AC18	
4	IO_L1P_GC_D13_4	AB10	
4	IO_L1N_GC_D12_4 (1)	AB9	
4	IO_L2P_GC_D11_4	AC17	
4	IO_L2N_GC_D10_4 (1)	AC16	
4	IO_L3P_GC_D9_4	AC8	
4	IO_L3N_GC_D8_4 (1)	AC9	
4	IO_L4P_GC_4	AD15	
4	IO_L4N_GC_VREF_4 (1)	AD14	

Table 2-4: **FF676 Package—LX30, LX50, LX85, and LX110 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
4	IO_L5P_GC_4	AD8	
4	IO_L5N_GC_4 (1)	AC7	
4	IO_L6P_GC_4	AD13	
4	IO_L6N_GC_4 (1)	AC14	
4	IO_L7P_GC_VRN_4	AB12	
4	IO_L7N_GC_VRP_4 (1)	AC11	
4	IO_L8P_CC_GC_4	AC13	
4	IO_L8N_CC_GC_4 (1)(2)	AC12	
4	IO_L9P_CC_GC_4	AD11	
4	IO_L9N_CC_GC_4 (1)(2)	AD10	
11	IO_L0P_11	G20	
11	IO_L0N_11	F20	
11	IO_L1P_11	E21	
11	IO_L1N_11	E20	
11	IO_L2P_11	E22	
11	IO_L2N_11	E23	
11	IO_L3P_11	F22	
11	IO_L3N_11	F23	
11	IO_L4P_11	G21	
11	IO_L4N_VREF_11	G22	
11	IO_L5P_11	H21	
11	IO_L5N_11	H22	
11	IO_L6P_11	J19	
11	IO_L6N_11	H19	
11	IO_L7P_11	H23	
11	IO_L7N_11	J23	
11	IO_L8P_CC_11	J21	
11	IO_L8N_CC_11 (2)	J20	
11	IO_L9P_CC_11	K21	
11	IO_L9N_CC_11 (2)	K20	
11	IO_L10P_CC_SM15P_11	K23	
11	IO_L10N_CC_SM15N_11 (2)	K22	
11	IO_L11P_CC_SM14P_11	L20	

Table 2-4: **FF676 Package—LX30, LX50, LX85, and LX110 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
11	IO_L11N_CC_SM14N_11(2)	L19	
11	IO_L12P_VRN_11	L23	
11	IO_L12N_VRP_11	L22	
11	IO_L13P_11	M22	
11	IO_L13N_11	M21	
11	IO_L14P_11	P19	
11	IO_L14N_VREF_11	N19	
11	IO_L15P_SM13P_11	M20	
11	IO_L15N_SM13N_11	M19	
11	IO_L16P_SM12P_11	P23	
11	IO_L16N_SM12N_11	N23	
11	IO_L17P_SM11P_11	N22	
11	IO_L17N_SM11N_11	N21	
11	IO_L18P_SM10P_11	R22	
11	IO_L18N_SM10N_11	R23	
11	IO_L19P_SM9P_11	P21	
11	IO_L19N_SM9N_11	P20	
12	IO_L0P_12	E7	
12	IO_L0N_12	F7	
12	IO_L1P_12	E6	
12	IO_L1N_12	E5	
12	IO_L2P_12	G6	
12	IO_L2N_12	G7	
12	IO_L3P_12	F5	
12	IO_L3N_12	F4	
12	IO_L4P_12	J6	
12	IO_L4N_VREF_12	H7	
12	IO_L5P_12	H6	
12	IO_L5N_12	G5	
12	IO_L6P_12	H4	
12	IO_L6N_12	G4	
12	IO_L7P_12	J5	
12	IO_L7N_12	J4	

Table 2-4: **FF676 Package—LX30, LX50, LX85, and LX110 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
12	IO_L8P_CC_12	K6	
12	IO_L8N_CC_12 (2)	K7	
12	IO_L9P_CC_12	L7	
12	IO_L9N_CC_12 (2)	M7	
12	IO_L10P_CC_12	K5	
12	IO_L10N_CC_12 (2)	L5	
12	IO_L11P_CC_12	L4	
12	IO_L11N_CC_12 (2)	L3	
12	IO_L12P_VRN_12	M5	
12	IO_L12N_VRP_12	M6	
12	IO_L13P_12	N7	
12	IO_L13N_12	N6	
12	IO_L14P_12	P3	
12	IO_L14N_VREF_12	N3	
12	IO_L15P_12	M4	
12	IO_L15N_12	N4	
12	IO_L16P_12	P5	
12	IO_L16N_12	P4	
12	IO_L17P_12	R3	
12	IO_L17N_12	T3	
12	IO_L18P_12	R6	
12	IO_L18N_12	R5	
12	IO_L19P_12	P6	
12	IO_L19N_12	R7	
13	IO_L0P_SM8P_13	F24	
13	IO_L0N_SM8N_13	F25	
13	IO_L1P_SM7P_13	E25	
13	IO_L1N_SM7N_13	E26	
13	IO_L2P_SM6P_13	G26	
13	IO_L2N_SM6N_13	H26	
13	IO_L3P_SM5P_13	G24	
13	IO_L3N_SM5N_13	G25	
13	IO_L4P_13	J25	

Table 2-4: **FF676 Package—LX30, LX50, LX85, and LX110 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
13	IO_L4N_VREF_13	J26	
13	IO_L5P_SM4P_13	H24	
13	IO_L5N_SM4N_13	J24	
13	IO_L6P_SM3P_13	L24	
13	IO_L6N_SM3N_13	L25	
13	IO_L7P_SM2P_13	K25	
13	IO_L7N_SM2N_13	K26	
13	IO_L8P_CC_SM1P_13	M25	
13	IO_L8N_CC_SM1N_13 (2)	M26	
13	IO_L9P_CC_SM0P_13	M24	
13	IO_L9N_CC_SM0N_13 (2)	N24	
13	IO_L10P_CC_13	P26	
13	IO_L10N_CC_13 (2)	N26	
13	IO_L11P_CC_13	P25	
13	IO_L11N_CC_13 (2)	P24	
13	IO_L12P_VRN_13	R25	
13	IO_L12N_VRP_13	R26	
13	IO_L13P_13	T24	
13	IO_L13N_13	T25	
13	IO_L14P_13	V26	
13	IO_L14N_VREF_13	U26	
13	IO_L15P_13	U24	
13	IO_L15N_13	U25	
13	IO_L16P_13	W25	
13	IO_L16N_13	W26	
13	IO_L17P_13	Y25	
13	IO_L17N_13	Y26	
13	IO_L18P_13	AB25	
13	IO_L18N_13	AA25	
13	IO_L19P_13	AC26	
13	IO_L19N_13	AB26	
14	IO_L0P_14	E2	
14	IO_L0N_14	E1	

Table 2-4: **FF676 Package—LX30, LX50, LX85, and LX110 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
14	IO_L1P_14	F3	
14	IO_L1N_14	E3	
14	IO_L2P_14	G1	
14	IO_L2N_14	H1	
14	IO_L3P_14	F2	
14	IO_L3N_14	G2	
14	IO_L4P_14	K3	
14	IO_L4N_VREF_14	K2	
14	IO_L5P_14	H3	
14	IO_L5N_14	J3	
14	IO_L6P_14	L2	
14	IO_L6N_14	K1	
14	IO_L7P_14	J1	
14	IO_L7N_14	H2	
14	IO_L8P_CC_14	M1	
14	IO_L8N_CC_14 (2)	N1	
14	IO_L9P_CC_14	M2	
14	IO_L9N_CC_14 (2)	N2	
14	IO_L10P_CC_14	P1	
14	IO_L10N_CC_14 (2)	R1	
14	IO_L11P_CC_14	T2	
14	IO_L11N_CC_14 (2)	R2	
14	IO_L12P_VRN_14	U2	
14	IO_L12N_VRP_14	U1	
14	IO_L13P_14	V2	
14	IO_L13N_14	V1	
14	IO_L14P_14	Y1	
14	IO_L14N_VREF_14	W1	
14	IO_L15P_14	AA2	
14	IO_L15N_14	Y2	
14	IO_L16P_14	AB2	
14	IO_L16N_14	AB1	
14	IO_L17P_14	AC2	

Table 2-4: **FF676 Package—LX30, LX50, LX85, and LX110 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
14	IO_L17N_14	AC1	
14	IO_L18P_14	AE1	
14	IO_L18N_14	AD1	
14	IO_L19P_14	AF2	
14	IO_L19N_14	AE2	
15	IO_L0P_15	C14	
15	IO_L0N_15	B14	
15	IO_L1P_15	A14	
15	IO_L1N_15	A15	
15	IO_L2P_15	B15	
15	IO_L2N_15	B16	
15	IO_L3P_15	D16	
15	IO_L3N_15	C16	
15	IO_L4P_15	D18	
15	IO_L4N_VREF_15	C17	
15	IO_L5P_15	B17	
15	IO_L5N_15	A17	
15	IO_L6P_15	A18	
15	IO_L6N_15	A19	
15	IO_L7P_15	B19	
15	IO_L7N_15	C18	
15	IO_L8P_CC_15	A20	
15	IO_L8N_CC_15 (2)	B20	
15	IO_L9P_CC_15	C19	
15	IO_L9N_CC_15 (2)	D19	
15	IO_L10P_CC_15	D21	
15	IO_L10N_CC_15 (2)	D20	
15	IO_L11P_CC_15	C21	
15	IO_L11N_CC_15 (2)	B21	
15	IO_L12P_VRN_15	D23	
15	IO_L12N_VRP_15	C22	
15	IO_L13P_15	B22	
15	IO_L13N_15	A22	

Table 2-4: **FF676 Package—LX30, LX50, LX85, and LX110 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
15	IO_L14P_15	A23	
15	IO_L14N_VREF_15	A24	
15	IO_L15P_15	B24	
15	IO_L15N_15	C23	
15	IO_L16P_15	D24	
15	IO_L16N_15	C24	
15	IO_L17P_15	B25	
15	IO_L17N_15	A25	
15	IO_L18P_15	B26	
15	IO_L18N_15	C26	
15	IO_L19P_15	D26	
15	IO_L19N_15	D25	
16	IO_L0P_16	D11	
16	IO_L0N_16	D10	
16	IO_L1P_16	C11	
16	IO_L1N_16	C12	
16	IO_L2P_16	C13	
16	IO_L2N_16	B12	
16	IO_L3P_16	A13	
16	IO_L3N_16	A12	
16	IO_L4P_16	C9	
16	IO_L4N_VREF_16	D9	
16	IO_L5P_16	B9	
16	IO_L5N_16	B10	
16	IO_L6P_16	B11	
16	IO_L6N_16	A10	
16	IO_L7P_16	A9	
16	IO_L7N_16	A8	
16	IO_L8P_CC_16	D8	
16	IO_L8N_CC_16 (2)	C8	
16	IO_L9P_CC_16	B7	
16	IO_L9N_CC_16 (2)	A7	
16	IO_L10P_CC_16	D5	

Table 2-4: **FF676 Package—LX30, LX50, LX85, and LX110 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
16	IO_L10N_CC_16[2]	D6	
16	IO_L11P_CC_16	C6	
16	IO_L11N_CC_16[2]	C7	
16	IO_L12P_VRN_16	A4	
16	IO_L12N_VRP_16	A5	
16	IO_L13P_16	B5	
16	IO_L13N_16	B6	
16	IO_L14P_16	D3	
16	IO_L14N_VREF_16	D4	
16	IO_L15P_16	C4	
16	IO_L15N_16	B4	
16	IO_L16P_16	C2	
16	IO_L16N_16	C3	
16	IO_L17P_16	A2	
16	IO_L17N_16	A3	
16	IO_L18P_16	D1	
16	IO_L18N_16	C1	
16	IO_L19P_16	B1	
16	IO_L19N_16	B2	
17	IO_L0P_17	T23	
17	IO_L0N_17	T22	
17	IO_L1P_17	R21	
17	IO_L1N_17	R20	
17	IO_L2P_17	T20	
17	IO_L2N_17	T19	
17	IO_L3P_17	U22	
17	IO_L3N_17	U21	
17	IO_L4P_17	W24	
17	IO_L4N_VREF_17	W23	
17	IO_L5P_17	V24	
17	IO_L5N_17	V23	
17	IO_L6P_17	AA23	
17	IO_L6N_17	AA24	

Table 2-4: **FF676 Package—LX30, LX50, LX85, and LX110 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
17	IO_L7P_17	Y23	
17	IO_L7N_17	Y22	
17	IO_L8P_CC_17	AC23	
17	IO_L8N_CC_17 (2)	AC22	
17	IO_L9P_CC_17	AB24	
17	IO_L9N_CC_17 (2)	AC24	
17	IO_L10P_CC_17	AB22	
17	IO_L10N_CC_17 (2)	AA22	
17	IO_L11P_CC_17	AC21	
17	IO_L11N_CC_17 (2)	AB21	
17	IO_L12P_VRN_17	V21	
17	IO_L12N_VRP_17	V22	
17	IO_L13P_17	W21	
17	IO_L13N_17	W20	
17	IO_L14P_17	U19	
17	IO_L14N_VREF_17	U20	
17	IO_L15P_17	V19	
17	IO_L15N_17	W19	
17	IO_L16P_17	Y21	
17	IO_L16N_17	Y20	
17	IO_L17P_17	AD19	
17	IO_L17N_17	AC19	
17	IO_L18P_17	AB20	
17	IO_L18N_17	AB19	
17	IO_L19P_17	AA20	
17	IO_L19N_17	AA19	
18	IO_L0P_18	V3	
18	IO_L0N_18	U4	
18	IO_L1P_18	T5	
18	IO_L1N_18	T4	
18	IO_L2P_18	T7	
18	IO_L2N_18	U7	
18	IO_L3P_18	U5	

Table 2-4: **FF676 Package—LX30, LX50, LX85, and LX110 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
18	IO_L3N_18	U6	
18	IO_L4P_18	V4	
18	IO_L4N_VREF_18	W4	
18	IO_L5P_18	W3	
18	IO_L5N_18	Y3	
18	IO_L6P_18	V6	
18	IO_L6N_18	V7	
18	IO_L7P_18	W5	
18	IO_L7N_18	W6	
18	IO_L8P_CC_18	Y6	
18	IO_L8N_CC_18 (2)	Y5	
18	IO_L9P_CC_18	AA4	
18	IO_L9N_CC_18 (2)	AA5	
18	IO_L10P_CC_18	Y7	
18	IO_L10N_CC_18 (2)	AA7	
18	IO_L11P_CC_18	AB4	
18	IO_L11N_CC_18 (2)	AA3	
18	IO_L12P_VRN_18	AC4	
18	IO_L12N_VRP_18	AC3	
18	IO_L13P_18	AD4	
18	IO_L13N_18	AD3	
18	IO_L14P_18	AB6	
18	IO_L14N_VREF_18	AB5	
18	IO_L15P_18	AC6	
18	IO_L15N_18	AB7	
18	IO_L16P_18	AF3	
18	IO_L16N_18	AE3	
18	IO_L17P_18	AD6	
18	IO_L17N_18	AD5	
18	IO_L18P_18	AF5	
18	IO_L18N_18	AF4	
18	IO_L19P_18	AE6	
18	IO_L19N_18	AE5	

Table 2-4: **FF676 Package—LX30, LX50, LX85, and LX110 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
21	IO_L0P_21	AD24	LX30
21	IO_L0N_21	AD23	LX30
21	IO_L1P_21	AE26	LX30
21	IO_L1N_21	AD26	LX30
21	IO_L2P_21	AF24	LX30
21	IO_L2N_21	AF25	LX30
21	IO_L3P_21	AE25	LX30
21	IO_L3N_21	AD25	LX30
21	IO_L4P_21	AF23	LX30
21	IO_L4N_VREF_21	AE23	LX30
21	IO_L5P_21	AD20	LX30
21	IO_L5N_21	AD21	LX30
21	IO_L6P_21	AE20	LX30
21	IO_L6N_21	AE21	LX30
21	IO_L7P_21	AF22	LX30
21	IO_L7N_21	AE22	LX30
21	IO_L8P_CC_21	AF18	LX30
21	IO_L8N_CC_21 (2)	AE18	LX30
21	IO_L9P_CC_21	AF19	LX30
21	IO_L9N_CC_21 (2)	AF20	LX30
21	IO_L10P_CC_21	AF17	LX30
21	IO_L10N_CC_21 (2)	AE17	LX30
21	IO_L11P_CC_21	AE16	LX30
21	IO_L11N_CC_21 (2)	AD16	LX30
21	IO_L12P_VRN_21	AF15	LX30
21	IO_L12N_VRP_21	AE15	LX30
21	IO_L13P_21	AF14	LX30
21	IO_L13N_21	AF13	LX30
21	IO_L14P_21	AF12	LX30
21	IO_L14N_VREF_21	AE13	LX30
21	IO_L15P_21	AE12	LX30
21	IO_L15N_21	AE11	LX30
21	IO_L16P_21	AF10	LX30

Table 2-4: **FF676 Package—LX30, LX50, LX85, and LX110 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
21	IO_L16N_21	AE10	LX30
21	IO_L17P_21	AF9	LX30
21	IO_L17N_21	AF8	LX30
21	IO_L18P_21	AF7	LX30
21	IO_L18N_21	AE7	LX30
21	IO_L19P_21	AE8	LX30
21	IO_L19N_21	AD9	LX30
NA	GND	A1	
NA	GND	F1	
NA	GND	L1	
NA	GND	T1	
NA	GND	AA1	
NA	GND	AF1	
NA	GND	D2	
NA	GND	P2	
NA	GND	AD2	
NA	GND	B3	
NA	GND	G3	
NA	GND	M3	
NA	GND	U3	
NA	GND	K4	
NA	GND	Y4	
NA	GND	AE4	
NA	GND	C5	
NA	GND	N5	
NA	GND	AC5	
NA	GND	A6	
NA	GND	F6	
NA	GND	T6	
NA	GND	AF6	
NA	GND	J7	
NA	GND	P7	
NA	GND	W7	

Table 2-4: **FF676 Package—LX30, LX50, LX85, and LX110 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	B8	
NA	GND	K8	
NA	GND	M8	
NA	GND	P8	
NA	GND	T8	
NA	GND	V8	
NA	GND	AB8	
NA	GND	E9	
NA	GND	J9	
NA	GND	L9	
NA	GND	N9	
NA	GND	R9	
NA	GND	U9	
NA	GND	W9	
NA	GND	AE9	
NA	GND	H10	
NA	GND	M10	
NA	GND	P10	
NA	GND	T10	
NA	GND	V10	
NA	GND	A11	
NA	GND	L11	
NA	GND	N11	
NA	GND	R11	
NA	GND	AA11	
NA	GND	AF11	
NA	GND	D12	
NA	GND	K12	
NA	GND	M12	
NA	GND	P12	
NA	GND	T12	
NA	GND	AD12	
NA	GND	B13	

Table 2-4: **FF676 Package—LX30, LX50, LX85, and LX110 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	G13	
NA	GND	J13	
NA	GND	L13	
NA	GND	U13	
NA	GND	W13	
NA	GND	K14	
NA	GND	T14	
NA	GND	V14	
NA	GND	Y14	
NA	GND	AE14	
NA	GND	C15	
NA	GND	J15	
NA	GND	L15	
NA	GND	N15	
NA	GND	R15	
NA	GND	U15	
NA	GND	W15	
NA	GND	AC15	
NA	GND	A16	
NA	GND	F16	
NA	GND	K16	
NA	GND	M16	
NA	GND	P16	
NA	GND	T16	
NA	GND	V16	
NA	GND	Y16	
NA	GND	AF16	
NA	GND	J17	
NA	GND	L17	
NA	GND	N17	
NA	GND	R17	
NA	GND	U17	
NA	GND	W17	

Table 2-4: **FF676 Package—LX30, LX50, LX85, and LX110 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	B18	
NA	GND	G18	
NA	GND	M18	
NA	GND	U18	
NA	GND	AB18	
NA	GND	E19	
NA	GND	K19	
NA	GND	R19	
NA	GND	Y19	
NA	GND	AE19	
NA	GND	H20	
NA	GND	V20	
NA	GND	A21	
NA	GND	L21	
NA	GND	AA21	
NA	GND	AF21	
NA	GND	D22	
NA	GND	P22	
NA	GND	AD22	
NA	GND	G23	
NA	GND	U23	
NA	GND	K24	
NA	GND	Y24	
NA	GND	C25	
NA	GND	N25	
NA	GND	AC25	
NA	GND	A26	
NA	GND	F26	
NA	GND	L26	
NA	GND	T26	
NA	GND	AA26	
NA	GND	AF26	
NA	VCCAUX	J8	

Table 2-4: **FF676 Package—LX30, LX50, LX85, and LX110 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	VCCAUX	L8	
NA	VCCAUX	N8	
NA	VCCAUX	R8	
NA	VCCAUX	U8	
NA	VCCAUX	W8	
NA	VCCAUX	W16	
NA	VCCAUX	K17	
NA	VCCAUX	M17	
NA	VCCAUX	P17	
NA	VCCAUX	T17	
NA	VCCAUX	V17	
NA	VCCINT	K9	
NA	VCCINT	M9	
NA	VCCINT	P9	
NA	VCCINT	T9	
NA	VCCINT	V9	
NA	VCCINT	L10	
NA	VCCINT	N10	
NA	VCCINT	R10	
NA	VCCINT	U10	
NA	VCCINT	M11	
NA	VCCINT	P11	
NA	VCCINT	T11	
NA	VCCINT	J12	
NA	VCCINT	L12	
NA	VCCINT	N12	
NA	VCCINT	R12	
NA	VCCINT	U12	
NA	VCCINT	K13	
NA	VCCINT	T13	
NA	VCCINT	V13	
NA	VCCINT	J14	
NA	VCCINT	L14	

Table 2-4: **FF676 Package—LX30, LX50, LX85, and LX110 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	VCCINT	U14	
NA	VCCINT	W14	
NA	VCCINT	H15	
NA	VCCINT	K15	
NA	VCCINT	M15	
NA	VCCINT	P15	
NA	VCCINT	T15	
NA	VCCINT	V15	
NA	VCCINT	Y15	
NA	VCCINT	J16	
NA	VCCINT	L16	
NA	VCCINT	N16	
NA	VCCINT	U16	
NA	VCCINT	R16	
0	VCCO_0	Y9	
0	VCCO_0	W12	
1	VCCO_1	C10	
1	VCCO_1	F11	
2	VCCO_2	AA16	
2	VCCO_2	AD17	
3	VCCO_3	E14	
3	VCCO_3	D17	
4	VCCO_4	AC10	
4	VCCO_4	AB13	
11	VCCO_11	F21	
11	VCCO_11	J22	
11	VCCO_11	H25	
12	VCCO_12	J2	
12	VCCO_12	H5	
12	VCCO_12	L6	
13	VCCO_13	N20	
13	VCCO_13	M23	
13	VCCO_13	R24	

Table 2-4: **FF676 Package—LX30, LX50, LX85, and LX110 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
14	VCCO_14	W2	
14	VCCO_14	R4	
14	VCCO_14	V5	
15	VCCO_15	C20	
15	VCCO_15	B23	
15	VCCO_15	E24	
16	VCCO_16	E4	
16	VCCO_16	D7	
16	VCCO_16	G8	
17	VCCO_17	T21	
17	VCCO_17	W22	
17	VCCO_17	V25	
18	VCCO_18	AB3	
18	VCCO_18	AA6	
18	VCCO_18	AD7	
21	VCCO_21	AC20	
21	VCCO_21	AB23	
21	VCCO_21	AE24	

Notes:

1. Do not connect a single ended clock to the N-side of the differential clock pair of pins, for example, IO_L3N_GC_3.
2. Do not connect a single-ended clock to the N-side of clock capable pins, for example, IO_L8N_CC_11.
3. RSVD pins must be tied to GND (logic 0).

FF1136 Package—LX50T, FX70T, LX85T, LX110T, LX155T, SX50T, SX95T, and FX100T

Table 2-5: **FF1136 Package—LX50T, FX70T, LX85T, LX110T, LX155T, SX50T, SX95T and FX100T**

Bank	Pin Description	Pin Number	No Connect (NC)
0	DXP_0	W18	
0	DXN_0	W17	
0	AVDD_0	T18	
0	AVSS_0	T17	
0	VP_0	U18	
0	VN_0	V17	
0	VREFP_0	V18	
0	VREFN_0	U17	
0	VBATT_0	L23	
0	PROGRAM_B_0	M22	
0	HSWAPEN_0	M23	
0	D_IN_0	P15	
0	DONE_0	M15	
0	CCLK_0	N15	
0	INIT_B_0	N14	
0	CS_B_0	N22	
0	RDWR_B_0	N23	
0	RSVD(3)	AB23	
0	RSVD(3)	AC23	
0	TCK_0	AB15	
0	M0_0	AD21	
0	M2_0	AD22	
0	M1_0	AC22	
0	TMS_0	AC14	
0	TDI_0	AC15	
0	D_OUT_BUSY_0	AD15	
0	TDO_0	AD14	
1	IO_L0P_A19_1	L21	
1	IO_L0N_A18_1	L20	
1	IO_L1P_A17_1	L15	

Table 2-5: **FF1136 Package—LX50T, FX70T, LX85T, LX110T, LX155T, SX50T, SX95T and FX100T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
1	IO_L1N_A16_1	L16	
1	IO_L2P_A15_D31_1	J22	
1	IO_L2N_A14_D30_1	K21	
1	IO_L3P_A13_D29_1	K16	
1	IO_L3N_A12_D28_1	J15	
1	IO_L4P_A11_D27_1	G22	
1	IO_L4N_VREF_A10_D26_1	H22	
1	IO_L5P_A9_D25_1	L14	
1	IO_L5N_A8_D24_1	K14	
1	IO_L6P_A7_D23_1	K23	
1	IO_L6N_A6_D22_1	K22	
1	IO_L7P_A5_D21_1	J12	
1	IO_L7N_A4_D20_1	H12	
1	IO_L8P_CC_A3_D19_1	G23	
1	IO_L8N_CC_A2_D18_1 (2)	H23	
1	IO_L9P_CC_A1_D17_1	K13	
1	IO_L9N_CC_A0_D16_1 (2)	K12	
2	IO_L0P_CC_RS1_2	AE13	
2	IO_L0N_CC_RS0_2 (2)	AE12	
2	IO_L1P_CC_A25_2	AF23	
2	IO_L1N_CC_A24_2 (2)	AG23	
2	IO_L2P_A23_2	AF13	
2	IO_L2N_A22_2	AG12	
2	IO_L3P_A21_2	AE22	
2	IO_L3N_A20_2	AE23	
2	IO_L4P_FCS_B_2	AE14	
2	IO_L4N_VREF_FOE_B_MOSI_2	AF14	
2	IO_L5P_FWE_B_2	AF20	
2	IO_L5N_CSO_B_2	AF21	
2	IO_L6P_D7_2	AF15	
2	IO_L6N_D6_2	AE16	
2	IO_L7P_D5_2	AE21	

Table 2-5: **FF1136 Package—LX50T, FX70T, LX85T, LX110T, LX155T, SX50T, SX95T and FX100T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
2	IO_L7N_D4_2	AD20	
2	IO_L8P_D3_2	AF16	
2	IO_L8N_D2_FS2_2	AE17	
2	IO_L9P_D1_FS1_2	AE19	
2	IO_L9N_D0_FS0_2	AD19	
3	IO_L0P_CC_GC_3	H17	
3	IO_L0N_CC_GC_3 (1)(2)	H18	
3	IO_L1P_CC_GC_3	K17	
3	IO_L1N_CC_GC_3 (1)(2)	L18	
3	IO_L2P_GC_VRN_3	G15	
3	IO_L2N_GC_VRP_3 (1)	G16	
3	IO_L3P_GC_3	K18	
3	IO_L3N_GC_3 (1)	J19	
3	IO_L4P_GC_3	J16	
3	IO_L4N_GC_VREF_3 (1)	J17	
3	IO_L5P_GC_3	L19	
3	IO_L5N_GC_3 (1)	K19	
3	IO_L6P_GC_3	H14	
3	IO_L6N_GC_3 (1)	H15	
3	IO_L7P_GC_3	J20	
3	IO_L7N_GC_3 (1)	J21	
3	IO_L8P_GC_3	J14	
3	IO_L8N_GC_3 (1)	H13	
3	IO_L9P_GC_3	H19	
3	IO_L9N_GC_3 (1)	H20	
4	IO_L0P_GC_D15_4	AG22	
4	IO_L0N_GC_D14_4 (1)	AH22	
4	IO_L1P_GC_D13_4	AH12	
4	IO_L1N_GC_D12_4 (1)	AG13	
4	IO_L2P_GC_D11_4	AH20	
4	IO_L2N_GC_D10_4 (1)	AH19	
4	IO_L3P_GC_D9_4	AH14	

Table 2-5: **FF1136 Package—LX50T, FX70T, LX85T, LX110T, LX155T, SX50T, SX95T and FX100T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
4	IO_L3N_GC_D8_4 (1)	AH13	
4	IO_L4P_GC_4	AG21	
4	IO_L4N_GC_VREF_4 (1)	AG20	
4	IO_L5P_GC_4	AH15	
4	IO_L5N_GC_4 (1)	AG15	
4	IO_L6P_GC_4	AG18	
4	IO_L6N_GC_4 (1)	AF19	
4	IO_L7P_GC_VRN_4	AH17	
4	IO_L7N_GC_VRP_4 (1)	AG16	
4	IO_L8P_CC_GC_4	AF18	
4	IO_L8N_CC_GC_4 (1)(2)	AE18	
4	IO_L9P_CC_GC_4	AH18	
4	IO_L9N_CC_GC_4 (1)(2)	AG17	
5	IO_L0P_5	B16	LX50T, LX85T, SX50T
5	IO_L0N_5	B15	LX50T, LX85T, SX50T
5	IO_L1P_5	A15	LX50T, LX85T, SX50T
5	IO_L1N_5	A14	LX50T, LX85T, SX50T
5	IO_L2P_5	B17	LX50T, LX85T, SX50T
5	IO_L2N_5	A16	LX50T, LX85T, SX50T
5	IO_L3P_5	C14	LX50T, LX85T, SX50T
5	IO_L3N_5	C15	LX50T, LX85T, SX50T
5	IO_L4P_5	E19	LX50T, LX85T, SX50T
5	IO_L4N_VREF_5	F19	LX50T, LX85T, SX50T
5	IO_L5P_5	C17	LX50T, LX85T, SX50T
5	IO_L5N_5	D17	LX50T, LX85T, SX50T
5	IO_L6P_5	E21	LX50T, LX85T, SX50T
5	IO_L6N_5	D20	LX50T, LX85T, SX50T
5	IO_L7P_5	D16	LX50T, LX85T, SX50T
5	IO_L7N_5	D15	LX50T, LX85T, SX50T
5	IO_L8P_CC_5	G20	LX50T, LX85T, SX50T
5	IO_L8N_CC_5 (2)	F20	LX50T, LX85T, SX50T
5	IO_L9P_CC_5	D14	LX50T, LX85T, SX50T

Table 2-5: **FF1136 Package—LX50T, FX70T, LX85T, LX110T, LX155T, SX50T, SX95T and FX100T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
5	IO_L9N_CC_5 (2)	E14	LX50T, LX85T, SX50T
5	IO_L10P_CC_5	E17	LX50T, LX85T, SX50T
5	IO_L10N_CC_5 (2)	E16	LX50T, LX85T, SX50T
5	IO_L11P_CC_5	F21	LX50T, LX85T, SX50T
5	IO_L11N_CC_5 (2)	G21	LX50T, LX85T, SX50T
5	IO_L12P_VRN_5	E18	LX50T, LX85T, SX50T
5	IO_L12N_VRP_5	D19	LX50T, LX85T, SX50T
5	IO_L13P_5	D21	LX50T, LX85T, SX50T
5	IO_L13N_5	D22	LX50T, LX85T, SX50T
5	IO_L14P_5	F18	LX50T, LX85T, SX50T
5	IO_L14N_VREF_5	G18	LX50T, LX85T, SX50T
5	IO_L15P_5	E22	LX50T, LX85T, SX50T
5	IO_L15N_5	F23	LX50T, LX85T, SX50T
5	IO_L16P_5	G17	LX50T, LX85T, SX50T
5	IO_L16N_5	F16	LX50T, LX85T, SX50T
5	IO_L17P_5	D24	LX50T, LX85T, SX50T
5	IO_L17N_5	E23	LX50T, LX85T, SX50T
5	IO_L18P_5	F14	LX50T, LX85T, SX50T
5	IO_L18N_5	F15	LX50T, LX85T, SX50T
5	IO_L19P_5	F24	LX50T, LX85T, SX50T
5	IO_L19N_5	E24	LX50T, LX85T, SX50T
6	IO_L0P_6	AH24	LX50T, LX85T, SX50T
6	IO_L0N_6	AJ24	LX50T, LX85T, SX50T
6	IO_L1P_6	AK12	LX50T, LX85T, SX50T
6	IO_L1N_6	AJ12	LX50T, LX85T, SX50T
6	IO_L2P_6	AH23	LX50T, LX85T, SX50T
6	IO_L2N_6	AJ22	LX50T, LX85T, SX50T
6	IO_L3P_6	AL13	LX50T, LX85T, SX50T
6	IO_L3N_6	AK13	LX50T, LX85T, SX50T
6	IO_L4P_6	AK24	LX50T, LX85T, SX50T
6	IO_L4N_VREF_6	AL23	LX50T, LX85T, SX50T
6	IO_L5P_6	AJ14	LX50T, LX85T, SX50T

Table 2-5: **FF1136 Package—LX50T, FX70T, LX85T, LX110T, LX155T, SX50T, SX95T and FX100T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
6	IO_L5N_6	AK14	LX50T, LX85T, SX50T
6	IO_L6P_6	AK23	LX50T, LX85T, SX50T
6	IO_L6N_6	AK22	LX50T, LX85T, SX50T
6	IO_L7P_6	AL15	LX50T, LX85T, SX50T
6	IO_L7N_6	AL14	LX50T, LX85T, SX50T
6	IO_L8P_CC_6	AJ21	LX50T, LX85T, SX50T
6	IO_L8N_CC_6 (2)	AJ20	LX50T, LX85T, SX50T
6	IO_L9P_CC_6	AJ16	LX50T, LX85T, SX50T
6	IO_L9N_CC_6 (2)	AJ15	LX50T, LX85T, SX50T
6	IO_L10P_CC_6	AK16	LX50T, LX85T, SX50T
6	IO_L10N_CC_6 (2)	AL16	LX50T, LX85T, SX50T
6	IO_L11P_CC_6	AL21	LX50T, LX85T, SX50T
6	IO_L11N_CC_6 (2)	AK21	LX50T, LX85T, SX50T
6	IO_L12P_VRN_6	AK17	LX50T, LX85T, SX50T
6	IO_L12N_VRP_6	AJ17	LX50T, LX85T, SX50T
6	IO_L13P_6	AL19	LX50T, LX85T, SX50T
6	IO_L13N_6	AL20	LX50T, LX85T, SX50T
6	IO_L14P_6	AK18	LX50T, LX85T, SX50T
6	IO_L14N_VREF_6	AL18	LX50T, LX85T, SX50T
6	IO_L15P_6	AJ19	LX50T, LX85T, SX50T
6	IO_L15N_6	AK19	LX50T, LX85T, SX50T
6	IO_L16P_6	AM15	LX50T, LX85T, SX50T
6	IO_L16N_6	AM16	LX50T, LX85T, SX50T
6	IO_L17P_6	AP16	LX50T, LX85T, SX50T
6	IO_L17N_6	AP17	LX50T, LX85T, SX50T
6	IO_L18P_6	AN15	LX50T, LX85T, SX50T
6	IO_L18N_6	AP15	LX50T, LX85T, SX50T
6	IO_L19P_6	AM17	LX50T, LX85T, SX50T
6	IO_L19N_6	AN17	LX50T, LX85T, SX50T
11	IO_L0P_11	B32	
11	IO_L0N_11	A33	
11	IO_L1P_11	B33	

Table 2-5: **FF1136 Package—LX50T, FX70T, LX85T, LX110T, LX155T, SX50T, SX95T and FX100T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
11	IO_L1N_11	C33	
11	IO_L2P_11	C32	
11	IO_L2N_11	D32	
11	IO_L3P_11	C34	
11	IO_L3N_11	D34	
11	IO_L4P_11	G32	
11	IO_L4N_VREF_11	H32	
11	IO_L5P_11	F33	
11	IO_L5N_11	E34	
11	IO_L6P_11	E32	
11	IO_L6N_11	E33	
11	IO_L7P_11	G33	
11	IO_L7N_11	F34	
11	IO_L8P_CC_11	J32	
11	IO_L8N_CC_11 (2)	H33	
11	IO_L9P_CC_11	H34	
11	IO_L9N_CC_11 (2)	J34	
11	IO_L10P_CC_SM15P_11	L34	
11	IO_L10N_CC_SM15N_11 (2)	K34	
11	IO_L11P_CC_SM14P_11	K33	
11	IO_L11N_CC_SM14N_11 (2)	K32	
11	IO_L12P_VRN_11	N33	
11	IO_L12N_VRP_11	M33	
11	IO_L13P_11	L33	
11	IO_L13N_11	M32	
11	IO_L14P_11	P34	
11	IO_L14N_VREF_11	N34	
11	IO_L15P_SM13P_11	P32	
11	IO_L15N_SM13N_11	N32	
11	IO_L16P_SM12P_11	T33	
11	IO_L16N_SM12N_11	R34	
11	IO_L17P_SM11P_11	R33	

Table 2-5: **FF1136 Package—LX50T, FX70T, LX85T, LX110T, LX155T, SX50T, SX95T and FX100T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
11	IO_L17N_SM11N_11	R32	
11	IO_L18P_SM10P_11	U33	
11	IO_L18N_SM10N_11	T34	
11	IO_L19P_SM9P_11	U32	
11	IO_L19N_SM9N_11	U31	
12	IO_L0P_12	M6	
12	IO_L0N_12	M5	
12	IO_L1P_12	N8	
12	IO_L1N_12	N7	
12	IO_L2P_12	M7	
12	IO_L2N_12	L6	
12	IO_L3P_12	N5	
12	IO_L3N_12	P5	
12	IO_L4P_12	L4	
12	IO_L4N_VREF_12	L5	
12	IO_L5P_12	P7	
12	IO_L5N_12	P6	
12	IO_L6P_12	K7	
12	IO_L6N_12	K6	
12	IO_L7P_12	R6	
12	IO_L7N_12	T6	
12	IO_L8P_CC_12	J6	
12	IO_L8N_CC_12 (2)	J5	
12	IO_L9P_CC_12	R7	
12	IO_L9N_CC_12 (2)	R8	
12	IO_L10P_CC_12	T8	
12	IO_L10N_CC_12 (2)	U7	
12	IO_L11P_CC_12	H7	
12	IO_L11N_CC_12 (2)	J7	
12	IO_L12P_VRN_12	R9	
12	IO_L12N_VRP_12	P9	
12	IO_L13P_12	H5	

Table 2-5: **FF1136 Package—LX50T, FX70T, LX85T, LX110T, LX155T, SX50T, SX95T and FX100T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
12	IO_L13N_12	G5	
12	IO_L14P_12	R11	
12	IO_L14N_VREF_12	P10	
12	IO_L15P_12	F5	
12	IO_L15N_12	F6	
12	IO_L16P_12	T10	
12	IO_L16N_12	T11	
12	IO_L17P_12	G6	
12	IO_L17N_12	G7	
12	IO_L18P_12	T9	
12	IO_L18N_12	U10	
12	IO_L19P_12	E6	
12	IO_L19N_12	E7	
13	IO_L0P_SM8P_13	V32	
13	IO_L0N_SM8N_13	V33	
13	IO_L1P_SM7P_13	W34	
13	IO_L1N_SM7N_13	V34	
13	IO_L2P_SM6P_13	Y33	
13	IO_L2N_SM6N_13	AA33	
13	IO_L3P_SM5P_13	AA34	
13	IO_L3N_SM5N_13	Y34	
13	IO_L4P_13	Y32	
13	IO_L4N_VREF_13	W32	
13	IO_L5P_SM4P_13	AC34	
13	IO_L5N_SM4N_13	AD34	
13	IO_L6P_SM3P_13	AC32	
13	IO_L6N_SM3N_13	AB32	
13	IO_L7P_SM2P_13	AC33	
13	IO_L7N_SM2N_13	AB33	
13	IO_L8P_CC_SM1P_13	AF33	
13	IO_L8N_CC_SM1N_13 (2)	AE33	
13	IO_L9P_CC_SM0P_13	AF34	

Table 2-5: **FF1136 Package—LX50T, FX70T, LX85T, LX110T, LX155T, SX50T, SX95T and FX100T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
13	IO_L9N_CC_SM0N_13 (2)	AE34	
13	IO_L10P_CC_13	AH34	
13	IO_L10N_CC_13 (2)	AJ34	
13	IO_L11P_CC_13	AD32	
13	IO_L11N_CC_13 (2)	AE32	
13	IO_L12P_VRN_13	AG33	
13	IO_L12N_VRP_13	AH33	
13	IO_L13P_13	AK34	
13	IO_L13N_13	AK33	
13	IO_L14P_13	AG32	
13	IO_L14N_VREF_13	AH32	
13	IO_L15P_13	AJ32	
13	IO_L15N_13	AK32	
13	IO_L16P_13	AL34	
13	IO_L16N_13	AL33	
13	IO_L17P_13	AM33	
13	IO_L17N_13	AM32	
13	IO_L18P_13	AN34	
13	IO_L18N_13	AN33	
13	IO_L19P_13	AN32	
13	IO_L19N_13	AP32	
15	IO_L0P_15	E29	
15	IO_L0N_15	F29	
15	IO_L1P_15	G30	
15	IO_L1N_15	F30	
15	IO_L2P_15	H29	
15	IO_L2N_15	J29	
15	IO_L3P_15	F31	
15	IO_L3N_15	E31	
15	IO_L4P_15	L29	
15	IO_L4N_VREF_15	K29	
15	IO_L5P_15	H30	

Table 2-5: **FF1136 Package—LX50T, FX70T, LX85T, LX110T, LX155T, SX50T, SX95T and FX100T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
15	IO_L5N_15	G31	
15	IO_L6P_15	J30	
15	IO_L6N_15	J31	
15	IO_L7P_15	L30	
15	IO_L7N_15	M30	
15	IO_L8P_CC_15	N29	
15	IO_L8N_CC_15 (2)	P29	
15	IO_L9P_CC_15	K31	
15	IO_L9N_CC_15 (2)	L31	
15	IO_L10P_CC_15	P31	
15	IO_L10N_CC_15 (2)	P30	
15	IO_L11P_CC_15	M31	
15	IO_L11N_CC_15 (2)	N30	
15	IO_L12P_VRN_15	R28	
15	IO_L12N_VRP_15	R29	
15	IO_L13P_15	T31	
15	IO_L13N_15	R31	
15	IO_L14P_15	U30	
15	IO_L14N_VREF_15	T30	
15	IO_L15P_15	T28	
15	IO_L15N_15	T29	
15	IO_L16P_15	U27	
15	IO_L16N_15	U28	
15	IO_L17P_15	R26	
15	IO_L17N_15	R27	
15	IO_L18P_15	U26	
15	IO_L18N_15	T26	
15	IO_L19P_15	U25	
15	IO_L19N_15	T25	
17	IO_L0P_17	W24	
17	IO_L0N_17	V24	
17	IO_L1P_17	Y26	

Table 2-5: **FF1136 Package—LX50T, FX70T, LX85T, LX110T, LX155T, SX50T, SX95T and FX100T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
17	IO_L1N_17	W26	
17	IO_L2P_17	V25	
17	IO_L2N_17	W25	
17	IO_L3P_17	Y27	
17	IO_L3N_17	W27	
17	IO_L4P_17	V30	
17	IO_L4N_VREF_17	W30	
17	IO_L5P_17	V28	
17	IO_L5N_17	V27	
17	IO_L6P_17	W31	
17	IO_L6N_17	Y31	
17	IO_L7P_17	W29	
17	IO_L7N_17	V29	
17	IO_L8P_CC_17	Y28	
17	IO_L8N_CC_17 (2)	Y29	
17	IO_L9P_CC_17	AB31	
17	IO_L9N_CC_17 (2)	AA31	
17	IO_L10P_CC_17	AB30	
17	IO_L10N_CC_17 (2)	AC30	
17	IO_L11P_CC_17	AA29	
17	IO_L11N_CC_17 (2)	AA30	
17	IO_L12P_VRN_17	AD31	
17	IO_L12N_VRP_17	AE31	
17	IO_L13P_17	AD30	
17	IO_L13N_17	AC29	
17	IO_L14P_17	AF31	
17	IO_L14N_VREF_17	AG31	
17	IO_L15P_17	AE29	
17	IO_L15N_17	AD29	
17	IO_L16P_17	AJ31	
17	IO_L16N_17	AK31	
17	IO_L17P_17	AF29	

Table 2-5: **FF1136 Package—LX50T, FX70T, LX85T, LX110T, LX155T, SX50T, SX95T and FX100T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
17	IO_L17N_17	AF30	
17	IO_L18P_17	AJ30	
17	IO_L18N_17	AH30	
17	IO_L19P_17	AH29	
17	IO_L19N_17	AG30	
18	IO_L0P_18	AC4	
18	IO_L0N_18	AC5	
18	IO_L1P_18	AB6	
18	IO_L1N_18	AB7	
18	IO_L2P_18	AA5	
18	IO_L2N_18	AB5	
18	IO_L3P_18	AC7	
18	IO_L3N_18	AD7	
18	IO_L4P_18	Y8	
18	IO_L4N_VREF_18	Y9	
18	IO_L5P_18	AD4	
18	IO_L5N_18	AD5	
18	IO_L6P_18	AA6	
18	IO_L6N_18	Y7	
18	IO_L7P_18	AD6	
18	IO_L7N_18	AE6	
18	IO_L8P_CC_18	W6	
18	IO_L8N_CC_18 (2)	Y6	
18	IO_L9P_CC_18	AE7	
18	IO_L9N_CC_18 (2)	AF6	
18	IO_L10P_CC_18	AG5	
18	IO_L10N_CC_18 (2)	AF5	
18	IO_L11P_CC_18	W7	
18	IO_L11N_CC_18 (2)	V7	
18	IO_L12P_VRN_18	AH5	
18	IO_L12N_VRP_18	AG6	
18	IO_L13P_18	Y11	

Table 2-5: **FF1136 Package—LX50T, FX70T, LX85T, LX110T, LX155T, SX50T, SX95T and FX100T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
18	IO_L13N_18	W11	
18	IO_L14P_18	AH7	
18	IO_L14N_VREF_18	AG7	
18	IO_L15P_18	W10	
18	IO_L15N_18	W9	
18	IO_L16P_18	AJ7	
18	IO_L16N_18	AJ6	
18	IO_L17P_18	V8	
18	IO_L17N_18	U8	
18	IO_L18P_18	AK7	
18	IO_L18N_18	AK6	
18	IO_L19P_18	V10	
18	IO_L19N_18	V9	
19	IO_L0P_19	K24	
19	IO_L0N_19	L24	
19	IO_L1P_19	L25	
19	IO_L1N_19	L26	
19	IO_L2P_19	J24	
19	IO_L2N_19	J25	
19	IO_L3P_19	M25	
19	IO_L3N_19	M26	
19	IO_L4P_19	J27	
19	IO_L4N_VREF_19	J26	
19	IO_L5P_19	G25	
19	IO_L5N_19	G26	
19	IO_L6P_19	H25	
19	IO_L6N_19	H24	
19	IO_L7P_19	F25	
19	IO_L7N_19	F26	
19	IO_L8P_CC_19	G27	
19	IO_L8N_CC_19 (2)	H27	
19	IO_L9P_CC_19	H28	

Table 2-5: **FF1136 Package—LX50T, FX70T, LX85T, LX110T, LX155T, SX50T, SX95T and FX100T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
19	IO_L9N_CC_19(2)	G28	
19	IO_L10P_CC_19	E28	
19	IO_L10N_CC_19(2)	F28	
19	IO_L11P_CC_19	E26	
19	IO_L11N_CC_19(2)	E27	
19	IO_L12P_VRN_19	N27	
19	IO_L12N_VRP_19	M27	
19	IO_L13P_19	K28	
19	IO_L13N_19	L28	
19	IO_L14P_19	K27	
19	IO_L14N_VREF_19	K26	
19	IO_L15P_19	M28	
19	IO_L15N_19	N28	
19	IO_L16P_19	P26	
19	IO_L16N_19	P27	
19	IO_L17P_19	N24	
19	IO_L17N_19	P24	
19	IO_L18P_19	P25	
19	IO_L18N_19	N25	
19	IO_L19P_19	R24	
19	IO_L19N_19	T24	
20	IO_L0P_20	E9	
20	IO_L0N_20	E8	
20	IO_L1P_20	F9	
20	IO_L1N_20	F8	
20	IO_L2P_20	F10	
20	IO_L2N_20	G10	
20	IO_L3P_20	G8	
20	IO_L3N_20	H8	
20	IO_L4P_20	D11	
20	IO_L4N_VREF_20	D10	
20	IO_L5P_20	K11	

Table 2-5: **FF1136 Package—LX50T, FX70T, LX85T, LX110T, LX155T, SX50T, SX95T and FX100T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
20	IO_L5N_20	J11	
20	IO_L6P_20	D12	
20	IO_L6N_20	C12	
20	IO_L7P_20	H10	
20	IO_L7N_20	H9	
20	IO_L8P_CC_20	A13	
20	IO_L8N_CC_20(2)	B12	
20	IO_L9P_CC_20	J10	
20	IO_L9N_CC_20(2)	J9	
20	IO_L10P_CC_20	K8	
20	IO_L10N_CC_20(2)	K9	
20	IO_L11P_CC_20	B13	
20	IO_L11N_CC_20(2)	C13	
20	IO_L12P_VRN_20	L10	
20	IO_L12N_VRP_20	L11	
20	IO_L13P_20	G11	
20	IO_L13N_20	G12	
20	IO_L14P_20	M8	
20	IO_L14N_VREF_20	L8	
20	IO_L15P_20	F11	
20	IO_L15N_20	E11	
20	IO_L16P_20	M10	
20	IO_L16N_20	L9	
20	IO_L17P_20	E12	
20	IO_L17N_20	E13	
20	IO_L18P_20	N10	
20	IO_L18N_20	N9	
20	IO_L19P_20	F13	
20	IO_L19N_20	G13	
21	IO_L0P_21	AA25	
21	IO_L0N_21	AA26	
21	IO_L1P_21	AB27	

Table 2-5: **FF1136 Package—LX50T, FX70T, LX85T, LX110T, LX155T, SX50T, SX95T and FX100T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
21	IO_L1N_21	AC27	
21	IO_L2P_21	Y24	
21	IO_L2N_21	AA24	
21	IO_L3P_21	AB25	
21	IO_L3N_21	AB26	
21	IO_L4P_21	AC28	
21	IO_L4N_VREF_21	AD27	
21	IO_L5P_21	AB28	
21	IO_L5N_21	AA28	
21	IO_L6P_21	AG28	
21	IO_L6N_21	AH28	
21	IO_L7P_21	AE28	
21	IO_L7N_21	AF28	
21	IO_L8P_CC_21	AK26	
21	IO_L8N_CC_21 (2)	AJ27	
21	IO_L9P_CC_21	AK29	
21	IO_L9N_CC_21 (2)	AJ29	
21	IO_L10P_CC_21	AK28	
21	IO_L10N_CC_21 (2)	AK27	
21	IO_L11P_CC_21	AH27	
21	IO_L11N_CC_21 (2)	AJ26	
21	IO_L12P_VRN_21	AJ25	
21	IO_L12N_VRP_21	AH25	
21	IO_L13P_21	AF24	
21	IO_L13N_21	AG25	
21	IO_L14P_21	AG27	
21	IO_L14N_VREF_21	AG26	
21	IO_L15P_21	AF25	
21	IO_L15N_21	AF26	
21	IO_L16P_21	AE27	
21	IO_L16N_21	AE26	
21	IO_L17P_21	AC25	

Table 2-5: **FF1136 Package—LX50T, FX70T, LX85T, LX110T, LX155T, SX50T, SX95T and FX100T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
21	IO_L17N_21	AC24	
21	IO_L18P_21	AD26	
21	IO_L18N_21	AD25	
21	IO_L19P_21	AD24	
21	IO_L19N_21	AE24	
22	IO_L0P_22	AN14	
22	IO_L0N_22	AP14	
22	IO_L1P_22	AB10	
22	IO_L1N_22	AA10	
22	IO_L2P_22	AN13	
22	IO_L2N_22	AM13	
22	IO_L3P_22	AA8	
22	IO_L3N_22	AA9	
22	IO_L4P_22	AP12	
22	IO_L4N_VREF_22	AN12	
22	IO_L5P_22	AC8	
22	IO_L5N_22	AB8	
22	IO_L6P_22	AM12	
22	IO_L6N_22	AM11	
22	IO_L7P_22	AC10	
22	IO_L7N_22	AC9	
22	IO_L8P_CC_22	AL11	
22	IO_L8N_CC_22 (2)	AL10	
22	IO_L9P_CC_22	AE8	
22	IO_L9N_CC_22 (2)	AD9	
22	IO_L10P_CC_22	AD10	
22	IO_L10N_CC_22 (2)	AD11	
22	IO_L11P_CC_22	AK11	
22	IO_L11N_CC_22 (2)	AJ11	
22	IO_L12P_VRN_22	AF8	
22	IO_L12N_VRP_22	AE9	
22	IO_L13P_22	AK8	

Table 2-5: **FF1136 Package—LX50T, FX70T, LX85T, LX110T, LX155T, SX50T, SX95T and FX100T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
22	IO_L13N_22	AK9	
22	IO_L14P_22	AF9	
22	IO_L14N_VREF_22	AF10	
22	IO_L15P_22	AJ9	
22	IO_L15N_22	AJ10	
22	IO_L16P_22	AF11	
22	IO_L16N_22	AE11	
22	IO_L17P_22	AH9	
22	IO_L17N_22	AH10	
22	IO_L18P_22	AG8	
22	IO_L18N_22	AH8	
22	IO_L19P_22	AG10	
22	IO_L19N_22	AG11	
23	IO_L0P_23	C20	LX50T, LX85T, SX50T
23	IO_L0N_23	B20	LX50T, LX85T, SX50T
23	IO_L1P_23	B21	LX50T, LX85T, SX50T
23	IO_L1N_23	A21	LX50T, LX85T, SX50T
23	IO_L2P_23	C19	LX50T, LX85T, SX50T
23	IO_L2N_23	C18	LX50T, LX85T, SX50T
23	IO_L3P_23	C22	LX50T, LX85T, SX50T
23	IO_L3N_23	B22	LX50T, LX85T, SX50T
23	IO_L4P_23	B18	LX50T, LX85T, SX50T
23	IO_L4N_VREF_23	A18	LX50T, LX85T, SX50T
23	IO_L5P_23	C23	LX50T, LX85T, SX50T
23	IO_L5N_23	B23	LX50T, LX85T, SX50T
23	IO_L6P_23	A19	LX50T, LX85T, SX50T
23	IO_L6N_23	A20	LX50T, LX85T, SX50T
23	IO_L7P_23	A23	LX50T, LX85T, SX50T
23	IO_L7N_23	A24	LX50T, LX85T, SX50T
23	IO_L8P_CC_23	C24	LX50T, LX85T, SX50T
23	IO_L8N_CC_23 (2)	D25	LX50T, LX85T, SX50T
23	IO_L9P_CC_23	B26	LX50T, LX85T, SX50T

Table 2-5: **FF1136 Package—LX50T, FX70T, LX85T, LX110T, LX155T, SX50T, SX95T and FX100T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
23	IO_L9N_CC_23 (2)	A25	LX50T, LX85T, SX50T
23	IO_L10P_CC_23	B27	LX50T, LX85T, SX50T
23	IO_L10N_CC_23 (2)	A26	LX50T, LX85T, SX50T
23	IO_L11P_CC_23	B25	LX50T, LX85T, SX50T
23	IO_L11N_CC_23 (2)	C25	LX50T, LX85T, SX50T
23	IO_L12P_VRN_23	C29	LX50T, LX85T, SX50T
23	IO_L12N_VRP_23	B28	LX50T, LX85T, SX50T
23	IO_L13P_23	D26	LX50T, LX85T, SX50T
23	IO_L13N_23	C27	LX50T, LX85T, SX50T
23	IO_L14P_23	A29	LX50T, LX85T, SX50T
23	IO_L14N_VREF_23	A28	LX50T, LX85T, SX50T
23	IO_L15P_23	C28	LX50T, LX85T, SX50T
23	IO_L15N_23	D27	LX50T, LX85T, SX50T
23	IO_L16P_23	B31	LX50T, LX85T, SX50T
23	IO_L16N_23	A31	LX50T, LX85T, SX50T
23	IO_L17P_23	C30	LX50T, LX85T, SX50T
23	IO_L17N_23	D29	LX50T, LX85T, SX50T
23	IO_L18P_23	D31	LX50T, LX85T, SX50T
23	IO_L18N_23	D30	LX50T, LX85T, SX50T
23	IO_L19P_23	A30	LX50T, LX85T, SX50T
23	IO_L19N_23	B30	LX50T, LX85T, SX50T
25	IO_L0P_25	AL29	LX50T, LX85T, SX50T
25	IO_L0N_25	AL30	LX50T, LX85T, SX50T
25	IO_L1P_25	AM31	LX50T, LX85T, SX50T
25	IO_L1N_25	AL31	LX50T, LX85T, SX50T
25	IO_L2P_25	AN30	LX50T, LX85T, SX50T
25	IO_L2N_25	AM30	LX50T, LX85T, SX50T
25	IO_L3P_25	AP30	LX50T, LX85T, SX50T
25	IO_L3N_25	AP31	LX50T, LX85T, SX50T
25	IO_L4P_25	AM27	LX50T, LX85T, SX50T
25	IO_L4N_VREF_25	AL28	LX50T, LX85T, SX50T
25	IO_L5P_25	AP29	LX50T, LX85T, SX50T

Table 2-5: **FF1136 Package—LX50T, FX70T, LX85T, LX110T, LX155T, SX50T, SX95T and FX100T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
25	IO_L5N_25	AN29	LX50T, LX85T, SX50T
25	IO_L6P_25	AP27	LX50T, LX85T, SX50T
25	IO_L6N_25	AN27	LX50T, LX85T, SX50T
25	IO_L7P_25	AN28	LX50T, LX85T, SX50T
25	IO_L7N_25	AM28	LX50T, LX85T, SX50T
25	IO_L8P_CC_25	AN25	LX50T, LX85T, SX50T
25	IO_L8N_CC_25 (2)	AM25	LX50T, LX85T, SX50T
25	IO_L9P_CC_25	AM26	LX50T, LX85T, SX50T
25	IO_L9N_CC_25 (2)	AL26	LX50T, LX85T, SX50T
25	IO_L10P_CC_25	AP26	LX50T, LX85T, SX50T
25	IO_L10N_CC_25 (2)	AP25	LX50T, LX85T, SX50T
25	IO_L11P_CC_25	AL25	LX50T, LX85T, SX50T
25	IO_L11N_CC_25 (2)	AL24	LX50T, LX85T, SX50T
25	IO_L12P_VRN_25	AN24	LX50T, LX85T, SX50T
25	IO_L12N_VRP_25	AP24	LX50T, LX85T, SX50T
25	IO_L13P_25	AM21	LX50T, LX85T, SX50T
25	IO_L13N_25	AM20	LX50T, LX85T, SX50T
25	IO_L14P_25	AN23	LX50T, LX85T, SX50T
25	IO_L14N_VREF_25	AM23	LX50T, LX85T, SX50T
25	IO_L15P_25	AN20	LX50T, LX85T, SX50T
25	IO_L15N_25	AP20	LX50T, LX85T, SX50T
25	IO_L16P_25	AN22	LX50T, LX85T, SX50T
25	IO_L16N_25	AM22	LX50T, LX85T, SX50T
25	IO_L17P_25	AN18	LX50T, LX85T, SX50T
25	IO_L17N_25	AM18	LX50T, LX85T, SX50T
25	IO_L18P_25	AP22	LX50T, LX85T, SX50T
25	IO_L18N_25	AP21	LX50T, LX85T, SX50T
25	IO_L19P_25	AN19	LX50T, LX85T, SX50T
25	IO_L19N_25	AP19	LX50T, LX85T, SX50T
NA	MGTTXP0_112	M2	
NA	MGTAVTTTX_112	M3	
NA	MGTTXN0_112	N2	

Table 2-5: **FF1136 Package—LX50T, FX70T, LX85T, LX110T, LX155T, SX50T, SX95T and FX100T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	MGTRXP0_112	N1	
NA	MGTAVTTRX_112	N3	
NA	MGTRXN0_112	P1	
NA	MGTAVCCPLL_112	T3	
NA	MGTRXN1_112	R1	
NA	MGTREFCLKN_112	P3	
NA	MGTRXP1_112	T1	
NA	MGTREFCLKP_112	P4	
NA	MGTTXN1_112	T2	
NA	MGTAVTTTX_112	U3	
NA	MGTTXP1_112	U2	
NA	MGTAVTTRXC	V5	
NA	MGTRREF_112	V4	
NC	NC	U5	LX50T, LX85T, LX110T, LX155T, SX50T, SX95T, FX70T, FX100T
NA	MGTTXP0_114	V2	
NA	MGTAVTTTX_114	AC3	
NA	MGTTXN0_114	W2	
NA	MGTRXP0_114	W1	
NA	MGTAVTTRX_114	W3	
NA	MGTRXN0_114	Y1	
NA	MGTAVCCPLL_114	AB3	
NA	MGTRXN1_114	AA1	
NA	MGTREFCLKN_114	Y3	
NA	MGTRXP1_114	AB1	
NA	MGTREFCLKP_114	Y4	
NA	MGTTXN1_114	AB2	
NA	MGTAVTTTX_114	V3	
NA	MGTTXP1_114	AC2	
NA	MGTTXP0_116	F2	
NA	MGTAVTTTX_116	F3	
NA	MGTTXN0_116	G2	

Table 2-5: **FF1136 Package—LX50T, FX70T, LX85T, LX110T, LX155T, SX50T, SX95T and FX100T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	MGTRXP0_116	G1	
NA	MGTAVTTRX_116	G3	
NA	MGTRXN0_116	H1	
NA	MGTAVCCPLL_116	K3	
NA	MGTRXN1_116	J1	
NA	MGTREFCLKN_116	H3	
NA	MGTRXP1_116	K1	
NA	MGTREFCLKP_116	H4	
NA	MGTTXN1_116	K2	
NA	MGTAVTTTX_116	L3	
NA	MGTTXP1_116	L2	
NA	MGTTXP0_118	AD2	
NA	MGTAVTTTX_118	AD3	
NA	MGTTXN0_118	AE2	
NA	MGTRXP0_118	AE1	
NA	MGTAVTTRX_118	AE3	
NA	MGTRXN0_118	AF1	
NA	MGTAVCCPLL_118	AH3	
NA	MGTRXN1_118	AG1	
NA	MGTREFCLKN_118	AF3	
NA	MGTRXP1_118	AH1	
NA	MGTREFCLKP_118	AF4	
NA	MGTTXN1_118	AH2	
NA	MGTAVTTTX_118	AJ3	
NA	MGTTXP1_118	AJ2	
NA	MGTTXP0_120	B4	
NA	MGTAVTTTX_120	C4	
NA	MGTTXN0_120	B3	
NA	MGTRXP0_120	A3	
NA	MGTAVTTRX_120	C3	
NA	MGTRXN0_120	A2	
NA	MGTAVCCPLL_120	D3	

Table 2-5: **FF1136 Package—LX50T, FX70T, LX85T, LX110T, LX155T, SX50T, SX95T and FX100T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	MGTRXN1_120	C1	
NA	MGTREFCLKN_120	D4	
NA	MGTRXP1_120	D1	
NA	MGTREFCLKP_120	E4	
NA	MGTTXN1_120	D2	
NA	MGTAVTTTX_120	E3	
NA	MGTTXP1_120	E2	
NA	MGTTXP0_122	AK2	
NA	MGTAVTTTX_122	AK3	
NA	MGTTXN0_122	AL2	
NA	MGTRXP0_122	AL1	
NA	MGTAVTTRX_122	AL3	
NA	MGTRXN0_122	AM1	
NA	MGTAVCCPLL_122	AM4	
NA	MGTRXN1_122	AP2	
NA	MGTREFCLKN_122	AL4	
NA	MGTRXP1_122	AP3	
NA	MGTREFCLKP_122	AL5	
NA	MGTTXN1_122	AN3	
NA	MGTAVTTTX_122	AM3	
NA	MGTTXP1_122	AN4	
NA	MGTTXP0_124	B10	LX50T, LX85T, SX50T
NA	MGTAVTTTX_124	C10	LX50T, LX85T, SX50T
NA	MGTTXN0_124	B9	LX50T, LX85T, SX50T
NA	MGTRXP0_124	A9	LX50T, LX85T, SX50T
NA	MGTAVTTRX_124	C9	LX50T, LX85T, SX50T
NA	MGTRXN0_124	A8	LX50T, LX85T, SX50T
NA	MGTAVCCPLL_124	C6	LX50T, LX85T, SX50T
NA	MGTRXN1_124	A7	LX50T, LX85T, SX50T
NA	MGTREFCLKN_124	C8	LX50T, LX85T, SX50T
NA	MGTRXP1_124	A6	LX50T, LX85T, SX50T
NA	MGTREFCLKP_124	D8	LX50T, LX85T, SX50T

Table 2-5: **FF1136 Package—LX50T, FX70T, LX85T, LX110T, LX155T, SX50T, SX95T and FX100T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	MGTTXN1_124	B6	LX50T, LX85T, SX50T
NA	MGTAVTTTX_124	C5	LX50T, LX85T, SX50T
NA	MGTTXP1_124	B5	LX50T, LX85T, SX50T
NA	MGTTXP0_126	AN5	LX50T, LX85T, SX50T
NA	MGTAVTTTX_126	AM10	LX50T, LX85T, SX50T
NA	MGTTXN0_126	AN6	LX50T, LX85T, SX50T
NA	MGTRXP0_126	AP6	LX50T, LX85T, SX50T
NA	MGTAVTTRX_126	AM6	LX50T, LX85T, SX50T
NA	MGTRXN0_126	AP7	LX50T, LX85T, SX50T
NA	MGTAVCCPLL_126	AM9	LX50T, LX85T, SX50T
NA	MGTRXN1_126	AP8	LX50T, LX85T, SX50T
NA	MGTREFCLKN_126	AM7	LX50T, LX85T, SX50T
NA	MGTRXP1_126	AP9	LX50T, LX85T, SX50T
NA	MGTREFCLKP_126	AL7	LX50T, LX85T, SX50T
NA	MGTTXN1_126	AN9	LX50T, LX85T, SX50T
NA	MGTAVTTTX_126	AM5	LX50T, LX85T, SX50T
NA	MGTTXP1_126	AN10	LX50T, LX85T, SX50T
NA	GND	B1	
NA	GND	AN1	
NA	GND	B2	
NA	GND	C2	
NA	GND	H2	
NA	GND	J2	
NA	GND	P2	
NA	GND	R2	
NA	GND	Y2	
NA	GND	AA2	
NA	GND	AF2	
NA	GND	AG2	
NA	GND	AM2	
NA	GND	AN2	
NA	GND	G4	

Table 2-5: **FF1136 Package—LX50T, FX70T, LX85T, LX110T, LX155T, SX50T, SX95T and FX100T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	K4	
NA	GND	M4	
NA	GND	N4	
NA	GND	T4	
NA	GND	W4	
NA	GND	AB4	
NA	GND	AE4	
NA	GND	AH4	
NA	GND	AK4	
NA	GND	E5	
NA	GND	K5	
NA	GND	R5	
NA	GND	T5	
NA	GND	W5	
NA	GND	Y5	
NA	GND	AE5	
NA	GND	AJ5	
NA	GND	D6	
NA	GND	H6	
NA	GND	U6	
NA	GND	V6	
NA	GND	AH6	
NA	GND	AL6	
NA	GND	B7	
NA	GND	F7	
NA	GND	L7	
NA	GND	AA7	
NA	GND	AN7	
NA	GND	B8	
NA	GND	P8	
NA	GND	AD8	
NA	GND	AN8	

Table 2-5: **FF1136 Package—LX50T, FX70T, LX85T, LX110T, LX155T, SX50T, SX95T and FX100T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	D9	
NA	GND	G9	
NA	GND	U9	
NA	GND	AG9	
NA	GND	AL9	
NA	GND	K10	
NA	GND	R10	
NA	GND	Y10	
NA	GND	AE10	
NA	GND	AK10	
NA	GND	A11	
NA	GND	B11	
NA	GND	C11	
NA	GND	N11	
NA	GND	U11	
NA	GND	AA11	
NA	GND	AC11	
NA	GND	AN11	
NA	GND	AP11	
NA	GND	A12	
NA	GND	F12	
NA	GND	M12	
NA	GND	P12	
NA	GND	T12	
NA	GND	V12	
NA	GND	Y12	
NA	GND	AB12	
NA	GND	AD12	
NA	GND	AF12	
NA	GND	J13	
NA	GND	L13	
NA	GND	N13	

Table 2-5: **FF1136 Package—LX50T, FX70T, LX85T, LX110T, LX155T, SX50T, SX95T and FX100T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	R13	
NA	GND	U13	
NA	GND	W13	
NA	GND	AA13	
NA	GND	AC13	
NA	GND	AJ13	
NA	GND	AP13	
NA	GND	B14	
NA	GND	M14	
NA	GND	P14	
NA	GND	T14	
NA	GND	V14	
NA	GND	Y14	
NA	GND	AB14	
NA	GND	AM14	
NA	GND	E15	
NA	GND	K15	
NA	GND	R15	
NA	GND	U15	
NA	GND	W15	
NA	GND	AA15	
NA	GND	AE15	
NA	GND	H16	
NA	GND	M16	
NA	GND	P16	
NA	GND	T16	
NA	GND	V16	
NA	GND	Y16	
NA	GND	AB16	
NA	GND	AD16	
NA	GND	AH16	
NA	GND	A17	

Table 2-5: **FF1136 Package—LX50T, FX70T, LX85T, LX110T, LX155T, SX50T, SX95T and FX100T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	L17	
NA	GND	N17	
NA	GND	R17	
NA	GND	AA17	
NA	GND	AC17	
NA	GND	AF17	
NA	GND	AL17	
NA	GND	D18	
NA	GND	J18	
NA	GND	M18	
NA	GND	P18	
NA	GND	Y18	
NA	GND	AB18	
NA	GND	AD18	
NA	GND	AP18	
NA	GND	G19	
NA	GND	N19	
NA	GND	R19	
NA	GND	U19	
NA	GND	W19	
NA	GND	AA19	
NA	GND	AC19	
NA	GND	AG19	
NA	GND	K20	
NA	GND	M20	
NA	GND	P20	
NA	GND	T20	
NA	GND	V20	
NA	GND	Y20	
NA	GND	AB20	
NA	GND	AE20	
NA	GND	AK20	

Table 2-5: **FF1136 Package—LX50T, FX70T, LX85T, LX110T, LX155T, SX50T, SX95T and FX100T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	C21	
NA	GND	H21	
NA	GND	N21	
NA	GND	R21	
NA	GND	U21	
NA	GND	W21	
NA	GND	AA21	
NA	GND	AC21	
NA	GND	AN21	
NA	GND	A22	
NA	GND	F22	
NA	GND	L22	
NA	GND	P22	
NA	GND	T22	
NA	GND	V22	
NA	GND	Y22	
NA	GND	AB22	
NA	GND	AF22	
NA	GND	J23	
NA	GND	R23	
NA	GND	U23	
NA	GND	W23	
NA	GND	AA23	
NA	GND	AJ23	
NA	GND	AP23	
NA	GND	B24	
NA	GND	M24	
NA	GND	AB24	
NA	GND	AG24	
NA	GND	AM24	
NA	GND	E25	
NA	GND	K25	

Table 2-5: **FF1136 Package—LX50T, FX70T, LX85T, LX110T, LX155T, SX50T, SX95T and FX100T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	R25	
NA	GND	Y25	
NA	GND	AE25	
NA	GND	H26	
NA	GND	N26	
NA	GND	V26	
NA	GND	AC26	
NA	GND	AH26	
NA	GND	A27	
NA	GND	L27	
NA	GND	AA27	
NA	GND	AF27	
NA	GND	AL27	
NA	GND	D28	
NA	GND	P28	
NA	GND	AD28	
NA	GND	AP28	
NA	GND	B29	
NA	GND	G29	
NA	GND	U29	
NA	GND	AG29	
NA	GND	K30	
NA	GND	Y30	
NA	GND	AK30	
NA	GND	C31	
NA	GND	N31	
NA	GND	AC31	
NA	GND	AN31	
NA	GND	A32	
NA	GND	F32	
NA	GND	T32	
NA	GND	AF32	

Table 2-5: **FF1136 Package—LX50T, FX70T, LX85T, LX110T, LX155T, SX50T, SX95T and FX100T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	D33	
NA	GND	J33	
NA	GND	W33	
NA	GND	AJ33	
NA	GND	AP33	
NA	GND	B34	
NA	GND	G34	
NA	GND	M34	
NA	GND	U34	
NA	GND	AB34	
NA	GND	AG34	
NA	GND	AM34	
NA	VCCAUX	M11	
NA	VCCAUX	P11	
NA	VCCAUX	V11	
NA	VCCAUX	AB11	
NA	VCCAUX	L12	
NA	VCCAUX	AC12	
NA	VCCAUX	M21	
NA	VCCAUX	P23	
NA	VCCAUX	T23	
NA	VCCAUX	V23	
NA	VCCAUX	Y23	
NA	VCCAUX	U24	
NA	VCCINT	N12	
NA	VCCINT	R12	
NA	VCCINT	U12	
NA	VCCINT	W12	
NA	VCCINT	AA12	
NA	VCCINT	M13	
NA	VCCINT	P13	
NA	VCCINT	T13	

Table 2-5: **FF1136 Package—LX50T, FX70T, LX85T, LX110T, LX155T, SX50T, SX95T and FX100T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	VCCINT	V13	
NA	VCCINT	Y13	
NA	VCCINT	AB13	
NA	VCCINT	AD13	
NA	VCCINT	R14	
NA	VCCINT	U14	
NA	VCCINT	W14	
NA	VCCINT	AA14	
NA	VCCINT	T15	
NA	VCCINT	V15	
NA	VCCINT	Y15	
NA	VCCINT	N16	
NA	VCCINT	R16	
NA	VCCINT	U16	
NA	VCCINT	W16	
NA	VCCINT	AA16	
NA	VCCINT	AC16	
NA	VCCINT	M17	
NA	VCCINT	P17	
NA	VCCINT	Y17	
NA	VCCINT	AB17	
NA	VCCINT	AD17	
NA	VCCINT	N18	
NA	VCCINT	R18	
NA	VCCINT	AA18	
NA	VCCINT	AC18	
NA	VCCINT	M19	
NA	VCCINT	P19	
NA	VCCINT	T19	
NA	VCCINT	V19	
NA	VCCINT	Y19	
NA	VCCINT	AB19	

Table 2-5: **FF1136 Package—LX50T, FX70T, LX85T, LX110T, LX155T, SX50T, SX95T and FX100T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	VCCINT	N20	
NA	VCCINT	R20	
NA	VCCINT	U20	
NA	VCCINT	W20	
NA	VCCINT	AA20	
NA	VCCINT	AC20	
NA	VCCINT	P21	
NA	VCCINT	T21	
NA	VCCINT	V21	
NA	VCCINT	Y21	
NA	VCCINT	AB21	
NA	VCCINT	R22	
NA	VCCINT	U22	
NA	VCCINT	W22	
0	VCCO_0	AA22	
0	VCCO_0	AD23	
1	VCCO_1	D13	
1	VCCO_1	G14	
2	VCCO_2	AM19	
2	VCCO_2	AH21	
3	VCCO_3	E20	
3	VCCO_3	D23	
4	VCCO_4	AL12	
4	VCCO_4	AG14	
5	VCCO_5	C16	
5	VCCO_5	F17	
5	VCCO_5	B19	
6	VCCO_6	AK15	
6	VCCO_6	AN16	
6	VCCO_6	AJ18	
11	VCCO_11	T27	
11	VCCO_11	R30	

Table 2-5: **FF1136 Package—LX50T, FX70T, LX85T, LX110T, LX155T, SX50T, SX95T and FX100T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
11	VCCO_11	V31	
12	VCCO_12	N6	
12	VCCO_12	T7	
12	VCCO_12	M9	
13	VCCO_13	W28	
13	VCCO_13	AB29	
13	VCCO_13	AA32	
15	VCCO_15	M29	
15	VCCO_15	L32	
15	VCCO_15	P33	
17	VCCO_17	AE30	
17	VCCO_17	AH31	
17	VCCO_17	AD33	
18	VCCO_18	AC6	
18	VCCO_18	W8	
18	VCCO_18	AB9	
19	VCCO_19	J28	
19	VCCO_19	E30	
19	VCCO_19	H31	
20	VCCO_20	J8	
20	VCCO_20	E10	
20	VCCO_20	H11	
21	VCCO_21	AJ28	
21	VCCO_21	AM29	
21	VCCO_21	AL32	
22	VCCO_22	AF7	
22	VCCO_22	AJ8	
22	VCCO_22	AH11	
23	VCCO_23	G24	
23	VCCO_23	C26	
23	VCCO_23	F27	
25	VCCO_25	AL22	

Table 2-5: **FF1136 Package—LX50T, FX70T, LX85T, LX110T, LX155T, SX50T, SX95T and FX100T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
25	VCCO_25	AK25	
25	VCCO_25	AN26	
NA	MGTAVCC_112	R3	
NA	MGTAVCC_112	R4	
NA	MGTAVCC_114	AA3	
NA	MGTAVCC_114	AA4	
NA	MGTAVCC_116	J3	
NA	MGTAVCC_116	J4	
NA	MGTAVCC_118	AG3	
NA	MGTAVCC_118	AG4	
NA	MGTAVCC_120	D5	
NA	MGTAVCC_120	F4	
NA	MGTAVCC_122	AJ4	
NA	MGTAVCC_122	AK5	
NA	MGTAVCC_124	C7	LX50T, LX85T, SX50T
NA	MGTAVCC_124	D7	LX50T, LX85T, SX50T
NA	MGTAVCC_126	AL8	LX50T, LX85T, SX50T
NA	MGTAVCC_126	AM8	LX50T, LX85T, SX50T
NA	FLOAT	U4	

Notes:

1. Do not connect a single-ended clock to the N-side of the differential clock pair of pins, for example, IO_L3N_GC_3.
2. Do not connect a single-ended clock to the N-side of clock capable pins, for example, IO_L8N_CC_11.
3. RSVD pins must be tied to GND (logic 0).

FF1153 Package—LX50, LX85, LX110, and LX155

Table 2-6: **FF1153 Package—LX50, LX85, LX110, and LX155**

Bank	Pin Description	Pin Number	No Connect (NC)
0	DXP_0	W18	
0	DXN_0	W17	
0	AVDD_0	T18	
0	AVSS_0	T17	
0	VP_0	U18	
0	VN_0	V17	
0	VREFP_0	V18	
0	VREFN_0	U17	
0	VBATT_0	P22	
0	PROGRAM_B_0	M22	
0	HSWAPEN_0	N22	
0	D_IN_0	N13	
0	DONE_0	N14	
0	CCLK_0	M13	
0	INIT_B_0	L13	
0	CS_B_0	M23	
0	RDWR_B_0	N23	
0	RSVD(3)	AB23	
0	RSVD(3)	AC23	
0	TCK_0	AA13	
0	M0_0	AD21	
0	M2_0	AD22	
0	M1_0	AC22	
0	TMS_0	AB13	
0	TDI_0	AC13	
0	D_OUT_BUSY_0	AD14	
0	TDO_0	AC14	
1	IO_L0P_A19_1	L20	
1	IO_L0N_A18_1	L19	
1	IO_L1P_A17_1	K17	
1	IO_L1N_A16_1	K18	

Table 2-6: **FF1153 Package—LX50, LX85, LX110, and LX155 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
1	IO_L2P_A15_D31_1	K21	
1	IO_L2N_A14_D30_1	L21	
1	IO_L3P_A13_D29_1	K16	
1	IO_L3N_A12_D28_1	L16	
1	IO_L4P_A11_D27_1	J19	
1	IO_L4N_VREF_A10_D26_1	K19	
1	IO_L5P_A9_D25_1	K12	
1	IO_L5N_A8_D24_1	J12	
1	IO_L6P_A7_D23_1	K22	
1	IO_L6N_A6_D22_1	J22	
1	IO_L7P_A5_D21_1	K13	
1	IO_L7N_A4_D20_1	K14	
1	IO_L8P_CC_A3_D19_1	L23	
1	IO_L8N_CC_A2_D18_1 (2)	K23	
1	IO_L9P_CC_A1_D17_1	L14	
1	IO_L9N_CC_A0_D16_1 (2)	L15	
2	IO_L0P_CC_RS1_2	AC15	
2	IO_L0N_CC_RS0_2 (2)	AD15	
2	IO_L1P_CC_A25_2	AE22	
2	IO_L1N_CC_A24_2 (2)	AE23	
2	IO_L2P_A23_2	AF15	
2	IO_L2N_A22_2	AE14	
2	IO_L3P_A21_2	AG23	
2	IO_L3N_A20_2	AF23	
2	IO_L4P_FCS_B_2	AE12	
2	IO_L4N_VREF_FOE_B_MOSI_2	AE13	
2	IO_L5P_FWE_B_2	AD20	
2	IO_L5N_CSO_B_2	AE21	
2	IO_L6P_D7_2	AE16	
2	IO_L6N_D6_2	AF16	
2	IO_L7P_D5_2	AD19	
2	IO_L7N_D4_2	AE19	
2	IO_L8P_D3_2	AD16	

Table 2-6: **FF1153 Package—LX50, LX85, LX110, and LX155 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
2	IO_L8N_D2_FS2_2	AE17	
2	IO_L9P_D1_FS1_2	AC19	
2	IO_L9N_D0_FS0_2	AC20	
3	IO_L0P_CC_GC_3	H18	
3	IO_L0N_CC_GC_3 (1)(2)	J17	
3	IO_L1P_CC_GC_3	H19	
3	IO_L1N_CC_GC_3 (1)(2)	H20	
3	IO_L2P_GC_VRN_3	J16	
3	IO_L2N_GC_VRP_3 (1)	J15	
3	IO_L3P_GC_3	J20	
3	IO_L3N_GC_3 (1)	J21	
3	IO_L4P_GC_3	J14	
3	IO_L4N_GC_VREF_3 (1)	H15	
3	IO_L5P_GC_3	G20	
3	IO_L5N_GC_3 (1)	F20	
3	IO_L6P_GC_3	H13	
3	IO_L6N_GC_3 (1)	H14	
3	IO_L7P_GC_3	G21	
3	IO_L7N_GC_3 (1)	G22	
3	IO_L8P_GC_3	H12	
3	IO_L8N_GC_3 (1)	G13	
3	IO_L9P_GC_3	H22	
3	IO_L9N_GC_3 (1)	H23	
4	IO_L0P_GC_D15_4	AG22	
4	IO_L0N_GC_D14_4 (1)	AF21	
4	IO_L1P_GC_D13_4	AG13	
4	IO_L1N_GC_D12_4 (1)	AF13	
4	IO_L2P_GC_D11_4	AG21	
4	IO_L2N_GC_D10_4 (1)	AH20	
4	IO_L3P_GC_D9_4	AH12	
4	IO_L3N_GC_D8_4 (1)	AG12	
4	IO_L4P_GC_4	AK19	
4	IO_L4N_GC_VREF_4 (1)	AJ19	

Table 2-6: **FF1153 Package—LX50, LX85, LX110, and LX155 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
4	IO_L5P_GC_4	AG15	
4	IO_L5N_GC_4 (1)	AF14	
4	IO_L6P_GC_4	AH19	
4	IO_L6N_GC_4 (1)	AG20	
4	IO_L7P_GC_VRN_4	AG17	
4	IO_L7N_GC_VRP_4 (1)	AG16	
4	IO_L8P_CC_GC_4	AF20	
4	IO_L8N_CC_GC_4 (1)(2)	AF19	
4	IO_L9P_CC_GC_4	AE18	
4	IO_L9N_CC_GC_4 (1)(2)	AF18	
5	IO_L0P_5	D15	LX50, LX85
5	IO_L0N_5	D14	LX50, LX85
5	IO_L1P_5	D12	LX50, LX85
5	IO_L1N_5	E11	LX50, LX85
5	IO_L2P_5	D16	LX50, LX85
5	IO_L2N_5	D17	LX50, LX85
5	IO_L3P_5	E12	LX50, LX85
5	IO_L3N_5	E13	LX50, LX85
5	IO_L4P_5	F19	LX50, LX85
5	IO_L4N_VREF_5	F18	LX50, LX85
5	IO_L5P_5	E18	LX50, LX85
5	IO_L5N_5	E17	LX50, LX85
5	IO_L6P_5	D19	LX50, LX85
5	IO_L6N_5	E19	LX50, LX85
5	IO_L7P_5	E16	LX50, LX85
5	IO_L7N_5	F16	LX50, LX85
5	IO_L8P_CC_5	D21	LX50, LX85
5	IO_L8N_CC_5 (2)	D20	LX50, LX85
5	IO_L9P_CC_5	G18	LX50, LX85
5	IO_L9N_CC_5 (2)	G17	LX50, LX85
5	IO_L10P_CC_5	G16	LX50, LX85
5	IO_L10N_CC_5 (2)	H17	LX50, LX85
5	IO_L11P_CC_5	E21	LX50, LX85

Table 2-6: **FF1153 Package—LX50, LX85, LX110, and LX155 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
5	IO_L11N_CC_5 (2)	F21	LX50, LX85
5	IO_L12P_VRN_5	F15	LX50, LX85
5	IO_L12N_VRP_5	E14	LX50, LX85
5	IO_L13P_5	D22	LX50, LX85
5	IO_L13N_5	E23	LX50, LX85
5	IO_L14P_5	G15	LX50, LX85
5	IO_L14N_VREF_5	F14	LX50, LX85
5	IO_L15P_5	E22	LX50, LX85
5	IO_L15N_5	F23	LX50, LX85
5	IO_L16P_5	G12	LX50, LX85
5	IO_L16N_5	F13	LX50, LX85
5	IO_L17P_5	D24	LX50, LX85
5	IO_L17N_5	E24	LX50, LX85
5	IO_L18P_5	G11	LX50, LX85
5	IO_L18N_5	F11	LX50, LX85
5	IO_L19P_5	F24	LX50, LX85
5	IO_L19N_5	G23	LX50, LX85
6	IO_L0P_6	AH22	LX50, LX85
6	IO_L0N_6	AH23	LX50, LX85
6	IO_L1P_6	AH14	LX50, LX85
6	IO_L1N_6	AH13	LX50, LX85
6	IO_L2P_6	AH24	LX50, LX85
6	IO_L2N_6	AJ24	LX50, LX85
6	IO_L3P_6	AJ14	LX50, LX85
6	IO_L3N_6	AH15	LX50, LX85
6	IO_L4P_6	AJ22	LX50, LX85
6	IO_L4N_VREF_6	AJ21	LX50, LX85
6	IO_L5P_6	AJ11	LX50, LX85
6	IO_L5N_6	AJ12	LX50, LX85
6	IO_L6P_6	AJ20	LX50, LX85
6	IO_L6N_6	AK21	LX50, LX85
6	IO_L7P_6	AK14	LX50, LX85
6	IO_L7N_6	AJ15	LX50, LX85

Table 2-6: **FF1153 Package—LX50, LX85, LX110, and LX155 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
6	IO_L8P_CC_6	AK22	LX50, LX85
6	IO_L8N_CC_6 (2)	AK23	LX50, LX85
6	IO_L9P_CC_6	AJ16	LX50, LX85
6	IO_L9N_CC_6 (2)	AH17	LX50, LX85
6	IO_L10P_CC_6	AJ17	LX50, LX85
6	IO_L10N_CC_6 (2)	AK16	LX50, LX85
6	IO_L11P_CC_6	AL23	LX50, LX85
6	IO_L11N_CC_6 (2)	AK24	LX50, LX85
6	IO_L12P_VRN_6	AK17	LX50, LX85
6	IO_L12N_VRP_6	AK18	LX50, LX85
6	IO_L13P_6	AL20	LX50, LX85
6	IO_L13N_6	AL21	LX50, LX85
6	IO_L14P_6	AG18	LX50, LX85
6	IO_L14N_VREF_6	AH18	LX50, LX85
6	IO_L15P_6	AL18	LX50, LX85
6	IO_L15N_6	AL19	LX50, LX85
6	IO_L16P_6	AK13	LX50, LX85
6	IO_L16N_6	AK12	LX50, LX85
6	IO_L17P_6	AL15	LX50, LX85
6	IO_L17N_6	AL16	LX50, LX85
6	IO_L18P_6	AK11	LX50, LX85
6	IO_L18N_6	AL11	LX50, LX85
6	IO_L19P_6	AL13	LX50, LX85
6	IO_L19N_6	AL14	LX50, LX85
11	IO_L0P_11	B32	
11	IO_L0N_11	A33	
11	IO_L1P_11	B33	
11	IO_L1N_11	C33	
11	IO_L2P_11	C32	
11	IO_L2N_11	D32	
11	IO_L3P_11	C34	
11	IO_L3N_11	D34	
11	IO_L4P_11	G32	

Table 2-6: **FF1153 Package—LX50, LX85, LX110, and LX155 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
11	IO_L4N_VREF_11	H32	
11	IO_L5P_11	F33	
11	IO_L5N_11	E34	
11	IO_L6P_11	E32	
11	IO_L6N_11	E33	
11	IO_L7P_11	G33	
11	IO_L7N_11	F34	
11	IO_L8P_CC_11	J32	
11	IO_L8N_CC_11 (2)	H33	
11	IO_L9P_CC_11	H34	
11	IO_L9N_CC_11 (2)	J34	
11	IO_L10P_CC_SM15P_11	L34	
11	IO_L10N_CC_SM15N_11 (2)	K34	
11	IO_L11P_CC_SM14P_11	K33	
11	IO_L11N_CC_SM14N_11 (2)	K32	
11	IO_L12P_VRN_11	N33	
11	IO_L12N_VRP_11	M33	
11	IO_L13P_11	L33	
11	IO_L13N_11	M32	
11	IO_L14P_11	P34	
11	IO_L14N_VREF_11	N34	
11	IO_L15P_SM13P_11	P32	
11	IO_L15N_SM13N_11	N32	
11	IO_L16P_SM12P_11	T33	
11	IO_L16N_SM12N_11	R34	
11	IO_L17P_SM11P_11	R33	
11	IO_L17N_SM11N_11	R32	
11	IO_L18P_SM10P_11	U33	
11	IO_L18N_SM10N_11	T34	
11	IO_L19P_SM9P_11	U31	
11	IO_L19N_SM9N_11	U32	
12	IO_L0P_12	A3	
12	IO_L0N_12	B3	

Table 2-6: **FF1153 Package—LX50, LX85, LX110, and LX155 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
12	IO_L1P_12	C2	
12	IO_L1N_12	B1	
12	IO_L2P_12	C3	
12	IO_L2N_12	B2	
12	IO_L3P_12	D2	
12	IO_L3N_12	D1	
12	IO_L4P_12	E3	
12	IO_L4N_VREF_12	F3	
12	IO_L5P_12	E2	
12	IO_L5N_12	E1	
12	IO_L6P_12	G3	
12	IO_L6N_12	G2	
12	IO_L7P_12	F1	
12	IO_L7N_12	G1	
12	IO_L8P_CC_12	K3	
12	IO_L8N_CC_12 (2)	L3	
12	IO_L9P_CC_12	J2	
12	IO_L9N_CC_12 (2)	K2	
12	IO_L10P_CC_12	K1	
12	IO_L10N_CC_12 (2)	J1	
12	IO_L11P_CC_12	H2	
12	IO_L11N_CC_12 (2)	H3	
12	IO_L12P_VRN_12	M1	
12	IO_L12N_VRP_12	L1	
12	IO_L13P_12	M3	
12	IO_L13N_12	N3	
12	IO_L14P_12	P2	
12	IO_L14N_VREF_12	R3	
12	IO_L15P_12	N2	
12	IO_L15N_12	M2	
12	IO_L16P_12	T1	
12	IO_L16N_12	R1	
12	IO_L17P_12	P1	

Table 2-6: **FF1153 Package—LX50, LX85, LX110, and LX155 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
12	IO_L17N_12	R2	
12	IO_L18P_12	U1	
12	IO_L18N_12	U2	
12	IO_L19P_12	U3	
12	IO_L19N_12	T3	
13	IO_L0P_SM8P_13	V33	
13	IO_L0N_SM8N_13	V32	
13	IO_L1P_SM7P_13	W34	
13	IO_L1N_SM7N_13	V34	
13	IO_L2P_SM6P_13	AA33	
13	IO_L2N_SM6N_13	Y33	
13	IO_L3P_SM5P_13	AA34	
13	IO_L3N_SM5N_13	Y34	
13	IO_L4P_13	Y32	
13	IO_L4N_VREF_13	W32	
13	IO_L5P_SM4P_13	AC34	
13	IO_L5N_SM4N_13	AD34	
13	IO_L6P_SM3P_13	AC32	
13	IO_L6N_SM3N_13	AB32	
13	IO_L7P_SM2P_13	AC33	
13	IO_L7N_SM2N_13	AB33	
13	IO_L8P_CC_SM1P_13	AF33	
13	IO_L8N_CC_SM1N_13 (2)	AE33	
13	IO_L9P_CC_SM0P_13	AF34	
13	IO_L9N_CC_SM0N_13 (2)	AE34	
13	IO_L10P_CC_13	AH34	
13	IO_L10N_CC_13 (2)	AJ34	
13	IO_L11P_CC_13	AD32	
13	IO_L11N_CC_13 (2)	AE32	
13	IO_L12P_VRN_13	AG33	
13	IO_L12N_VRP_13	AH33	
13	IO_L13P_13	AK34	
13	IO_L13N_13	AK33	

Table 2-6: **FF1153 Package—LX50, LX85, LX110, and LX155 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
13	IO_L14P_13	AG32	
13	IO_L14N_VREF_13	AH32	
13	IO_L15P_13	AJ32	
13	IO_L15N_13	AK32	
13	IO_L16P_13	AL34	
13	IO_L16N_13	AL33	
13	IO_L17P_13	AM33	
13	IO_L17N_13	AM32	
13	IO_L18P_13	AN34	
13	IO_L18N_13	AN33	
13	IO_L19P_13	AN32	
13	IO_L19N_13	AP32	
14	IO_L0P_14	V4	
14	IO_L0N_14	V3	
14	IO_L1P_14	W1	
14	IO_L1N_14	V2	
14	IO_L2P_14	Y3	
14	IO_L2N_14	Y2	
14	IO_L3P_14	W2	
14	IO_L3N_14	Y1	
14	IO_L4P_14	AC3	
14	IO_L4N_VREF_14	AB2	
14	IO_L5P_14	AB1	
14	IO_L5N_14	AA1	
14	IO_L6P_14	AB3	
14	IO_L6N_14	AA3	
14	IO_L7P_14	AC2	
14	IO_L7N_14	AD1	
14	IO_L8P_CC_14	AE2	
14	IO_L8N_CC_14 (2)	AD2	
14	IO_L9P_CC_14	AF1	
14	IO_L9N_CC_14 (2)	AE1	
14	IO_L10P_CC_14	AG1	

Table 2-6: **FF1153 Package—LX50, LX85, LX110, and LX155 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
14	IO_L10N_CC_14 (2)	AG2	
14	IO_L11P_CC_14	AF3	
14	IO_L11N_CC_14 (2)	AE3	
14	IO_L12P_VRN_14	AJ1	
14	IO_L12N_VRP_14	AK1	
14	IO_L13P_14	AK2	
14	IO_L13N_14	AK3	
14	IO_L14P_14	AH2	
14	IO_L14N_VREF_14	AJ2	
14	IO_L15P_14	AG3	
14	IO_L15N_14	AH3	
14	IO_L16P_14	AL1	
14	IO_L16N_14	AM1	
14	IO_L17P_14	AN2	
14	IO_L17N_14	AP2	
14	IO_L18P_14	AM2	
14	IO_L18N_14	AL3	
14	IO_L19P_14	AM3	
14	IO_L19N_14	AN3	
15	IO_L0P_15	E29	
15	IO_L0N_15	F29	
15	IO_L1P_15	G30	
15	IO_L1N_15	F30	
15	IO_L2P_15	H29	
15	IO_L2N_15	J29	
15	IO_L3P_15	F31	
15	IO_L3N_15	E31	
15	IO_L4P_15	K29	
15	IO_L4N_VREF_15	L29	
15	IO_L5P_15	H30	
15	IO_L5N_15	G31	
15	IO_L6P_15	J30	
15	IO_L6N_15	J31	

Table 2-6: **FF1153 Package—LX50, LX85, LX110, and LX155 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
15	IO_L7P_15	L30	
15	IO_L7N_15	M30	
15	IO_L8P_CC_15	N29	
15	IO_L8N_CC_15 (2)	P29	
15	IO_L9P_CC_15	K31	
15	IO_L9N_CC_15 (2)	L31	
15	IO_L10P_CC_15	P31	
15	IO_L10N_CC_15 (2)	P30	
15	IO_L11P_CC_15	N30	
15	IO_L11N_CC_15 (2)	M31	
15	IO_L12P_VRN_15	R28	
15	IO_L12N_VRP_15	R29	
15	IO_L13P_15	T31	
15	IO_L13N_15	R31	
15	IO_L14P_15	U30	
15	IO_L14N_VREF_15	T30	
15	IO_L15P_15	T28	
15	IO_L15N_15	T29	
15	IO_L16P_15	U27	
15	IO_L16N_15	U28	
15	IO_L17P_15	R26	
15	IO_L17N_15	R27	
15	IO_L18P_15	U26	
15	IO_L18N_15	T26	
15	IO_L19P_15	U25	
15	IO_L19N_15	T25	
16	IO_L0P_16	J6	
16	IO_L0N_16	K6	
16	IO_L1P_16	G5	
16	IO_L1N_16	F5	
16	IO_L2P_16	J5	
16	IO_L2N_16	H5	
16	IO_L3P_16	E4	

Table 2-6: **FF1153 Package—LX50, LX85, LX110, and LX155 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
16	IO_L3N_16	F4	
16	IO_L4P_16	L6	
16	IO_L4N_VREF_16	M6	
16	IO_L5P_16	H4	
16	IO_L5N_16	J4	
16	IO_L6P_16	M5	
16	IO_L6N_16	L5	
16	IO_L7P_16	K4	
16	IO_L7N_16	L4	
16	IO_L8P_CC_16	N4	
16	IO_L8N_CC_16 (2)	N5	
16	IO_L9P_CC_16	P4	
16	IO_L9N_CC_16 (2)	R4	
16	IO_L10P_CC_16	U5	
16	IO_L10N_CC_16 (2)	T4	
16	IO_L11P_CC_16	P5	
16	IO_L11N_CC_16 (2)	P6	
16	IO_L12P_VRN_16	R9	
16	IO_L12N_VRP_16	R8	
16	IO_L13P_16	U6	
16	IO_L13N_16	T5	
16	IO_L14P_16	R6	
16	IO_L14N_VREF_16	R7	
16	IO_L15P_16	U7	
16	IO_L15N_16	T6	
16	IO_L16P_16	U8	
16	IO_L16N_16	T8	
16	IO_L17P_16	R11	
16	IO_L17N_16	T10	
16	IO_L18P_16	U10	
16	IO_L18N_16	T9	
16	IO_L19P_16	U11	
16	IO_L19N_16	T11	

Table 2-6: **FF1153 Package—LX50, LX85, LX110, and LX155 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
17	IO_L0P_17	W24	
17	IO_L0N_17	V24	
17	IO_L1P_17	Y26	
17	IO_L1N_17	W26	
17	IO_L2P_17	V25	
17	IO_L2N_17	W25	
17	IO_L3P_17	Y27	
17	IO_L3N_17	W27	
17	IO_L4P_17	V30	
17	IO_L4N_VREF_17	W30	
17	IO_L5P_17	V28	
17	IO_L5N_17	V27	
17	IO_L6P_17	W31	
17	IO_L6N_17	Y31	
17	IO_L7P_17	W29	
17	IO_L7N_17	V29	
17	IO_L8P_CC_17	Y28	
17	IO_L8N_CC_17 (2)	Y29	
17	IO_L9P_CC_17	AB31	
17	IO_L9N_CC_17 (2)	AA31	
17	IO_L10P_CC_17	AC30	
17	IO_L10N_CC_17 (2)	AB30	
17	IO_L11P_CC_17	AA29	
17	IO_L11N_CC_17 (2)	AA30	
17	IO_L12P_VRN_17	AD31	
17	IO_L12N_VRP_17	AE31	
17	IO_L13P_17	AD30	
17	IO_L13N_17	AC29	
17	IO_L14P_17	AF31	
17	IO_L14N_VREF_17	AG31	
17	IO_L15P_17	AE29	
17	IO_L15N_17	AD29	
17	IO_L16P_17	AJ31	

Table 2-6: **FF1153 Package—LX50, LX85, LX110, and LX155 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
17	IO_L16N_17	AK31	
17	IO_L17P_17	AF29	
17	IO_L17N_17	AF30	
17	IO_L18P_17	AJ30	
17	IO_L18N_17	AH30	
17	IO_L19P_17	AH29	
17	IO_L19N_17	AG30	
18	IO_L0P_18	Y11	
18	IO_L0N_18	W11	
18	IO_L1P_18	W9	
18	IO_L1N_18	Y9	
18	IO_L2P_18	W10	
18	IO_L2N_18	V10	
18	IO_L3P_18	V9	
18	IO_L3N_18	V8	
18	IO_L4P_18	W7	
18	IO_L4N_VREF_18	V7	
18	IO_L5P_18	W5	
18	IO_L5N_18	V5	
18	IO_L6P_18	Y7	
18	IO_L6N_18	Y8	
18	IO_L7P_18	Y6	
18	IO_L7N_18	W6	
18	IO_L8P_CC_18	AA6	
18	IO_L8N_CC_18 (2)	AA5	
18	IO_L9P_CC_18	Y4	
18	IO_L9N_CC_18 (2)	W4	
18	IO_L10P_CC_18	AA4	
18	IO_L10N_CC_18 (2)	AB5	
18	IO_L11P_CC_18	AB6	
18	IO_L11N_CC_18 (2)	AC5	
18	IO_L12P_VRN_18	AC4	
18	IO_L12N_VRP_18	AD4	

Table 2-6: **FF1153 Package—LX50, LX85, LX110, and LX155 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
18	IO_L13P_18	AD5	
18	IO_L13N_18	AD6	
18	IO_L14P_18	AE4	
18	IO_L14N_VREF_18	AF4	
18	IO_L15P_18	AF5	
18	IO_L15N_18	AE6	
18	IO_L16P_18	AH4	
18	IO_L16N_18	AJ4	
18	IO_L17P_18	AF6	
18	IO_L17N_18	AG6	
18	IO_L18P_18	AK4	
18	IO_L18N_18	AJ5	
18	IO_L19P_18	AG5	
18	IO_L19N_18	AH5	
19	IO_L0P_19	K24	
19	IO_L0N_19	L24	
19	IO_L1P_19	L25	
19	IO_L1N_19	L26	
19	IO_L2P_19	J24	
19	IO_L2N_19	J25	
19	IO_L3P_19	M25	
19	IO_L3N_19	M26	
19	IO_L4P_19	J27	
19	IO_L4N_VREF_19	J26	
19	IO_L5P_19	G25	
19	IO_L5N_19	G26	
19	IO_L6P_19	H25	
19	IO_L6N_19	H24	
19	IO_L7P_19	F25	
19	IO_L7N_19	F26	
19	IO_L8P_CC_19	G27	
19	IO_L8N_CC_19 (2)	H27	
19	IO_L9P_CC_19	H28	

Table 2-6: **FF1153 Package—LX50, LX85, LX110, and LX155 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
19	IO_L9N_CC_19(2)	G28	
19	IO_L10P_CC_19	E28	
19	IO_L10N_CC_19(2)	F28	
19	IO_L11P_CC_19	E26	
19	IO_L11N_CC_19(2)	E27	
19	IO_L12P_VRN_19	N27	
19	IO_L12N_VRP_19	M27	
19	IO_L13P_19	K28	
19	IO_L13N_19	L28	
19	IO_L14P_19	K27	
19	IO_L14N_VREF_19	K26	
19	IO_L15P_19	M28	
19	IO_L15N_19	N28	
19	IO_L16P_19	P26	
19	IO_L16N_19	P27	
19	IO_L17P_19	N24	
19	IO_L17N_19	P24	
19	IO_L18P_19	P25	
19	IO_L18N_19	N25	
19	IO_L19P_19	R24	
19	IO_L19N_19	T24	
20	IO_L0P_20	K11	
20	IO_L0N_20	J11	
20	IO_L1P_20	H10	
20	IO_L1N_20	G10	
20	IO_L2P_20	J10	
20	IO_L2N_20	J9	
20	IO_L3P_20	F10	
20	IO_L3N_20	E9	
20	IO_L4P_20	L11	
20	IO_L4N_VREF_20	L10	
20	IO_L5P_20	E7	
20	IO_L5N_20	E8	

Table 2-6: **FF1153 Package—LX50, LX85, LX110, and LX155 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
20	IO_L6P_20	M11	
20	IO_L6N_20	M10	
20	IO_L7P_20	F9	
20	IO_L7N_20	F8	
20	IO_L8P_CC_20	K9	
20	IO_L8N_CC_20 (2)	L9	
20	IO_L9P_CC_20	H9	
20	IO_L9N_CC_20 (2)	G8	
20	IO_L10P_CC_20	F6	
20	IO_L10N_CC_20 (2)	E6	
20	IO_L11P_CC_20	L8	
20	IO_L11N_CC_20 (2)	K8	
20	IO_L12P_VRN_20	H7	
20	IO_L12N_VRP_20	H8	
20	IO_L13P_20	K7	
20	IO_L13N_20	J7	
20	IO_L14P_20	G6	
20	IO_L14N_VREF_20	G7	
20	IO_L15P_20	M8	
20	IO_L15N_20	M7	
20	IO_L16P_20	P7	
20	IO_L16N_20	N7	
20	IO_L17P_20	N9	
20	IO_L17N_20	N10	
20	IO_L18P_20	P9	
20	IO_L18N_20	N8	
20	IO_L19P_20	P11	
20	IO_L19N_20	P10	
21	IO_L0P_21	AA25	
21	IO_L0N_21	AA26	
21	IO_L1P_21	AB27	
21	IO_L1N_21	AC27	
21	IO_L2P_21	Y24	

Table 2-6: **FF1153 Package—LX50, LX85, LX110, and LX155 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
21	IO_L2N_21	AA24	
21	IO_L3P_21	AB25	
21	IO_L3N_21	AB26	
21	IO_L4P_21	AC28	
21	IO_L4N_VREF_21	AD27	
21	IO_L5P_21	AB28	
21	IO_L5N_21	AA28	
21	IO_L6P_21	AG28	
21	IO_L6N_21	AH28	
21	IO_L7P_21	AE28	
21	IO_L7N_21	AF28	
21	IO_L8P_CC_21	AK26	
21	IO_L8N_CC_21 (2)	AJ27	
21	IO_L9P_CC_21	AK29	
21	IO_L9N_CC_21 (2)	AJ29	
21	IO_L10P_CC_21	AK28	
21	IO_L10N_CC_21 (2)	AK27	
21	IO_L11P_CC_21	AH27	
21	IO_L11N_CC_21 (2)	AJ26	
21	IO_L12P_VRN_21	AJ25	
21	IO_L12N_VRP_21	AH25	
21	IO_L13P_21	AF24	
21	IO_L13N_21	AG25	
21	IO_L14P_21	AG27	
21	IO_L14N_VREF_21	AG26	
21	IO_L15P_21	AF25	
21	IO_L15N_21	AF26	
21	IO_L16P_21	AE27	
21	IO_L16N_21	AE26	
21	IO_L17P_21	AC25	
21	IO_L17N_21	AC24	
21	IO_L18P_21	AD26	
21	IO_L18N_21	AD25	

Table 2-6: **FF1153 Package—LX50, LX85, LX110, and LX155 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
21	IO_L19P_21	AD24	
21	IO_L19N_21	AE24	
22	IO_L0P_22	AA10	
22	IO_L0N_22	AA11	
22	IO_L1P_22	AA8	
22	IO_L1N_22	AA9	
22	IO_L2P_22	AB11	
22	IO_L2N_22	AB10	
22	IO_L3P_22	AB8	
22	IO_L3N_22	AB7	
22	IO_L4P_22	AC8	
22	IO_L4N_VREF_22	AC7	
22	IO_L5P_22	AJ7	
22	IO_L5N_22	AJ6	
22	IO_L6P_22	AE7	
22	IO_L6N_22	AD7	
22	IO_L7P_22	AG7	
22	IO_L7N_22	AH7	
22	IO_L8P_CC_22	AD9	
22	IO_L8N_CC_22 (2)	AC9	
22	IO_L9P_CC_22	AG8	
22	IO_L9N_CC_22 (2)	AH8	
22	IO_L10P_CC_22	AE8	
22	IO_L10N_CC_22 (2)	AF8	
22	IO_L11P_CC_22	AC10	
22	IO_L11N_CC_22 (2)	AD10	
22	IO_L12P_VRN_22	AK6	
22	IO_L12N_VRP_22	AK7	
22	IO_L13P_22	AE9	
22	IO_L13N_22	AF9	
22	IO_L14P_22	AH9	
22	IO_L14N_VREF_22	AJ9	
22	IO_L15P_22	AF10	

Table 2-6: **FF1153 Package—LX50, LX85, LX110, and LX155 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
22	IO_L15N_22	AG10	
22	IO_L16P_22	AK9	
22	IO_L16N_22	AK8	
22	IO_L17P_22	AG11	
22	IO_L17N_22	AF11	
22	IO_L18P_22	AJ10	
22	IO_L18N_22	AH10	
22	IO_L19P_22	AD11	
22	IO_L19N_22	AE11	
23	IO_L0P_23	C20	LX50, LX85
23	IO_L0N_23	B20	LX50, LX85
23	IO_L1P_23	B21	LX50, LX85
23	IO_L1N_23	A21	LX50, LX85
23	IO_L2P_23	C19	LX50, LX85
23	IO_L2N_23	C18	LX50, LX85
23	IO_L3P_23	C22	LX50, LX85
23	IO_L3N_23	B22	LX50, LX85
23	IO_L4P_23	B18	LX50, LX85
23	IO_L4N_VREF_23	A18	LX50, LX85
23	IO_L5P_23	C23	LX50, LX85
23	IO_L5N_23	B23	LX50, LX85
23	IO_L6P_23	A19	LX50, LX85
23	IO_L6N_23	A20	LX50, LX85
23	IO_L7P_23	A23	LX50, LX85
23	IO_L7N_23	A24	LX50, LX85
23	IO_L8P_CC_23	C24	LX50, LX85
23	IO_L8N_CC_23 (2)	D25	LX50, LX85
23	IO_L9P_CC_23	B26	LX50, LX85
23	IO_L9N_CC_23 (2)	A25	LX50, LX85
23	IO_L10P_CC_23	B27	LX50, LX85
23	IO_L10N_CC_23 (2)	A26	LX50, LX85
23	IO_L11P_CC_23	B25	LX50, LX85
23	IO_L11N_CC_23 (2)	C25	LX50, LX85

Table 2-6: **FF1153 Package—LX50, LX85, LX110, and LX155 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
23	IO_L12P_VRN_23	C29	LX50, LX85
23	IO_L12N_VRP_23	B28	LX50, LX85
23	IO_L13P_23	D26	LX50, LX85
23	IO_L13N_23	C27	LX50, LX85
23	IO_L14P_23	A29	LX50, LX85
23	IO_L14N_VREF_23	A28	LX50, LX85
23	IO_L15P_23	C28	LX50, LX85
23	IO_L15N_23	D27	LX50, LX85
23	IO_L16P_23	B31	LX50, LX85
23	IO_L16N_23	A31	LX50, LX85
23	IO_L17P_23	C30	LX50, LX85
23	IO_L17N_23	D29	LX50, LX85
23	IO_L18P_23	D31	LX50, LX85
23	IO_L18N_23	D30	LX50, LX85
23	IO_L19P_23	A30	LX50, LX85
23	IO_L19N_23	B30	LX50, LX85
24	IO_L0P_24	A15	LX50, LX85
24	IO_L0N_24	A14	LX50, LX85
24	IO_L1P_24	C14	LX50, LX85
24	IO_L1N_24	C13	LX50, LX85
24	IO_L2P_24	B15	LX50, LX85
24	IO_L2N_24	C15	LX50, LX85
24	IO_L3P_24	B13	LX50, LX85
24	IO_L3N_24	A13	LX50, LX85
24	IO_L4P_24	B16	LX50, LX85
24	IO_L4N_VREF_24	A16	LX50, LX85
24	IO_L5P_24	B12	LX50, LX85
24	IO_L5N_24	C12	LX50, LX85
24	IO_L6P_24	B17	LX50, LX85
24	IO_L6N_24	C17	LX50, LX85
24	IO_L7P_24	A11	LX50, LX85
24	IO_L7N_24	B11	LX50, LX85
24	IO_L8P_CC_24	D11	LX50, LX85

Table 2-6: **FF1153 Package—LX50, LX85, LX110, and LX155 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
24	IO_L8N_CC_24 (2)	D10	LX50, LX85
24	IO_L9P_CC_24	A10	LX50, LX85
24	IO_L9N_CC_24 (2)	A9	LX50, LX85
24	IO_L10P_CC_24	B8	LX50, LX85
24	IO_L10N_CC_24 (2)	A8	LX50, LX85
24	IO_L11P_CC_24	B10	LX50, LX85
24	IO_L11N_CC_24 (2)	C10	LX50, LX85
24	IO_L12P_VRN_24	A5	LX50, LX85
24	IO_L12N_VRP_24	A6	LX50, LX85
24	IO_L13P_24	B6	LX50, LX85
24	IO_L13N_24	B7	LX50, LX85
24	IO_L14P_24	B5	LX50, LX85
24	IO_L14N_VREF_24	A4	LX50, LX85
24	IO_L15P_24	C8	LX50, LX85
24	IO_L15N_24	C7	LX50, LX85
24	IO_L16P_24	C4	LX50, LX85
24	IO_L16N_24	C5	LX50, LX85
24	IO_L17P_24	D9	LX50, LX85
24	IO_L17N_24	C9	LX50, LX85
24	IO_L18P_24	D5	LX50, LX85
24	IO_L18N_24	D4	LX50, LX85
24	IO_L19P_24	D6	LX50, LX85
24	IO_L19N_24	D7	LX50, LX85
25	IO_L0P_25	AL29	LX50, LX85
25	IO_L0N_25	AL30	LX50, LX85
25	IO_L1P_25	AM31	LX50, LX85
25	IO_L1N_25	AL31	LX50, LX85
25	IO_L2P_25	AN30	LX50, LX85
25	IO_L2N_25	AM30	LX50, LX85
25	IO_L3P_25	AP30	LX50, LX85
25	IO_L3N_25	AP31	LX50, LX85
25	IO_L4P_25	AM27	LX50, LX85
25	IO_L4N_VREF_25	AL28	LX50, LX85

Table 2-6: **FF1153 Package—LX50, LX85, LX110, and LX155 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
25	IO_L5P_25	AP29	LX50, LX85
25	IO_L5N_25	AN29	LX50, LX85
25	IO_L6P_25	AP27	LX50, LX85
25	IO_L6N_25	AN27	LX50, LX85
25	IO_L7P_25	AN28	LX50, LX85
25	IO_L7N_25	AM28	LX50, LX85
25	IO_L8P_CC_25	AN25	LX50, LX85
25	IO_L8N_CC_25 (2)	AM25	LX50, LX85
25	IO_L9P_CC_25	AM26	LX50, LX85
25	IO_L9N_CC_25 (2)	AL26	LX50, LX85
25	IO_L10P_CC_25	AP26	LX50, LX85
25	IO_L10N_CC_25 (2)	AP25	LX50, LX85
25	IO_L11P_CC_25	AL25	LX50, LX85
25	IO_L11N_CC_25 (2)	AL24	LX50, LX85
25	IO_L12P_VRN_25	AN24	LX50, LX85
25	IO_L12N_VRP_25	AP24	LX50, LX85
25	IO_L13P_25	AM21	LX50, LX85
25	IO_L13N_25	AM20	LX50, LX85
25	IO_L14P_25	AN23	LX50, LX85
25	IO_L14N_VREF_25	AM23	LX50, LX85
25	IO_L15P_25	AN20	LX50, LX85
25	IO_L15N_25	AP20	LX50, LX85
25	IO_L16P_25	AN22	LX50, LX85
25	IO_L16N_25	AM22	LX50, LX85
25	IO_L17P_25	AN18	LX50, LX85
25	IO_L17N_25	AM18	LX50, LX85
25	IO_L18P_25	AP22	LX50, LX85
25	IO_L18N_25	AP21	LX50, LX85
25	IO_L19P_25	AN19	LX50, LX85
25	IO_L19N_25	AP19	LX50, LX85
26	IO_L0P_26	AL5	LX50, LX85
26	IO_L0N_26	AL6	LX50, LX85
26	IO_L1P_26	AN5	LX50, LX85

Table 2-6: **FF1153 Package—LX50, LX85, LX110, and LX155 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
26	IO_L1N_26	AN4	LX50, LX85
26	IO_L2P_26	AM5	LX50, LX85
26	IO_L2N_26	AL4	LX50, LX85
26	IO_L3P_26	AP5	LX50, LX85
26	IO_L3N_26	AP4	LX50, LX85
26	IO_L4P_26	AL8	LX50, LX85
26	IO_L4N_VREF_26	AL9	LX50, LX85
26	IO_L5P_26	AN7	LX50, LX85
26	IO_L5N_26	AM6	LX50, LX85
26	IO_L6P_26	AM8	LX50, LX85
26	IO_L6N_26	AM7	LX50, LX85
26	IO_L7P_26	AN9	LX50, LX85
26	IO_L7N_26	AN8	LX50, LX85
26	IO_L8P_CC_26	AM10	LX50, LX85
26	IO_L8N_CC_26 (2)	AL10	LX50, LX85
26	IO_L9P_CC_26	AP7	LX50, LX85
26	IO_L9N_CC_26 (2)	AP6	LX50, LX85
26	IO_L10P_CC_26	AP9	LX50, LX85
26	IO_L10N_CC_26 (2)	AP10	LX50, LX85
26	IO_L11P_CC_26	AN10	LX50, LX85
26	IO_L11N_CC_26 (2)	AM11	LX50, LX85
26	IO_L12P_VRN_26	AM12	LX50, LX85
26	IO_L12N_VRP_26	AN12	LX50, LX85
26	IO_L13P_26	AN17	LX50, LX85
26	IO_L13N_26	AM17	LX50, LX85
26	IO_L14P_26	AN13	LX50, LX85
26	IO_L14N_VREF_26	AM13	LX50, LX85
26	IO_L15P_26	AP16	LX50, LX85
26	IO_L15N_26	AP17	LX50, LX85
26	IO_L16P_26	AP11	LX50, LX85
26	IO_L16N_26	AP12	LX50, LX85
26	IO_L17P_26	AM15	LX50, LX85
26	IO_L17N_26	AM16	LX50, LX85

Table 2-6: **FF1153 Package—LX50, LX85, LX110, and LX155 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
26	IO_L18P_26	AP14	LX50, LX85
26	IO_L18N_26	AN14	LX50, LX85
26	IO_L19P_26	AP15	LX50, LX85
26	IO_L19N_26	AN15	LX50, LX85
NA	GND	A1	
NA	GND	A12	
NA	GND	A17	
NA	GND	A2	
NA	GND	A22	
NA	GND	A27	
NA	GND	A32	
NA	GND	A7	
NA	GND	AA15	
NA	GND	AA17	
NA	GND	AA19	
NA	GND	AA2	
NA	GND	AA21	
NA	GND	AA23	
NA	GND	AA27	
NA	GND	AA7	
NA	GND	AB12	
NA	GND	AB14	
NA	GND	AB16	
NA	GND	AB18	
NA	GND	AB20	
NA	GND	AB22	
NA	GND	AB24	
NA	GND	AB34	
NA	GND	AB4	
NA	GND	AC1	
NA	GND	AC11	
NA	GND	AC17	
NA	GND	AC21	

Table 2-6: **FF1153 Package—LX50, LX85, LX110, and LX155 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	AC26	
NA	GND	AC31	
NA	GND	AD12	
NA	GND	AD18	
NA	GND	AD28	
NA	GND	AD8	
NA	GND	AE10	
NA	GND	AE15	
NA	GND	AE20	
NA	GND	AE25	
NA	GND	AE5	
NA	GND	AF12	
NA	GND	AF2	
NA	GND	AF22	
NA	GND	AF32	
NA	GND	AG19	
NA	GND	AG29	
NA	GND	AG34	
NA	GND	AG9	
NA	GND	AH1	
NA	GND	AH16	
NA	GND	AH26	
NA	GND	AH6	
NA	GND	AJ13	
NA	GND	AJ23	
NA	GND	AJ3	
NA	GND	AJ33	
NA	GND	AK10	
NA	GND	AK20	
NA	GND	AK30	
NA	GND	AL17	
NA	GND	AL2	
NA	GND	AL27	

Table 2-6: **FF1153 Package—LX50, LX85, LX110, and LX155 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	AL7	
NA	GND	AM14	
NA	GND	AM24	
NA	GND	AM34	
NA	GND	AM4	
NA	GND	AN1	
NA	GND	AN11	
NA	GND	AN21	
NA	GND	AN26	
NA	GND	AN31	
NA	GND	AP13	
NA	GND	AP18	
NA	GND	AP23	
NA	GND	AP28	
NA	GND	AP3	
NA	GND	AP33	
NA	GND	AP8	
NA	GND	B14	
NA	GND	B24	
NA	GND	B34	
NA	GND	B4	
NA	GND	C1	
NA	GND	C11	
NA	GND	C21	
NA	GND	C31	
NA	GND	D18	
NA	GND	D28	
NA	GND	D3	
NA	GND	D33	
NA	GND	D8	
NA	GND	E15	
NA	GND	E25	
NA	GND	E5	

Table 2-6: **FF1153 Package—LX50, LX85, LX110, and LX155 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	F12	
NA	GND	F2	
NA	GND	F22	
NA	GND	F32	
NA	GND	G19	
NA	GND	G29	
NA	GND	G34	
NA	GND	G9	
NA	GND	H1	
NA	GND	H11	
NA	GND	H16	
NA	GND	H26	
NA	GND	H6	
NA	GND	J13	
NA	GND	J18	
NA	GND	J23	
NA	GND	J28	
NA	GND	J3	
NA	GND	J33	
NA	GND	K10	
NA	GND	K15	
NA	GND	K20	
NA	GND	K25	
NA	GND	K30	
NA	GND	L17	
NA	GND	L2	
NA	GND	L22	
NA	GND	L27	
NA	GND	L7	
NA	GND	M12	
NA	GND	M14	
NA	GND	M16	
NA	GND	M18	

Table 2-6: **FF1153 Package—LX50, LX85, LX110, and LX155 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	M20	
NA	GND	M24	
NA	GND	M34	
NA	GND	M4	
NA	GND	M9	
NA	GND	N1	
NA	GND	N11	
NA	GND	N15	
NA	GND	N17	
NA	GND	N19	
NA	GND	N21	
NA	GND	N26	
NA	GND	N31	
NA	GND	P12	
NA	GND	P14	
NA	GND	P16	
NA	GND	P18	
NA	GND	P20	
NA	GND	P28	
NA	GND	P8	
NA	GND	R10	
NA	GND	R13	
NA	GND	R15	
NA	GND	R17	
NA	GND	R19	
NA	GND	R21	
NA	GND	R23	
NA	GND	R25	
NA	GND	R5	
NA	GND	T12	
NA	GND	T14	
NA	GND	T16	
NA	GND	T2	

Table 2-6: **FF1153 Package—LX50, LX85, LX110, and LX155 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	T20	
NA	GND	T22	
NA	GND	T27	
NA	GND	T32	
NA	GND	U13	
NA	GND	U15	
NA	GND	U19	
NA	GND	U21	
NA	GND	U23	
NA	GND	U29	
NA	GND	U34	
NA	GND	U9	
NA	GND	V1	
NA	GND	V12	
NA	GND	V14	
NA	GND	V16	
NA	GND	V20	
NA	GND	V22	
NA	GND	V26	
NA	GND	V6	
NA	GND	W13	
NA	GND	W15	
NA	GND	W19	
NA	GND	W21	
NA	GND	W23	
NA	GND	W3	
NA	GND	W33	
NA	GND	Y10	
NA	GND	Y12	
NA	GND	Y14	
NA	GND	Y16	
NA	GND	Y18	
NA	GND	Y20	

Table 2-6: **FF1153 Package—LX50, LX85, LX110, and LX155 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	Y22	
NA	GND	Y25	
NA	GND	Y30	
NA	VCCAUX	AA12	
NA	VCCAUX	AC12	
NA	VCCAUX	AD23	
NA	VCCAUX	L12	
NA	VCCAUX	N12	
NA	VCCAUX	P23	
NA	VCCAUX	R12	
NA	VCCAUX	T23	
NA	VCCAUX	U24	
NA	VCCAUX	V11	
NA	VCCAUX	V23	
NA	VCCAUX	Y23	
NA	VCCINT	AA14	
NA	VCCINT	AA16	
NA	VCCINT	AA18	
NA	VCCINT	AA20	
NA	VCCINT	AA22	
NA	VCCINT	AB15	
NA	VCCINT	AB17	
NA	VCCINT	AB19	
NA	VCCINT	AB21	
NA	VCCINT	AC16	
NA	VCCINT	AC18	
NA	VCCINT	AD17	
NA	VCCINT	L18	
NA	VCCINT	M15	
NA	VCCINT	M17	
NA	VCCINT	M19	
NA	VCCINT	M21	
NA	VCCINT	N16	

Table 2-6: **FF1153 Package—LX50, LX85, LX110, and LX155 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	VCCINT	N18	
NA	VCCINT	N20	
NA	VCCINT	P13	
NA	VCCINT	P15	
NA	VCCINT	P17	
NA	VCCINT	P19	
NA	VCCINT	P21	
NA	VCCINT	R14	
NA	VCCINT	R16	
NA	VCCINT	R18	
NA	VCCINT	R20	
NA	VCCINT	R22	
NA	VCCINT	T13	
NA	VCCINT	T15	
NA	VCCINT	T19	
NA	VCCINT	T21	
NA	VCCINT	U12	
NA	VCCINT	U14	
NA	VCCINT	U16	
NA	VCCINT	U20	
NA	VCCINT	U22	
NA	VCCINT	V13	
NA	VCCINT	V15	
NA	VCCINT	V19	
NA	VCCINT	V21	
NA	VCCINT	W12	
NA	VCCINT	W14	
NA	VCCINT	W16	
NA	VCCINT	W20	
NA	VCCINT	W22	
NA	VCCINT	Y13	
NA	VCCINT	Y15	
NA	VCCINT	Y17	

Table 2-6: **FF1153 Package—LX50, LX85, LX110, and LX155 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	VCCINT	Y19	
NA	VCCINT	Y21	
0	VCCO_0	AD13	
0	VCCO_0	AG14	
1	VCCO_1	D13	
1	VCCO_1	G14	
11	VCCO_11	P33	
11	VCCO_11	R30	
11	VCCO_11	V31	
12	VCCO_12	T7	
12	VCCO_12	U4	
12	VCCO_12	W8	
13	VCCO_13	AA32	
13	VCCO_13	AB29	
13	VCCO_13	W28	
14	VCCO_14	AB9	
14	VCCO_14	AC6	
14	VCCO_14	Y5	
15	VCCO_15	H31	
15	VCCO_15	L32	
15	VCCO_15	M29	
16	VCCO_16	K5	
16	VCCO_16	N6	
16	VCCO_16	P3	
17	VCCO_17	AD33	
17	VCCO_17	AE30	
17	VCCO_17	AH31	
18	VCCO_18	AD3	
18	VCCO_18	AF7	
18	VCCO_18	AG4	
19	VCCO_19	B29	
19	VCCO_19	E30	
19	VCCO_19	F27	

Table 2-6: **FF1153 Package—LX50, LX85, LX110, and LX155 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
2	VCCO_2	AH21	
2	VCCO_2	AL22	
20	VCCO_20	F7	
20	VCCO_20	G4	
20	VCCO_20	J8	
21	VCCO_21	AJ28	
21	VCCO_21	AL32	
21	VCCO_21	AM29	
22	VCCO_22	AJ8	
22	VCCO_22	AK5	
22	VCCO_22	AN6	
23	VCCO_23	C26	
23	VCCO_23	D23	
23	VCCO_23	G24	
24	VCCO_24	B9	
24	VCCO_24	C6	
24	VCCO_24	E10	
25	VCCO_25	AF27	
25	VCCO_25	AG24	
25	VCCO_25	AK25	
26	VCCO_26	AH11	
26	VCCO_26	AL12	
26	VCCO_26	AM9	
3	VCCO_3	E20	
3	VCCO_3	H21	
4	VCCO_4	AF17	
4	VCCO_4	AK15	
5	VCCO_5	B19	
5	VCCO_5	C16	
5	VCCO_5	F17	
6	VCCO_6	AJ18	
6	VCCO_6	AM19	

Table 2-6: **FF1153 Package—LX50, LX85, LX110, and LX155 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
6	VCCO_6	AN16	

Notes:

1. Do not connect a single ended clock to the N-side of the differential clock pair of pins, for example IO_L3N_GC_3.
2. Do not connect a single-ended clock to the N-side of clock capable pins, for example, IO_L8N_CC_11.
3. RSVD pins must be tied to GND (logic 0).

FF1156 Package—TX150T

Table 2-7: **FF1156 Package—TX150T**

Bank	Pin Description	Pin Number	No Connect (NC)
0	DXP_0	W18	
0	DXN_0	W17	
0	AVDD_0	T18	
0	AVSS_0	T17	
0	VP_0	U18	
0	VN_0	V17	
0	VREFP_0	V18	
0	VREFN_0	U17	
0	VBATT_0	P24	
0	PROGRAM_B_0	U26	
0	HSWAPEN_0	T26	
0	D_IN_0	K11	
0	DONE_0	L11	
0	CCLK_0	M10	
0	INIT_B_0	L10	
0	CS_B_0	AA25	
0	RDWR_B_0	T25	
0	RSVD_0(3)	AC24	
0	RSVD_0(3)	AC23	
0	TCK_0	AB10	
0	M0_0	AB20	
0	M2_0	AC20	
0	M1_0	AD20	
0	TMS_0	AC10	
0	TDI_0	AC9	
0	D_OUT_BUSY_0	AD10	
0	TDO_0	AD9	
1	IO_L0P_A19_1	K17	
1	IO_L0N_A18_1	J16	
1	IO_L1P_A17_1	H15	
1	IO_L1N_A16_1	J15	

Table 2-7: **FF1156 Package—TX150T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
1	IO_L2P_A15_D31_1	L16	
1	IO_L2N_A14_D30_1	K16	
1	IO_L3P_A13_D29_1	M15	
1	IO_L3N_A12_D28_1	N15	
1	IO_L4P_A11_D27_1	M16	
1	IO_L4N_VREF_A10_D26_1	L15	
1	IO_L5P_A9_D25_1	L14	
1	IO_L5N_A8_D24_1	L13	
1	IO_L6P_A7_D23_1	M17	
1	IO_L6N_A6_D22_1	L18	
1	IO_L7P_A5_D21_1	M11	
1	IO_L7N_A4_D20_1	M12	
1	IO_L8P_CC_A3_D19_1	M18	
1	IO_L8N_CC_A2_D18_1 (2)	N17	
1	IO_L9P_CC_A1_D17_1	M13	
1	IO_L9N_CC_A0_D16_1 (2)	N13	
2	IO_L0P_CC_RS1_2	AC14	
2	IO_L0N_CC_RS0_2 (2)	AD14	
2	IO_L1P_CC_A25_2	AE19	
2	IO_L1N_CC_A24_2 (2)	AD19	
2	IO_L2P_A23_2	AE13	
2	IO_L2N_A22_2	AF14	
2	IO_L3P_A21_2	AE18	
2	IO_L3N_A20_2	AE17	
2	IO_L4P_FCS_B_2	AE14	
2	IO_L4N_VREF_FOE_B_MOSI_2	AF15	
2	IO_L5P_FWE_B_2	AE16	
2	IO_L5N_CSO_B_2	AF16	
2	IO_L6P_D7_2	AD15	
2	IO_L6N_D6_2	AD16	
2	IO_L7P_D5_2	AC17	
2	IO_L7N_D4_2	AD17	
2	IO_L8P_D3_2	AC15	

Table 2-7: **FF1156 Package—TX150T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
2	IO_L8N_D2_FS2_2	AB16	
2	IO_L9P_D1_FS1_2	AB18	
2	IO_L9N_D0_FS0_2	AC19	
3	IO_L0P_CC_GC_3	G17	
3	IO_L0N_CC_GC_3 (1)(2)	H17	
3	IO_L1P_CC_GC_3	B18	
3	IO_L1N_CC_GC_3 (1)(2)	C18	
3	IO_L2P_GC_VRN_3	D17	
3	IO_L2N_GC_VRP_3 (1)	E17	
3	IO_L3P_GC_3	E18	
3	IO_L3N_GC_3 (1)	E19	
3	IO_L4P_GC_3	B17	
3	IO_L4N_GC_VREF_3 (1)	C17	
3	IO_L5P_GC_3	F18	
3	IO_L5N_GC_3 (1)	G18	
3	IO_L6P_GC_3	F16	
3	IO_L6N_GC_3 (1)	G16	
3	IO_L7P_GC_3	H18	
3	IO_L7N_GC_3 (1)	J17	
3	IO_L8P_GC_3	E16	
3	IO_L8N_GC_3 (1)	F15	
3	IO_L9P_GC_3	K18	
3	IO_L9N_GC_3 (1)	L19	
4	IO_L0P_GC_D15_4	AG18	
4	IO_L0N_GC_D14_4 (1)	AH18	
4	IO_L1P_GC_D13_4	AG13	
4	IO_L1N_GC_D12_4 (1)	AF13	
4	IO_L2P_GC_D11_4	AK18	
4	IO_L2N_GC_D10_4 (1)	AL18	
4	IO_L3P_GC_D9_4	AH13	
4	IO_L3N_GC_D8_4 (1)	AG12	
4	IO_L4P_GC_4	AK17	
4	IO_L4N_GC_VREF_4 (1)	AK16	

Table 2-7: **FF1156 Package—TX150T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
4	IO_L5P_GC_4	AJ14	
4	IO_L5N_GC_4 (1)	AH14	
4	IO_L6P_GC_4	AJ17	
4	IO_L6N_GC_4 (1)	AH17	
4	IO_L7P_GC_VRN_4	AH15	
4	IO_L7N_GC_VRP_4 (1)	AG15	
4	IO_L8P_CC_GC_4	AG17	
4	IO_L8N_CC_GC_4 (1)(2)	AG16	
4	IO_L9P_CC_GC_4	AJ16	
4	IO_L9N_CC_GC_4 (1)(2)	AJ15	
11	IO_L0P_11	AD25	
11	IO_L0N_11	AE26	
11	IO_L1P_11	AF28	
11	IO_L1N_11	AE27	
11	IO_L2P_11	AD26	
11	IO_L2N_11	AD27	
11	IO_L3P_11	AC28	
11	IO_L3N_11	AB28	
11	IO_L4P_11	W27	
11	IO_L4N_VREF_11	V27	
11	IO_L5P_11	AE28	
11	IO_L5N_11	AD29	
11	IO_L6P_11	Y28	
11	IO_L6N_11	Y27	
11	IO_L7P_11	AA28	
11	IO_L7N_11	AA29	
11	IO_L8P_CC_11	U25	
11	IO_L8N_CC_11 (2)	V25	
11	IO_L9P_CC_11	AG28	
11	IO_L9N_CC_11 (2)	AH29	
11	IO_L10P_CC_SM15P_11	AF29	
11	IO_L10N_CC_SM15N_11 (2)	AE29	
11	IO_L11P_CC_SM14P_11	AB27	

Table 2-7: **FF1156 Package—TX150T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
11	IO_L11N_CC_SM14N_11 (2)	AC27	
11	IO_L12P_VRN_11	AD30	
11	IO_L12N_VRP_11	AC29	
11	IO_L13P_11	AA26	
11	IO_L13N_11	AB26	
11	IO_L14P_11	AB30	
11	IO_L14N_VREF_11	AC30	
11	IO_L15P_SM13P_11	AB25	
11	IO_L15N_SM13N_11	AC25	
11	IO_L16P_SM12P_11	W29	
11	IO_L16N_SM12N_11	Y29	
11	IO_L17P_SM11P_11	Y26	
11	IO_L17N_SM11N_11	W26	
11	IO_L18P_SM10P_11	Y24	
11	IO_L18N_SM10N_11	W24	
11	IO_L19P_SM9P_11	V24	
11	IO_L19N_SM9N_11	W25	
12	IO_L0P_12	F9	
12	IO_L0N_12	F8	
12	IO_L1P_12	J11	
12	IO_L1N_12	J10	
12	IO_L2P_12	F10	
12	IO_L2N_12	G10	
12	IO_L3P_12	H10	
12	IO_L3N_12	H9	
12	IO_L4P_12	F11	
12	IO_L4N_VREF_12	E11	
12	IO_L5P_12	G8	
12	IO_L5N_12	H8	
12	IO_L6P_12	G12	
12	IO_L6N_12	G11	
12	IO_L7P_12	F6	
12	IO_L7N_12	G6	

Table 2-7: **FF1156 Package—TX150T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
12	IO_L8P_CC_12	K12	
12	IO_L8N_CC_12(2)	J12	
12	IO_L9P_CC_12	H7	
12	IO_L9N_CC_12(2)	J7	
12	IO_L10P_CC_12	K8	
12	IO_L10N_CC_12(2)	J9	
12	IO_L11P_CC_12	H12	
12	IO_L11N_CC_12(2)	G13	
12	IO_L12P_VRN_12	K6	
12	IO_L12N_VRP_12	J6	
12	IO_L13P_12	F13	
12	IO_L13N_12	F14	
12	IO_L14P_12	L8	
12	IO_L14N_VREF_12	K9	
12	IO_L15P_12	G15	
12	IO_L15N_12	H14	
12	IO_L16P_12	M8	
12	IO_L16N_12	L9	
12	IO_L17P_12	H13	
12	IO_L17N_12	J14	
12	IO_L18P_12	L6	
12	IO_L18N_12	K7	
12	IO_L19P_12	K13	
12	IO_L19N_12	K14	
13	IO_L0P_SM8P_13	AF26	
13	IO_L0N_SM8N_13	AG27	
13	IO_L1P_SM7P_13	AD21	
13	IO_L1N_SM7N_13	AE21	
13	IO_L2P_SM6P_13	AG26	
13	IO_L2N_SM6N_13	AH27	
13	IO_L3P_SM5P_13	AD22	
13	IO_L3N_SM5N_13	AE22	
13	IO_L4P_13	AH28	

Table 2-7: **FF1156 Package—TX150T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
13	IO_L4N_VREF_13	AJ27	
13	IO_L5P_SM4P_13	AF19	
13	IO_L5N_SM4N_13	AF18	
13	IO_L6P_SM3P_13	AJ25	
13	IO_L6N_SM3N_13	AK26	
13	IO_L7P_SM2P_13	AH20	
13	IO_L7N_SM2N_13	AH19	
13	IO_L8P_CC_SM1P_13	AE24	
13	IO_L8N_CC_SM1N_13 (2)	AF25	
13	IO_L9P_CC_SM0P_13	AK19	
13	IO_L9N_CC_SM0N_13 (2)	AJ19	
13	IO_L10P_CC_13	AF20	
13	IO_L10N_CC_13 (2)	AG20	
13	IO_L11P_CC_13	AJ24	
13	IO_L11N_CC_13 (2)	AK24	
13	IO_L12P_VRN_13	AJ20	
13	IO_L12N_VRP_13	AJ21	
13	IO_L13P_13	AH25	
13	IO_L13N_13	AG25	
13	IO_L14P_13	AF21	
13	IO_L14N_VREF_13	AG21	
13	IO_L15P_13	AH23	
13	IO_L15N_13	AH24	
13	IO_L16P_13	AE23	
13	IO_L16N_13	AD24	
13	IO_L17P_13	AG22	
13	IO_L17N_13	AG23	
13	IO_L18P_13	AF24	
13	IO_L18N_13	AF23	
13	IO_L19P_13	AJ22	
13	IO_L19N_13	AH22	
14	IO_L0P_14	AB8	
14	IO_L0N_14	AA8	

Table 2-7: **FF1156 Package—TX150T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
14	IO_L1P_14	T9	
14	IO_L1N_14	T10	
14	IO_L2P_14	AA6	
14	IO_L2N_14	Y6	
14	IO_L3P_14	V10	
14	IO_L3N_14	U10	
14	IO_L4P_14	Y7	
14	IO_L4N_VREF_14	W7	
14	IO_L5P_14	V8	
14	IO_L5N_14	V9	
14	IO_L6P_14	W6	
14	IO_L6N_14	V7	
14	IO_L7P_14	U8	
14	IO_L7N_14	T8	
14	IO_L8P_CC_14	AA10	
14	IO_L8N_CC_14 (2)	AA9	
14	IO_L9P_CC_14	R8	
14	IO_L9N_CC_14 (2)	R9	
14	IO_L10P_CC_14	W9	
14	IO_L10N_CC_14 (2)	W10	
14	IO_L11P_CC_14	U7	
14	IO_L11N_CC_14 (2)	U6	
14	IO_L12P_VRN_14	P9	
14	IO_L12N_VRP_14	N9	
14	IO_L13P_14	R6	
14	IO_L13N_14	T6	
14	IO_L14P_14	P10	
14	IO_L14N_VREF_14	N10	
14	IO_L15P_14	R7	
14	IO_L15N_14	P6	
14	IO_L16P_14	N8	
14	IO_L16N_14	P7	
14	IO_L17P_14	L5	

Table 2-7: **FF1156 Package—TX150T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
14	IO_L17N_14	M5	
14	IO_L18P_14	M7	
14	IO_L18N_14	M6	
14	IO_L19P_14	Y8	
14	IO_L19N_14	Y9	
23	IO_L0P_23	F28	
23	IO_L0N_23	G28	
23	IO_L1P_23	P25	
23	IO_L1N_23	R26	
23	IO_L2P_23	G27	
23	IO_L2N_23	H27	
23	IO_L3P_23	N25	
23	IO_L3N_23	P26	
23	IO_L4P_23	J26	
23	IO_L4N_VREF_23	J27	
23	IO_L5P_23	R28	
23	IO_L5N_23	P27	
23	IO_L6P_23	H28	
23	IO_L6N_23	H29	
23	IO_L7P_23	U28	
23	IO_L7N_23	U27	
23	IO_L8P_CC_23	J29	
23	IO_L8N_CC_23 (2)	K29	
23	IO_L9P_CC_23	V29	
23	IO_L9N_CC_23 (2)	V28	
23	IO_L10P_CC_23	R27	
23	IO_L10N_CC_23 (2)	T28	
23	IO_L11P_CC_23	L26	
23	IO_L11N_CC_23 (2)	K26	
23	IO_L12P_VRN_23	N27	
23	IO_L12N_VRP_23	N28	
23	IO_L13P_23	K28	
23	IO_L13N_23	K27	

Table 2-7: **FF1156 Package—TX150T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
23	IO_L14P_23	M26	
23	IO_L14N_VREF_23	M25	
23	IO_L15P_23	L29	
23	IO_L15N_23	L28	
23	IO_L16P_23	T29	
23	IO_L16N_23	R29	
23	IO_L17P_23	M30	
23	IO_L17N_23	L30	
23	IO_L18P_23	P29	
23	IO_L18N_23	N29	
23	IO_L19P_23	M27	
23	IO_L19N_23	M28	
26	IO_L0P_26	AD7	
26	IO_L0N_26	AE7	
26	IO_L1P_26	AE6	
26	IO_L1N_26	AF6	
26	IO_L2P_26	AD5	
26	IO_L2N_26	AD6	
26	IO_L3P_26	AG6	
26	IO_L3N_26	AG7	
26	IO_L4P_26	AC8	
26	IO_L4N_VREF_26	AC7	
26	IO_L5P_26	AE8	
26	IO_L5N_26	AF8	
26	IO_L6P_26	AB5	
26	IO_L6N_26	AC5	
26	IO_L7P_26	AE9	
26	IO_L7N_26	AF9	
26	IO_L8P_CC_26	AB6	
26	IO_L8N_CC_26 (2)	AB7	
26	IO_L9P_CC_26	AF10	
26	IO_L9N_CC_26 (2)	AG10	
26	IO_L10P_CC_26	AH8	

Table 2-7: **FF1156 Package—TX150T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
26	IO_L10N_CC_26 (2)	AG8	
26	IO_L11P_CC_26	AD12	
26	IO_L11N_CC_26 (2)	AC12	
26	IO_L12P_VRN_26	AJ7	
26	IO_L12N_VRP_26	AH7	
26	IO_L13P_26	AJ12	
26	IO_L13N_26	AH12	
26	IO_L14P_26	AJ10	
26	IO_L14N_VREF_26	AH9	
26	IO_L15P_26	AJ11	
26	IO_L15N_26	AK11	
26	IO_L16P_26	AE11	
26	IO_L16N_26	AF11	
26	IO_L17P_26	AJ9	
26	IO_L17N_26	AK9	
26	IO_L18P_26	AD11	
26	IO_L18N_26	AE12	
26	IO_L19P_26	AH10	
26	IO_L19N_26	AG11	
27	IO_L0P_27	H24	
27	IO_L0N_27	H23	
27	IO_L1P_27	G22	
27	IO_L1N_27	H22	
27	IO_L2P_27	F21	
27	IO_L2N_27	G21	
27	IO_L3P_27	H19	
27	IO_L3N_27	G20	
27	IO_L4P_27	F19	
27	IO_L4N_VREF_27	F20	
27	IO_L5P_27	J20	
27	IO_L5N_27	H20	
27	IO_L6P_27	G23	
27	IO_L6N_27	F23	

Table 2-7: **FF1156 Package—TX150T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
27	IO_L7P_27	K19	
27	IO_L7N_27	J19	
27	IO_L8P_CC_27	F24	
27	IO_L8N_CC_27(2)	E24	
27	IO_L9P_CC_27	M20	
27	IO_L9N_CC_27(2)	L20	
27	IO_L10P_CC_27	J21	
27	IO_L10N_CC_27(2)	K21	
27	IO_L11P_CC_27	G25	
27	IO_L11N_CC_27(2)	F25	
27	IO_L12P_VRN_27	J22	
27	IO_L12N_VRP_27	K22	
27	IO_L13P_27	G26	
27	IO_L13N_27	F26	
27	IO_L14P_27	L23	
27	IO_L14N_VREF_27	K23	
27	IO_L15P_27	J25	
27	IO_L15N_27	H25	
27	IO_L16P_27	L21	
27	IO_L16N_27	M21	
27	IO_L17P_27	K24	
27	IO_L17N_27	J24	
27	IO_L18P_27	N22	
27	IO_L18N_27	M22	
27	IO_L19P_27	L24	
27	IO_L19N_27	L25	
NA	MGTTXP0_111	M33	
NA	MGTAVTTTX_111	U32	
NA	MGTTXN0_111	N33	
NA	MGTAVCC_111	R32	
NA	MGTRXP0_111	N34	
NA	MGTAVTTRX_111	N32	
NA	MGTRXN0_111	P34	

Table 2-7: **FF1156 Package—TX150T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	MGTAVCCPLL_111	T32	
NA	MGTRXN1_111	R34	
NA	MGTREFCLKN_111	P32	
NA	MGTRXP1_111	T34	
NA	MGTREFCLKP_111	P31	
NA	MGTTXN1_111	T33	
NA	MGTTXP1_111	U33	
NA	MGTAVTTRXC_L	U31	
NA	MGTRREF_111	V31	
NA	MGTTXP0_112	M2	
NA	MGTAVTTTX_112	U3	
NA	MGTTXN0_112	N2	
NA	MGTAVCC_112	R3	
NA	MGTRXP0_112	N1	
NA	MGTAVTTRX_112	N3	
NA	MGTRXN0_112	P1	
NA	MGTAVCCPLL_112	T3	
NA	MGTRXN1_112	R1	
NA	MGTREFCLKN_112	P3	
NA	MGTRXP1_112	T1	
NA	MGTREFCLKP_112	P4	
NA	MGTTXN1_112	T2	
NA	MGTTXP1_112	U2	
NA	MGTAVTTRXC_R	U4	
NA	MGTRREF_112	V4	
NA	MGTTXP0_113	V33	
NA	MGTAVTTTX_113	AC32	
NA	MGTTXN0_113	W33	
NA	MGTAVCC_113	AA32	
NA	MGTRXP0_113	W34	
NA	MGTAVTTRX_113	W32	
NA	MGTRXN0_113	Y34	
NA	MGTAVCCPLL_113	AB32	

Table 2-7: **FF1156 Package—TX150T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	MGTRXN1_113	AA34	
NA	MGTREFCLKN_113	Y32	
NA	MGTRXP1_113	AB34	
NA	MGTREFCLKP_113	Y31	
NA	MGTTXN1_113	AB33	
NA	MGTTXP1_113	AC33	
NA	MGTTXP0_114	V2	
NA	MGTAVTTTX_114	AC3	
NA	MGTTXN0_114	W2	
NA	MGTAVCC_114	AA3	
NA	MGTRXP0_114	W1	
NA	MGTAVTTRX_114	W3	
NA	MGTRXN0_114	Y1	
NA	MGTAVCCPLL_114	AB3	
NA	MGTRXN1_114	AA1	
NA	MGTREFCLKN_114	Y3	
NA	MGTRXP1_114	AB1	
NA	MGTREFCLKP_114	Y4	
NA	MGTTXN1_114	AB2	
NA	MGTTXP1_114	AC2	
NA	MGTTXP0_115	F33	
NA	MGTAVTTTX_115	L32	
NA	MGTTXN0_115	G33	
NA	MGTAVCC_115	J32	
NA	MGTRXP0_115	G34	
NA	MGTAVTTRX_115	G32	
NA	MGTRXN0_115	H34	
NA	MGTAVCCPLL_115	K32	
NA	MGTRXN1_115	J34	
NA	MGTREFCLKN_115	H32	
NA	MGTRXP1_115	K34	
NA	MGTREFCLKP_115	H31	
NA	MGTTXN1_115	K33	

Table 2-7: **FF1156 Package—TX150T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	MGTTXP1_115	L33	
NA	MGTTXP0_116	F2	
NA	MGTAVTTTX_116	L3	
NA	MGTTXN0_116	G2	
NA	MGTAVCC_116	J3	
NA	MGTRXP0_116	G1	
NA	MGTAVTTRX_116	G3	
NA	MGTRXN0_116	H1	
NA	MGTAVCCPLL_116	K3	
NA	MGTRXN1_116	J1	
NA	MGTREFCLKN_116	H3	
NA	MGTRXP1_116	K1	
NA	MGTREFCLKP_116	H4	
NA	MGTTXN1_116	K2	
NA	MGTTXP1_116	L2	
NA	MGTTXP0_117	AD33	
NA	MGTAVTTTX_117	AJ32	
NA	MGTTXN0_117	AE33	
NA	MGTAVCC_117	AG32	
NA	MGTRXP0_117	AE34	
NA	MGTAVTTRX_117	AE32	
NA	MGTRXN0_117	AF34	
NA	MGTAVCCPLL_117	AH32	
NA	MGTRXN1_117	AG34	
NA	MGTREFCLKN_117	AF32	
NA	MGTRXP1_117	AH34	
NA	MGTREFCLKP_117	AF31	
NA	MGTTXN1_117	AH33	
NA	MGTTXP1_117	AJ33	
NA	MGTTXP0_118	AD2	
NA	MGTAVTTTX_118	AJ3	
NA	MGTTXN0_118	AE2	
NA	MGTAVCC_118	AG3	

Table 2-7: **FF1156 Package—TX150T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	MGTRXP0_118	AE1	
NA	MGTAVTTRX_118	AE3	
NA	MGTRXN0_118	AF1	
NA	MGTAVCCPLL_118	AH3	
NA	MGTRXN1_118	AG1	
NA	MGTREFCLKN_118	AF3	
NA	MGTRXP1_118	AH1	
NA	MGTREFCLKP_118	AF4	
NA	MGTTXN1_118	AH2	
NA	MGTTXP1_118	AJ2	
NA	MGTTXP0_119	B32	
NA	MGTAVTTTX_119	E32	
NA	MGTTXN0_119	B33	
NA	MGTAVCC_119	D31	
NA	MGTRXP0_119	A33	
NA	MGTAVTTRX_119	C32	
NA	MGTRXN0_119	A34	
NA	MGTAVCCPLL_119	D32	
NA	MGTRXN1_119	C34	
NA	MGTREFCLKN_119	E31	
NA	MGTRXP1_119	D34	
NA	MGTREFCLKP_119	F31	
NA	MGTTXN1_119	D33	
NA	MGTTXP1_119	E33	
NA	MGTTXP0_120	B3	
NA	MGTAVTTTX_120	E3	
NA	MGTTXN0_120	B2	
NA	MGTAVCC_120	D4	
NA	MGTRXP0_120	A2	
NA	MGTAVTTRX_120	C3	
NA	MGTRXN0_120	A1	
NA	MGTAVCCPLL_120	D3	
NA	MGTRXN1_120	C1	

Table 2-7: **FF1156 Package—TX150T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	MGTREFCLKN_120	E4	
NA	MGTRXP1_120	D1	
NA	MGTREFCLKP_120	F4	
NA	MGTTXN1_120	D2	
NA	MGTTXP1_120	E2	
NA	MGTTXP0_121	AK33	
NA	MGTAVTTTX_121	AM32	
NA	MGTTXN0_121	AL33	
NA	MGTAVCC_121	AL31	
NA	MGTRXP0_121	AL34	
NA	MGTAVTTRX_121	AL32	
NA	MGTRXN0_121	AM34	
NA	MGTAVCCPLL_121	AM31	
NA	MGTRXN1_121	AP34	
NA	MGTREFCLKN_121	AL30	
NA	MGTRXP1_121	AP33	
NA	MGTREFCLKP_121	AK30	
NA	MGTTXN1_121	AN33	
NA	MGTTXP1_121	AN32	
NA	MGTTXP0_122	AK2	
NA	MGTAVTTTX_122	AM3	
NA	MGTTXN0_122	AL2	
NA	MGTAVCC_122	AL4	
NA	MGTRXP0_122	AL1	
NA	MGTAVTTRX_122	AL3	
NA	MGTRXN0_122	AM1	
NA	MGTAVCCPLL_122	AM4	
NA	MGTRXN1_122	AP1	
NA	MGTREFCLKN_122	AL5	
NA	MGTRXP1_122	AP2	
NA	MGTREFCLKP_122	AK5	
NA	MGTTXN1_122	AN2	
NA	MGTTXP1_122	AN3	

Table 2-7: **FF1156 Package—TX150T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	MGTTXP0_123	B26	
NA	MGTAVTTTX_123	C30	
NA	MGTTXN0_123	B27	
NA	MGTAVCC_123	C27	
NA	MGTRXP0_123	A27	
NA	MGTAVTTRX_123	C26	
NA	MGTRXN0_123	A28	
NA	MGTAVCCPLL_123	C29	
NA	MGTRXN1_123	A29	
NA	MGTREFCLKN_123	D28	
NA	MGTRXP1_123	A30	
NA	MGTREFCLKP_123	D27	
NA	MGTTXN1_123	B30	
NA	MGTTXP1_123	B31	
NA	MGTTXP0_124	B9	
NA	MGTAVTTTX_124	C5	
NA	MGTTXN0_124	B8	
NA	MGTAVCC_124	C8	
NA	MGTRXP0_124	A8	
NA	MGTAVTTRX_124	C9	
NA	MGTRXN0_124	A7	
NA	MGTAVCCPLL_124	C6	
NA	MGTRXN1_124	A6	
NA	MGTREFCLKN_124	D7	
NA	MGTRXP1_124	A5	
NA	MGTREFCLKP_124	D8	
NA	MGTTXN1_124	B5	
NA	MGTTXP1_124	B4	
NA	MGTTXP0_125	AN31	
NA	MGTAVTTTX_125	AM25	
NA	MGTTXN0_125	AN30	
NA	MGTAVCC_125	AM27	
NA	MGTRXP0_125	AP30	

Table 2-7: **FF1156 Package—TX150T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	MGTAVTTRX_125	AM29	
NA	MGTRXN0_125	AP29	
NA	MGTAVCCPLL_125	AM26	
NA	MGTRXN1_125	AP28	
NA	MGTREFCLKN_125	AM28	
NA	MGTRXP1_125	AP27	
NA	MGTREFCLKP_125	AL28	
NA	MGTTXN1_125	AN27	
NA	MGTTXP1_125	AN26	
NA	MGTTXP0_126	AN4	
NA	MGTAVTTTX_126	AM10	
NA	MGTTXN0_126	AN5	
NA	MGTAVCC_126	AM8	
NA	MGTRXP0_126	AP5	
NA	MGTAVTTRX_126	AM6	
NA	MGTRXN0_126	AP6	
NA	MGTAVCCPLL_126	AM9	
NA	MGTRXN1_126	AP7	
NA	MGTREFCLKN_126	AM7	
NA	MGTRXP1_126	AP8	
NA	MGTREFCLKP_126	AL7	
NA	MGTTXN1_126	AN8	
NA	MGTTXP1_126	AN9	
NA	MGTTXP0_127	B20	
NA	MGTAVTTTX_127	C24	
NA	MGTTXN0_127	B21	
NA	MGTAVCC_127	C21	
NA	MGTRXP0_127	A21	
NA	MGTAVTTRX_127	C20	
NA	MGTRXN0_127	A22	
NA	MGTAVCCPLL_127	C23	
NA	MGTRXN1_127	A23	
NA	MGTREFCLKN_127	D22	

Table 2-7: **FF1156 Package—TX150T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	MGTRXP1_127	A24	
NA	MGTREFCLKP_127	D21	
NA	MGTTXN1_127	B24	
NA	MGTTXP1_127	B25	
NA	MGTTXP0_128	B15	
NA	MGTAVTTTX_128	C11	
NA	MGTTXN0_128	B14	
NA	MGTAVCC_128	C14	
NA	MGTRXP0_128	A14	
NA	MGTAVTTRX_128	C15	
NA	MGTRXN0_128	A13	
NA	MGTAVCCPLL_128	C12	
NA	MGTRXN1_128	A12	
NA	MGTREFCLKN_128	D13	
NA	MGTRXP1_128	A11	
NA	MGTREFCLKP_128	D14	
NA	MGTTXN1_128	B11	
NA	MGTTXP1_128	B10	
NA	MGTTXP0_129	AN25	
NA	MGTAVTTTX_129	AP19	
NA	MGTTXN0_129	AN24	
NA	MGTAVCC_129	AM21	
NA	MGTRXP0_129	AP24	
NA	MGTAVTTRX_129	AM23	
NA	MGTRXN0_129	AP23	
NA	MGTAVCCPLL_129	AM20	
NA	MGTRXN1_129	AP22	
NA	MGTREFCLKN_129	AM22	
NA	MGTRXP1_129	AP21	
NA	MGTREFCLKP_129	AL22	
NA	MGTTXN1_129	AN21	
NA	MGTTXP1_129	AN20	
NA	MGTTXP0_130	AN10	

Table 2-7: **FF1156 Package—TX150T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	MGTAVTTTX_130	AP16	
NA	MGTTXN0_130	AN11	
NA	MGTAVCC_130	AM14	
NA	MGTRXP0_130	AP11	
NA	MGTAVTTRX_130	AM12	
NA	MGTRXN0_130	AP12	
NA	MGTAVCCPLL_130	AM15	
NA	MGTRXN1_130	AP13	
NA	MGTREFCLKN_130	AM13	
NA	MGTRXP1_130	AP14	
NA	MGTREFCLKP_130	AL13	
NA	MGTTXN1_130	AN14	
NA	MGTTXP1_130	AN15	
NA	GND	A3	
NA	GND	A4	
NA	GND	A9	
NA	GND	A10	
NA	GND	A15	
NA	GND	A16	
NA	GND	A17	
NA	GND	A19	
NA	GND	A20	
NA	GND	A25	
NA	GND	A26	
NA	GND	A31	
NA	GND	A32	
NA	GND	AA2	
NA	GND	AA4	
NA	GND	AA5	
NA	GND	AA7	
NA	GND	AA11	
NA	GND	AA13	
NA	GND	AA15	

Table 2-7: **FF1156 Package—TX150T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	AA17	
NA	GND	AA19	
NA	GND	AA21	
NA	GND	AA23	
NA	GND	AA27	
NA	GND	AA30	
NA	GND	AA31	
NA	GND	AA33	
NA	GND	AB4	
NA	GND	AB9	
NA	GND	AB14	
NA	GND	AB22	
NA	GND	AB24	
NA	GND	AB31	
NA	GND	AC1	
NA	GND	AC4	
NA	GND	AC11	
NA	GND	AC13	
NA	GND	AC21	
NA	GND	AC31	
NA	GND	AC34	
NA	GND	AD1	
NA	GND	AD3	
NA	GND	AD4	
NA	GND	AD8	
NA	GND	AD18	
NA	GND	AD23	
NA	GND	AD28	
NA	GND	AD31	
NA	GND	AD32	
NA	GND	AD34	
NA	GND	AE4	
NA	GND	AE5	

Table 2-7: **FF1156 Package—TX150T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	AE15	
NA	GND	AE25	
NA	GND	AE30	
NA	GND	AE31	
NA	GND	AF2	
NA	GND	AF5	
NA	GND	AF12	
NA	GND	AF22	
NA	GND	AF30	
NA	GND	AF33	
NA	GND	AG2	
NA	GND	AG4	
NA	GND	AG5	
NA	GND	AG9	
NA	GND	AG19	
NA	GND	AG29	
NA	GND	AG30	
NA	GND	AG31	
NA	GND	AG33	
NA	GND	AH4	
NA	GND	AH5	
NA	GND	AH6	
NA	GND	AH16	
NA	GND	AH26	
NA	GND	AH30	
NA	GND	AH31	
NA	GND	AJ1	
NA	GND	AJ4	
NA	GND	AJ5	
NA	GND	AJ6	
NA	GND	AJ8	
NA	GND	AJ13	
NA	GND	AJ23	

Table 2-7: **FF1156 Package—TX150T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	AJ28	
NA	GND	AJ29	
NA	GND	AJ30	
NA	GND	AJ31	
NA	GND	AJ34	
NA	GND	AK1	
NA	GND	AK3	
NA	GND	AK4	
NA	GND	AK6	
NA	GND	AK7	
NA	GND	AK8	
NA	GND	AK10	
NA	GND	AK12	
NA	GND	AK13	
NA	GND	AK14	
NA	GND	AK15	
NA	GND	AK20	
NA	GND	AK21	
NA	GND	AK22	
NA	GND	AK23	
NA	GND	AK25	
NA	GND	AK27	
NA	GND	AK28	
NA	GND	AK29	
NA	GND	AK31	
NA	GND	AK32	
NA	GND	AK34	
NA	GND	AL6	
NA	GND	AL8	
NA	GND	AL9	
NA	GND	AL10	
NA	GND	AL11	
NA	GND	AL12	

Table 2-7: **FF1156 Package—TX150T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	AL14	
NA	GND	AL15	
NA	GND	AL16	
NA	GND	AL17	
NA	GND	AL19	
NA	GND	AL20	
NA	GND	AL21	
NA	GND	AL23	
NA	GND	AL24	
NA	GND	AL25	
NA	GND	AL26	
NA	GND	AL27	
NA	GND	AL29	
NA	GND	AM2	
NA	GND	AM5	
NA	GND	AM11	
NA	GND	AM16	
NA	GND	AM17	
NA	GND	AM18	
NA	GND	AM19	
NA	GND	AM24	
NA	GND	AM30	
NA	GND	AM33	
NA	GND	AN1	
NA	GND	AN6	
NA	GND	AN7	
NA	GND	AN12	
NA	GND	AN13	
NA	GND	AN16	
NA	GND	AN17	
NA	GND	AN18	
NA	GND	AN19	
NA	GND	AN22	

Table 2-7: **FF1156 Package—TX150T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	AN23	
NA	GND	AN28	
NA	GND	AN29	
NA	GND	AN34	
NA	GND	AP3	
NA	GND	AP4	
NA	GND	AP9	
NA	GND	AP10	
NA	GND	AP15	
NA	GND	AP17	
NA	GND	AP18	
NA	GND	AP20	
NA	GND	AP25	
NA	GND	AP26	
NA	GND	AP31	
NA	GND	AP32	
NA	GND	B1	
NA	GND	B6	
NA	GND	B7	
NA	GND	B12	
NA	GND	B13	
NA	GND	B16	
NA	GND	B19	
NA	GND	B22	
NA	GND	B23	
NA	GND	B28	
NA	GND	B29	
NA	GND	B34	
NA	GND	C2	
NA	GND	C4	
NA	GND	C7	
NA	GND	C10	
NA	GND	C13	

Table 2-7: **FF1156 Package—TX150T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	C16	
NA	GND	C19	
NA	GND	C22	
NA	GND	C25	
NA	GND	C28	
NA	GND	C31	
NA	GND	C33	
NA	GND	D5	
NA	GND	D6	
NA	GND	D9	
NA	GND	D10	
NA	GND	D11	
NA	GND	D12	
NA	GND	D15	
NA	GND	D16	
NA	GND	D18	
NA	GND	D19	
NA	GND	D20	
NA	GND	D23	
NA	GND	D24	
NA	GND	D25	
NA	GND	D26	
NA	GND	D29	
NA	GND	D30	
NA	GND	E1	
NA	GND	E5	
NA	GND	E6	
NA	GND	E7	
NA	GND	E8	
NA	GND	E9	
NA	GND	E10	
NA	GND	E12	
NA	GND	E13	

Table 2-7: **FF1156 Package—TX150T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	E14	
NA	GND	E15	
NA	GND	E20	
NA	GND	E21	
NA	GND	E22	
NA	GND	E23	
NA	GND	E25	
NA	GND	E26	
NA	GND	E27	
NA	GND	E28	
NA	GND	E29	
NA	GND	E30	
NA	GND	E34	
NA	GND	F1	
NA	GND	F3	
NA	GND	F5	
NA	GND	F7	
NA	GND	F12	
NA	GND	F22	
NA	GND	F27	
NA	GND	F29	
NA	GND	F30	
NA	GND	F32	
NA	GND	F34	
NA	GND	G4	
NA	GND	G5	
NA	GND	G9	
NA	GND	G19	
NA	GND	G29	
NA	GND	G30	
NA	GND	G31	
NA	GND	H2	
NA	GND	H5	

Table 2-7: **FF1156 Package—TX150T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	H6	
NA	GND	H16	
NA	GND	H26	
NA	GND	H30	
NA	GND	H33	
NA	GND	J2	
NA	GND	J4	
NA	GND	J5	
NA	GND	J13	
NA	GND	J23	
NA	GND	J30	
NA	GND	J31	
NA	GND	J33	
NA	GND	K4	
NA	GND	K5	
NA	GND	K10	
NA	GND	K20	
NA	GND	K30	
NA	GND	K31	
NA	GND	L1	
NA	GND	L4	
NA	GND	L7	
NA	GND	L17	
NA	GND	L27	
NA	GND	L31	
NA	GND	L34	
NA	GND	M1	
NA	GND	M3	
NA	GND	M4	
NA	GND	M9	
NA	GND	M14	
NA	GND	M24	
NA	GND	M31	

Table 2-7: **FF1156 Package—TX150T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	M32	
NA	GND	M34	
NA	GND	N4	
NA	GND	N5	
NA	GND	N6	
NA	GND	N11	
NA	GND	N19	
NA	GND	N21	
NA	GND	N23	
NA	GND	N30	
NA	GND	N31	
NA	GND	P2	
NA	GND	P5	
NA	GND	P8	
NA	GND	P12	
NA	GND	P14	
NA	GND	P16	
NA	GND	P18	
NA	GND	P20	
NA	GND	P22	
NA	GND	P28	
NA	GND	P30	
NA	GND	P33	
NA	GND	R2	
NA	GND	R4	
NA	GND	R5	
NA	GND	R11	
NA	GND	R13	
NA	GND	R15	
NA	GND	R17	
NA	GND	R19	
NA	GND	R21	
NA	GND	R23	

Table 2-7: **FF1156 Package—TX150T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	R25	
NA	GND	R30	
NA	GND	R31	
NA	GND	R33	
NA	GND	T4	
NA	GND	T5	
NA	GND	T12	
NA	GND	T14	
NA	GND	T16	
NA	GND	T20	
NA	GND	T22	
NA	GND	T24	
NA	GND	T30	
NA	GND	T31	
NA	GND	U1	
NA	GND	U5	
NA	GND	U9	
NA	GND	U11	
NA	GND	U13	
NA	GND	U15	
NA	GND	U19	
NA	GND	U21	
NA	GND	U23	
NA	GND	U29	
NA	GND	U30	
NA	GND	U34	
NA	GND	V1	
NA	GND	V3	
NA	GND	V5	
NA	GND	V6	
NA	GND	V12	
NA	GND	V14	
NA	GND	V16	

Table 2-7: **FF1156 Package—TX150T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	V20	
NA	GND	V22	
NA	GND	V26	
NA	GND	V30	
NA	GND	V32	
NA	GND	V34	
NA	GND	W4	
NA	GND	W5	
NA	GND	W11	
NA	GND	W13	
NA	GND	W15	
NA	GND	W19	
NA	GND	W21	
NA	GND	W23	
NA	GND	W28	
NA	GND	W30	
NA	GND	W31	
NA	GND	Y2	
NA	GND	Y5	
NA	GND	Y10	
NA	GND	Y12	
NA	GND	Y14	
NA	GND	Y16	
NA	GND	Y18	
NA	GND	Y20	
NA	GND	Y22	
NA	GND	Y30	
NA	GND	Y33	
0	VCCO_0	AC22	
0	VCCO_0	M19	
1	VCCO_1	K15	
1	VCCO_1	L12	
1	VCCO_1	N16	

Table 2-7: **FF1156 Package—TX150T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
2	VCCO_2	AB19	
2	VCCO_2	AC16	
2	VCCO_2	AD13	
3	VCCO_3	A18	
3	VCCO_3	F17	
3	VCCO_3	J18	
4	VCCO_4	AF17	
4	VCCO_4	AG14	
4	VCCO_4	AJ18	
11	VCCO_11	AB29	
11	VCCO_11	AC26	
11	VCCO_11	AF27	
11	VCCO_11	Y25	
12	VCCO_12	G7	
12	VCCO_12	G14	
12	VCCO_12	H11	
12	VCCO_12	J8	
13	VCCO_13	AE20	
13	VCCO_13	AG24	
13	VCCO_13	AH21	
13	VCCO_13	AJ26	
14	VCCO_14	N7	
14	VCCO_14	R10	
14	VCCO_14	T7	
14	VCCO_14	W8	
23	VCCO_23	J28	
23	VCCO_23	M29	
23	VCCO_23	N26	
23	VCCO_23	T27	
26	VCCO_26	AC6	
26	VCCO_26	AE10	
26	VCCO_26	AF7	
26	VCCO_26	AH11	

Table 2-7: **FF1156 Package—TX150T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
27	VCCO_27	G24	
27	VCCO_27	H21	
27	VCCO_27	K25	
27	VCCO_27	L22	
NA	VCCAUX	P23	
NA	VCCAUX	AB11	
NA	VCCAUX	T23	
NA	VCCAUX	M23	
NA	VCCAUX	N12	
NA	VCCAUX	N24	
NA	VCCAUX	P11	
NA	VCCAUX	R24	
NA	VCCAUX	T11	
NA	VCCAUX	U24	
NA	VCCAUX	V11	
NA	VCCAUX	Y11	
NA	VCCINT	AA12	
NA	VCCINT	AA14	
NA	VCCINT	AA16	
NA	VCCINT	AA18	
NA	VCCINT	AA20	
NA	VCCINT	AA22	
NA	VCCINT	AB15	
NA	VCCINT	AB17	
NA	VCCINT	AB21	
NA	VCCINT	AC18	
NA	VCCINT	N14	
NA	VCCINT	N18	
NA	VCCINT	N20	
NA	VCCINT	P13	
NA	VCCINT	P15	
NA	VCCINT	P17	
NA	VCCINT	P19	

Table 2-7: **FF1156 Package—TX150T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	VCCINT	P21	
NA	VCCINT	AA24	
NA	VCCINT	R12	
NA	VCCINT	R14	
NA	VCCINT	R16	
NA	VCCINT	R18	
NA	VCCINT	R20	
NA	VCCINT	R22	
NA	VCCINT	T13	
NA	VCCINT	T15	
NA	VCCINT	T19	
NA	VCCINT	T21	
NA	VCCINT	AB23	
NA	VCCINT	U12	
NA	VCCINT	U14	
NA	VCCINT	U16	
NA	VCCINT	U20	
NA	VCCINT	U22	
NA	VCCINT	V13	
NA	VCCINT	V15	
NA	VCCINT	V19	
NA	VCCINT	V21	
NA	VCCINT	V23	
NA	VCCINT	W12	
NA	VCCINT	W14	
NA	VCCINT	W16	
NA	VCCINT	W20	
NA	VCCINT	W22	
NA	VCCINT	Y13	
NA	VCCINT	Y15	
NA	VCCINT	Y17	
NA	VCCINT	Y19	
NA	VCCINT	Y21	

Table 2-7: **FF1156 Package—TX150T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	VCCINT	Y23	
NA	RSVD(3)	AB12	
NA	RSVD(3)	AB13	

Notes:

1. Do not connect a single-ended clock to the N-side of the differential clock pair of pins, for example, IO_L3N_GC_3.
2. Do not connect a single-ended clock to the N-side of clock capable pins, for example, IO_L8N_CC_11.
3. RSVD pins must be tied to GND (logic 0).

FF1738 Package—FX100T, LX110T, FX130T, LX155T, FX200T, LX220T, SX240T, and LX330T

Table 2-8: **FF1738 Package—FX100T, LX110T, FX130T, LX155T, FX200T, LX220T, SX240T, and LX330T**

Bank	Pin Description	Pin Number	No Connect (NC)
0	DXP_0	AC22	
0	DXN_0	AC21	
0	AVDD_0	Y22	
0	AVSS_0	Y21	
0	VP_0	AA22	
0	VN_0	AB21	
0	VREFP_0	AB22	
0	VREFN_0	AA21	
0	VBATT_0	P30	
0	PROGRAM_B_0	R29	
0	HSWAPEN_0	P15	
0	D_IN_0	R15	
0	DONE_0	R14	
0	CCLK_0	AH14	
0	INIT_B_0	T14	
0	CS_B_0	T30	
0	RDWR_B_0	R30	
0	RSVD(3)	V31	
0	RSVD(3)	AF30	
0	TCK_0	AG29	
0	M0_0	AH29	
0	M2_0	AJ28	
0	M1_0	AH30	
0	TMS_0	AH15	
0	TDI_0	AH16	
0	D_OUT_BUSY_0	AJ16	
0	TDO_0	AJ15	
1	IO_L0P_A19_1	N25	
1	IO_L0N_A18_1	P25	
1	IO_L1P_A17_1	P18	

Table 2-8: **FF1738 Package—FX100T, LX110T, FX130T, LX155T, FX200T, LX220T, SX240T, and LX330T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
1	IO_L1N_A16_1	P17	
1	IO_L2P_A15_D31_1	P26	
1	IO_L2N_A14_D30_1	N26	
1	IO_L3P_A13_D29_1	M16	
1	IO_L3N_A12_D28_1	N16	
1	IO_L4P_A11_D27_1	P27	
1	IO_L4N_VREF_A10_D26_1	P28	
1	IO_L5P_A9_D25_1	N15	
1	IO_L5N_A8_D24_1	N14	
1	IO_L6P_A7_D23_1	N28	
1	IO_L6N_A6_D22_1	N29	
1	IO_L7P_A5_D21_1	M14	
1	IO_L7N_A4_D20_1	M13	
1	IO_L8P_CC_A3_D19_1	N30	
1	IO_L8N_CC_A2_D18_1 (2)	M29	
1	IO_L9P_CC_A1_D17_1	N13	
1	IO_L9N_CC_A0_D16_1 (2)	P13	
2	IO_L0P_CC_RS1_2	AK12	
2	IO_L0N_CC_RS0_2 (2)	AK13	
2	IO_L1P_CC_A25_2	AJ30	
2	IO_L1N_CC_A24_2 (2)	AK30	
2	IO_L2P_A23_2	AK15	
2	IO_L2N_A22_2	AK14	
2	IO_L3P_A21_2	AL30	
2	IO_L3N_A20_2	AM29	
2	IO_L4P_FCS_B_2	AL14	
2	IO_L4N_VREF_FOE_B_MOSI_2	AM13	
2	IO_L5P_FWE_B_2	AM28	
2	IO_L5N_CSO_B_2	AL29	
2	IO_L6P_D7_2	AN13	
2	IO_L6N_D6_2	AP13	
2	IO_L7P_D5_2	AK28	

Table 2-8: **FF1738 Package—FX100T, LX110T, FX130T, LX155T, FX200T, LX220T, SX240T, and LX330T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
2	IO_L7N_D4_2	AK29	
2	IO_L8P_D3_2	AN14	
2	IO_L8N_D2_FS2_2	AM14	
2	IO_L9P_D1_FS1_2	AK27	
2	IO_L9N_D0_FS0_2	AJ26	
3	IO_L0P_CC_GC_3	J16	
3	IO_L0N_CC_GC_3 (1)(2)	J15	
3	IO_L1P_CC_GC_3	M26	
3	IO_L1N_CC_GC_3 (1)(2)	L27	
3	IO_L2P_GC_VRN_3	J17	
3	IO_L2N_GC_VRP_3 (1)	K17	
3	IO_L3P_GC_3	M27	
3	IO_L3N_GC_3 (1)	M28	
3	IO_L4P_GC_3	L17	
3	IO_L4N_GC_VREF_3 (1)	M17	
3	IO_L5P_GC_3	L29	
3	IO_L5N_GC_3 (1)	K28	
3	IO_L6P_GC_3	L16	
3	IO_L6N_GC_3 (1)	L15	
3	IO_L7P_GC_3	K29	
3	IO_L7N_GC_3 (1)	J30	
3	IO_L8P_GC_3	L14	
3	IO_L8N_GC_3 (1)	K15	
3	IO_L9P_GC_3	K30	
3	IO_L9N_GC_3 (1)	L30	
4	IO_L0P_GC_D15_4	AN30	
4	IO_L0N_GC_D14_4 (1)	AP30	
4	IO_L1P_GC_D13_4	AK17	
4	IO_L1N_GC_D12_4 (1)	AL17	
4	IO_L2P_GC_D11_4	AN29	
4	IO_L2N_GC_D10_4 (1)	AP28	
4	IO_L3P_GC_D9_4	AL15	

Table 2-8: **FF1738 Package—FX100T, LX110T, FX130T, LX155T, FX200T, LX220T, SX240T, and LX330T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
4	IO_L3N_GC_D8_4 (1)	AL16	
4	IO_L4P_GC_4	AP27	
4	IO_L4N_GC_VREF_4 (1)	AN28	
4	IO_L5P_GC_4	AM16	
4	IO_L5N_GC_4 (1)	AM17	
4	IO_L6P_GC_4	AM27	
4	IO_L6N_GC_4 (1)	AM26	
4	IO_L7P_GC_VRN_4	AN15	
4	IO_L7N_GC_VRP_4 (1)	AN16	
4	IO_L8P_CC_GC_4	AL27	
4	IO_L8N_CC_GC_4 (1)(2)	AL26	
4	IO_L9P_CC_GC_4	AP16	
4	IO_L9N_CC_GC_4 (1)(2)	AP15	
5	IO_L0P_5	L24	
5	IO_L0N_5	M24	
5	IO_L1P_5	E18	
5	IO_L1N_5	E17	
5	IO_L2P_5	K24	
5	IO_L2N_5	L25	
5	IO_L3P_5	F16	
5	IO_L3N_5	F17	
5	IO_L4P_5	K25	
5	IO_L4N_VREF_5	J25	
5	IO_L5P_5	G16	
5	IO_L5N_5	H16	
5	IO_L6P_5	H26	
5	IO_L6N_5	J26	
5	IO_L7P_5	G18	
5	IO_L7N_5	G17	
5	IO_L8P_CC_5	J28	
5	IO_L8N_CC_5 (2)	J27	
5	IO_L9P_CC_5	J18	

Table 2-8: **FF1738 Package—FX100T, LX110T, FX130T, LX155T, FX200T, LX220T, SX240T, and LX330T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
5	IO_L9N_CC_5 (2)	H18	
5	IO_L10P_CC_5	K18	
5	IO_L10N_CC_5 (2)	K19	
5	IO_L11P_CC_5	K27	
5	IO_L11N_CC_5 (2)	L26	
5	IO_L12P_VRN_5	N20	
5	IO_L12N_VRP_5	P20	
5	IO_L13P_5	G27	
5	IO_L13N_5	F27	
5	IO_L14P_5	M19	
5	IO_L14N_VREF_5	N19	
5	IO_L15P_5	G28	
5	IO_L15N_5	H28	
5	IO_L16P_5	M18	
5	IO_L16N_5	N18	
5	IO_L17P_5	G29	
5	IO_L17N_5	F29	
5	IO_L18P_5	L20	
5	IO_L18N_5	L19	
5	IO_L19P_5	H29	
5	IO_L19N_5	H30	
6	IO_L0P_6	AR29	
6	IO_L0N_6	AR28	
6	IO_L1P_6	AT14	
6	IO_L1N_6	AR14	
6	IO_L2P_6	AR30	
6	IO_L2N_6	AT30	
6	IO_L3P_6	AT15	
6	IO_L3N_6	AR15	
6	IO_L4P_6	AT29	
6	IO_L4N_VREF_6	AU29	
6	IO_L5P_6	AT17	

Table 2-8: **FF1738 Package—FX100T, LX110T, FX130T, LX155T, FX200T, LX220T, SX240T, and LX330T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
6	IO_L5N_6	AT16	
6	IO_L6P_6	AU28	
6	IO_L6N_6	AT27	
6	IO_L7P_6	AP17	
6	IO_L7N_6	AR17	
6	IO_L8P_CC_6	AT26	
6	IO_L8N_CC_6 (2)	AR27	
6	IO_L9P_CC_6	AN20	
6	IO_L9N_CC_6 (2)	AN19	
6	IO_L10P_CC_6	AN18	
6	IO_L10N_CC_6 (2)	AM18	
6	IO_L11P_CC_6	AN26	
6	IO_L11N_CC_6 (2)	AP26	
6	IO_L12P_VRN_6	AR18	
6	IO_L12N_VRP_6	AP18	
6	IO_L13P_6	AN25	
6	IO_L13N_6	AP25	
6	IO_L14P_6	AT19	
6	IO_L14N_VREF_6	AR19	
6	IO_L15P_6	AM24	
6	IO_L15N_6	AN24	
6	IO_L16P_6	AK18	
6	IO_L16N_6	AK19	
6	IO_L17P_6	AK24	
6	IO_L17N_6	AK25	
6	IO_L18P_6	AM19	
6	IO_L18N_6	AL19	
6	IO_L19P_6	AL25	
6	IO_L19N_6	AL24	
7	IO_L0P_7	M23	FX100T, LX110T, LX155T, LX220T
7	IO_L0N_7	M22	FX100T, LX110T, LX155T, LX220T

Table 2-8: **FF1738 Package—FX100T, LX110T, FX130T, LX155T, FX200T, LX220T, SX240T, and LX330T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
7	IO_L1P_7	M21	FX100T, LX110T, LX155T, LX220T
7	IO_L1N_7	L21	FX100T, LX110T, LX155T, LX220T
7	IO_L2P_7	N24	FX100T, LX110T, LX155T, LX220T
7	IO_L2N_7	N23	FX100T, LX110T, LX155T, LX220T
7	IO_L3P_7	N22	FX100T, LX110T, LX155T, LX220T
7	IO_L3N_7	N21	FX100T, LX110T, LX155T, LX220T
7	IO_L4P_7	H21	FX100T, LX110T, LX155T, LX220T
7	IO_L4N_VREF_7	J21	FX100T, LX110T, LX155T, LX220T
7	IO_L5P_7	J20	FX100T, LX110T, LX155T, LX220T
7	IO_L5N_7	K20	FX100T, LX110T, LX155T, LX220T
7	IO_L6P_7	L22	FX100T, LX110T, LX155T, LX220T
7	IO_L6N_7	K23	FX100T, LX110T, LX155T, LX220T
7	IO_L7P_7	K22	FX100T, LX110T, LX155T, LX220T
7	IO_L7N_7	J22	FX100T, LX110T, LX155T, LX220T
7	IO_L8P_CC_7	F22	FX100T, LX110T, LX155T, LX220T
7	IO_L8N_CC_7 (2)	G22	FX100T, LX110T, LX155T, LX220T
7	IO_L9P_CC_7	G21	FX100T, LX110T, LX155T, LX220T
7	IO_L9N_CC_7 (2)	F21	FX100T, LX110T, LX155T, LX220T
7	IO_L10P_CC_7	E22	FX100T, LX110T, LX155T, LX220T
7	IO_L10N_CC_7 (2)	E23	FX100T, LX110T, LX155T, LX220T

Table 2-8: **FF1738 Package—FX100T, LX110T, FX130T, LX155T, FX200T, LX220T, SX240T, and LX330T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
7	IO_L11P_CC_7	F24	FX100T, LX110T, LX155T, LX220T
7	IO_L11N_CC_7 (2)	G23	FX100T, LX110T, LX155T, LX220T
7	IO_L12P_VRN_7	E19	FX100T, LX110T, LX155T, LX220T
7	IO_L12N_VRP_7	D18	FX100T, LX110T, LX155T, LX220T
7	IO_L13P_7	J23	FX100T, LX110T, LX155T, LX220T
7	IO_L13N_7	H23	FX100T, LX110T, LX155T, LX220T
7	IO_L14P_7	E20	FX100T, LX110T, LX155T, LX220T
7	IO_L14N_VREF_7	F20	FX100T, LX110T, LX155T, LX220T
7	IO_L15P_7	G24	FX100T, LX110T, LX155T, LX220T
7	IO_L15N_7	H24	FX100T, LX110T, LX155T, LX220T
7	IO_L16P_7	F19	FX100T, LX110T, LX155T, LX220T
7	IO_L16N_7	G19	FX100T, LX110T, LX155T, LX220T
7	IO_L17P_7	F26	FX100T, LX110T, LX155T, LX220T
7	IO_L17N_7	F25	FX100T, LX110T, LX155T, LX220T
7	IO_L18P_7	H19	FX100T, LX110T, LX155T, LX220T
7	IO_L18N_7	H20	FX100T, LX110T, LX155T, LX220T
7	IO_L19P_7	H25	FX100T, LX110T, LX155T, LX220T
7	IO_L19N_7	G26	FX100T, LX110T, LX155T, LX220T
8	IO_L0P_8	AL21	FX100T, LX110T, LX155T, LX220T
8	IO_L0N_8	AL22	FX100T, LX110T, LX155T, LX220T

Table 2-8: **FF1738 Package—FX100T, LX110T, FX130T, LX155T, FX200T, LX220T, SX240T, and LX330T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
8	IO_L1P_8	AK23	FX100T, LX110T, LX155T, LX220T
8	IO_L1N_8	AK22	FX100T, LX110T, LX155T, LX220T
8	IO_L2P_8	AJ22	FX100T, LX110T, LX155T, LX220T
8	IO_L2N_8	AJ21	FX100T, LX110T, LX155T, LX220T
8	IO_L3P_8	AK20	FX100T, LX110T, LX155T, LX220T
8	IO_L3N_8	AL20	FX100T, LX110T, LX155T, LX220T
8	IO_L4P_8	AU26	FX100T, LX110T, LX155T, LX220T
8	IO_L4N_VREF_8	AU27	FX100T, LX110T, LX155T, LX220T
8	IO_L5P_8	AU19	FX100T, LX110T, LX155T, LX220T
8	IO_L5N_8	AU18	FX100T, LX110T, LX155T, LX220T
8	IO_L6P_8	AR25	FX100T, LX110T, LX155T, LX220T
8	IO_L6N_8	AT25	FX100T, LX110T, LX155T, LX220T
8	IO_L7P_8	AR20	FX100T, LX110T, LX155T, LX220T
8	IO_L7N_8	AT20	FX100T, LX110T, LX155T, LX220T
8	IO_L8P_CC_8	AT24	FX100T, LX110T, LX155T, LX220T
8	IO_L8N_CC_8 (2)	AR24	FX100T, LX110T, LX155T, LX220T
8	IO_L9P_CC_8	AU21	FX100T, LX110T, LX155T, LX220T
8	IO_L9N_CC_8 (2)	AT21	FX100T, LX110T, LX155T, LX220T
8	IO_L10P_CC_8	AV21	FX100T, LX110T, LX155T, LX220T
8	IO_L10N_CC_8 (2)	AV20	FX100T, LX110T, LX155T, LX220T

Table 2-8: **FF1738 Package—FX100T, LX110T, FX130T, LX155T, FX200T, LX220T, SX240T, and LX330T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
8	IO_L11P_CC_8	AU24	FX100T, LX110T, LX155T, LX220T
8	IO_L11N_CC_8 (2)	AV25	FX100T, LX110T, LX155T, LX220T
8	IO_L12P_VRN_8	AU23	FX100T, LX110T, LX155T, LX220T
8	IO_L12N_VRP_8	AU22	FX100T, LX110T, LX155T, LX220T
8	IO_L13P_8	AV23	FX100T, LX110T, LX155T, LX220T
8	IO_L13N_8	AV24	FX100T, LX110T, LX155T, LX220T
8	IO_L14P_8	AR23	FX100T, LX110T, LX155T, LX220T
8	IO_L14N_VREF_8	AP22	FX100T, LX110T, LX155T, LX220T
8	IO_L15P_8	AR22	FX100T, LX110T, LX155T, LX220T
8	IO_L15N_8	AT22	FX100T, LX110T, LX155T, LX220T
8	IO_L16P_8	AM22	FX100T, LX110T, LX155T, LX220T
8	IO_L16N_8	AM23	FX100T, LX110T, LX155T, LX220T
8	IO_L17P_8	AN23	FX100T, LX110T, LX155T, LX220T
8	IO_L17N_8	AP23	FX100T, LX110T, LX155T, LX220T
8	IO_L18P_8	AP20	FX100T, LX110T, LX155T, LX220T
8	IO_L18N_8	AP21	FX100T, LX110T, LX155T, LX220T
8	IO_L19P_8	AN21	FX100T, LX110T, LX155T, LX220T
8	IO_L19N_8	AM21	FX100T, LX110T, LX155T, LX220T
11	IO_L0P_11	F42	
11	IO_L0N_11	G42	
11	IO_L1P_11	F41	

Table 2-8: **FF1738 Package—FX100T, LX110T, FX130T, LX155T, FX200T, LX220T, SX240T, and LX330T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
11	IO_L1N_11	G41	
11	IO_L2P_11	H41	
11	IO_L2N_11	J41	
11	IO_L3P_11	J42	
11	IO_L3N_11	K42	
11	IO_L4P_11	L40	
11	IO_L4N_VREF_11	L41	
11	IO_L5P_11	L42	
11	IO_L5N_11	M41	
11	IO_L6P_11	M42	
11	IO_L6N_11	N41	
11	IO_L7P_11	N40	
11	IO_L7N_11	P40	
11	IO_L8P_CC_11	W40	
11	IO_L8N_CC_11 (2)	Y40	
11	IO_L9P_CC_11	AA40	
11	IO_L9N_CC_11 (2)	AA39	
11	IO_L10P_CC_SM15P_11	Y39	
11	IO_L10N_CC_SM15N_11 (2)	Y38	
11	IO_L11P_CC_SM14P_11	Y37	
11	IO_L11N_CC_SM14N_11 (2)	AA37	
11	IO_L12P_VRN_11	R42	
11	IO_L12N_VRP_11	P42	
11	IO_L13P_11	P41	
11	IO_L13N_11	R40	
11	IO_L14P_11	T40	
11	IO_L14N_VREF_11	T41	
11	IO_L15P_SM13P_11	T42	
11	IO_L15N_SM13N_11	U41	
11	IO_L16P_SM12P_11	U42	
11	IO_L16N_SM12N_11	V41	
11	IO_L17P_SM11P_11	V40	

Table 2-8: **FF1738 Package—FX100T, LX110T, FX130T, LX155T, FX200T, LX220T, SX240T, and LX330T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
11	IO_L17N_SM11N_11	W41	
11	IO_L18P_SM10P_11	W42	
11	IO_L18N_SM10N_11	Y42	
11	IO_L19P_SM9P_11	AA42	
11	IO_L19N_SM9N_11	AA41	
12	IO_L0P_12	AA7	
12	IO_L0N_12	AA6	
12	IO_L1P_12	G6	
12	IO_L1N_12	H5	
12	IO_L2P_12	W5	
12	IO_L2N_12	W6	
12	IO_L3P_12	H6	
12	IO_L3N_12	J5	
12	IO_L4P_12	Y7	
12	IO_L4N_VREF_12	W7	
12	IO_L5P_12	J6	
12	IO_L5N_12	K5	
12	IO_L6P_12	W8	
12	IO_L6N_12	V8	
12	IO_L7P_12	K4	
12	IO_L7N_12	L5	
12	IO_L8P_CC_12	V5	
12	IO_L8N_CC_12 (2)	V6	
12	IO_L9P_CC_12	L6	
12	IO_L9N_CC_12 (2)	M6	
12	IO_L10P_CC_12	N5	
12	IO_L10N_CC_12 (2)	N6	
12	IO_L11P_CC_12	U7	
12	IO_L11N_CC_12 (2)	U6	
12	IO_L12P_VRN_12	P5	
12	IO_L12N_VRP_12	P6	
12	IO_L13P_12	T7	

Table 2-8: **FF1738 Package—FX100T, LX110T, FX130T, LX155T, FX200T, LX220T, SX240T, and LX330T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
12	IO_L13N_12	T6	
12	IO_L14P_12	R4	
12	IO_L14N_VREF_12	R5	
12	IO_L15P_12	T5	
12	IO_L15N_12	T4	
12	IO_L16P_12	AA11	
12	IO_L16N_12	AA10	
12	IO_L17P_12	AA9	
12	IO_L17N_12	Y10	
12	IO_L18P_12	W11	
12	IO_L18N_12	W10	
12	IO_L19P_12	Y9	
12	IO_L19N_12	Y8	
13	IO_L0P_SM8P_13	AB41	
13	IO_L0N_SM8N_13	AB42	
13	IO_L1P_SM7P_13	AC41	
13	IO_L1N_SM7N_13	AD42	
13	IO_L2P_SM6P_13	AE42	
13	IO_L2N_SM6N_13	AD41	
13	IO_L3P_SM5P_13	AF41	
13	IO_L3N_SM5N_13	AF42	
13	IO_L4P_13	AF40	
13	IO_L4N_VREF_13	AG41	
13	IO_L5P_SM4P_13	AG42	
13	IO_L5N_SM4N_13	AH41	
13	IO_L6P_SM3P_13	AJ42	
13	IO_L6N_SM3N_13	AJ41	
13	IO_L7P_SM2P_13	AH40	
13	IO_L7N_SM2N_13	AJ40	
13	IO_L8P_CC_SM1P_13	AB37	
13	IO_L8N_CC_SM1N_13 (2)	AB38	
13	IO_L9P_CC_SM0P_13	AB39	

Table 2-8: **FF1738 Package—FX100T, LX110T, FX130T, LX155T, FX200T, LX220T, SX240T, and LX330T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
13	IO_L9N_CC_SM0N_13 (2)	AC38	
13	IO_L10P_CC_13	AE40	
13	IO_L10N_CC_13 (2)	AD40	
13	IO_L11P_CC_13	AC40	
13	IO_L11N_CC_13 (2)	AC39	
13	IO_L12P_VRN_13	AK40	
13	IO_L12N_VRP_13	AL40	
13	IO_L13P_13	AL41	
13	IO_L13N_13	AK42	
13	IO_L14P_13	AL42	
13	IO_L14N_VREF_13	AM42	
13	IO_L15P_13	AM41	
13	IO_L15N_13	AN41	
13	IO_L16P_13	AP42	
13	IO_L16N_13	AP41	
13	IO_L17P_13	AR42	
13	IO_L17N_13	AT42	
13	IO_L18P_13	AT41	
13	IO_L18N_13	AU41	
13	IO_L19P_13	AU42	
13	IO_L19N_13	AV41	
15	IO_L0P_15	H38	
15	IO_L0N_15	H39	
15	IO_L1P_15	G38	
15	IO_L1N_15	G39	
15	IO_L2P_15	F39	
15	IO_L2N_15	F40	
15	IO_L3P_15	E39	
15	IO_L3N_15	E40	
15	IO_L4P_15	R39	
15	IO_L4N_VREF_15	R38	
15	IO_L5P_15	R37	

Table 2-8: **FF1738 Package—FX100T, LX110T, FX130T, LX155T, FX200T, LX220T, SX240T, and LX330T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
15	IO_L5N_15	P37	
15	IO_L6P_15	P38	
15	IO_L6N_15	N38	
15	IO_L7P_15	N39	
15	IO_L7N_15	M39	
15	IO_L8P_CC_15	M38	
15	IO_L8N_CC_15 (2)	L39	
15	IO_L9P_CC_15	K38	
15	IO_L9N_CC_15 (2)	J38	
15	IO_L10P_CC_15	H40	
15	IO_L10N_CC_15 (2)	J40	
15	IO_L11P_CC_15	K40	
15	IO_L11N_CC_15 (2)	K39	
15	IO_L12P_VRN_15	V38	
15	IO_L12N_VRP_15	U37	
15	IO_L13P_15	T37	
15	IO_L13N_15	U38	
15	IO_L14P_15	T39	
15	IO_L14N_VREF_15	U39	
15	IO_L15P_15	V39	
15	IO_L15N_15	W38	
15	IO_L16P_15	AA35	
15	IO_L16N_15	AA36	
15	IO_L17P_15	AA34	
15	IO_L17N_15	Y34	
15	IO_L18P_15	Y35	
15	IO_L18N_15	W35	
15	IO_L19P_15	W36	
15	IO_L19N_15	W37	
17	IO_L0P_17	AB34	
17	IO_L0N_17	AC34	
17	IO_L1P_17	AC35	

Table 2-8: **FF1738 Package—FX100T, LX110T, FX130T, LX155T, FX200T, LX220T, SX240T, and LX330T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
17	IO_L1N_17	AB36	
17	IO_L2P_17	AC36	
17	IO_L2N_17	AD35	
17	IO_L3P_17	AD36	
17	IO_L3N_17	AD37	
17	IO_L4P_17	AE37	
17	IO_L4N_VREF_17	AD38	
17	IO_L5P_17	AE39	
17	IO_L5N_17	AE38	
17	IO_L6P_17	AF39	
17	IO_L6N_17	AG38	
17	IO_L7P_17	AG37	
17	IO_L7N_17	AF37	
17	IO_L8P_CC_17	AN40	
17	IO_L8N_CC_17 (2)	AP40	
17	IO_L9P_CC_17	AR40	
17	IO_L9N_CC_17 (2)	AT40	
17	IO_L10P_CC_17	AV40	
17	IO_L10N_CC_17 (2)	AU39	
17	IO_L11P_CC_17	AT39	
17	IO_L11N_CC_17 (2)	AR39	
17	IO_L12P_VRN_17	AG39	
17	IO_L12N_VRP_17	AH39	
17	IO_L13P_17	AJ38	
17	IO_L13N_17	AK39	
17	IO_L14P_17	AK38	
17	IO_L14N_VREF_17	AK37	
17	IO_L15P_17	AJ37	
17	IO_L15N_17	AH38	
17	IO_L16P_17	AL39	
17	IO_L16N_17	AM39	
17	IO_L17P_17	AN39	

Table 2-8: **FF1738 Package—FX100T, LX110T, FX130T, LX155T, FX200T, LX220T, SX240T, and LX330T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
17	IO_L17N_17	AP38	
17	IO_L18P_17	AN38	
17	IO_L18N_17	AM38	
17	IO_L19P_17	AM37	
17	IO_L19N_17	AL37	
18	IO_L0P_18	AJ7	
18	IO_L0N_18	AK7	
18	IO_L1P_18	AB11	
18	IO_L1N_18	AC10	
18	IO_L2P_18	AL5	
18	IO_L2N_18	AK5	
18	IO_L3P_18	AB9	
18	IO_L3N_18	AB8	
18	IO_L4P_18	AJ6	
18	IO_L4N_VREF_18	AJ5	
18	IO_L5P_18	AC8	
18	IO_L5N_18	AC9	
18	IO_L6P_18	AH6	
18	IO_L6N_18	AH5	
18	IO_L7P_18	AD10	
18	IO_L7N_18	AD11	
18	IO_L8P_CC_18	AG4	
18	IO_L8N_CC_18 (2)	AH4	
18	IO_L9P_CC_18	AB7	
18	IO_L9N_CC_18 (2)	AB6	
18	IO_L10P_CC_18	AC5	
18	IO_L10N_CC_18 (2)	AC6	
18	IO_L11P_CC_18	AF5	
18	IO_L11N_CC_18 (2)	AF6	
18	IO_L12P_VRN_18	AD6	
18	IO_L12N_VRP_18	AD7	
18	IO_L13P_18	AG6	

Table 2-8: **FF1738 Package—FX100T, LX110T, FX130T, LX155T, FX200T, LX220T, SX240T, and LX330T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
18	IO_L13N_18	AG7	
18	IO_L14P_18	AE5	
18	IO_L14N_VREF_18	AD5	
18	IO_L15P_18	AF7	
18	IO_L15N_18	AE7	
18	IO_L16P_18	AD8	
18	IO_L16N_18	AE8	
18	IO_L17P_18	AF9	
18	IO_L17N_18	AF10	
18	IO_L18P_18	AE9	
18	IO_L18N_18	AE10	
18	IO_L19P_18	AF11	
18	IO_L19N_18	AF12	
19	IO_L0P_19	R34	
19	IO_L0N_19	P35	
19	IO_L1P_19	N35	
19	IO_L1N_19	M36	
19	IO_L2P_19	L37	
19	IO_L2N_19	M37	
19	IO_L3P_19	N36	
19	IO_L3N_19	P36	
19	IO_L4P_19	L36	
19	IO_L4N_VREF_19	L35	
19	IO_L5P_19	K35	
19	IO_L5N_19	J35	
19	IO_L6P_19	H35	
19	IO_L6N_19	J36	
19	IO_L7P_19	K37	
19	IO_L7N_19	J37	
19	IO_L8P_CC_19	U34	
19	IO_L8N_CC_19 (2)	T35	
19	IO_L9P_CC_19	T34	

Table 2-8: **FF1738 Package—FX100T, LX110T, FX130T, LX155T, FX200T, LX220T, SX240T, and LX330T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
19	IO_L9N_CC_19(2)	U33	
19	IO_L10P_CC_19	R35	
19	IO_L10N_CC_19(2)	T36	
19	IO_L11P_CC_19	U36	
19	IO_L11N_CC_19(2)	V36	
19	IO_L12P_VRN_19	H36	
19	IO_L12N_VRP_19	G37	
19	IO_L13P_19	F36	
19	IO_L13N_19	G36	
19	IO_L14P_19	F37	
19	IO_L14N_VREF_19	E37	
19	IO_L15P_19	E38	
19	IO_L15N_19	D37	
19	IO_L16P_19	V35	
19	IO_L16N_19	V34	
19	IO_L17P_19	V33	
19	IO_L17N_19	W33	
19	IO_L18P_19	Y33	
19	IO_L18N_19	W32	
19	IO_L19P_19	Y32	
19	IO_L19N_19	AA32	
20	IO_L0P_20	N9	
20	IO_L0N_20	N8	
20	IO_L1P_20	E9	
20	IO_L1N_20	E8	
20	IO_L2P_20	P7	
20	IO_L2N_20	P8	
20	IO_L3P_20	D7	
20	IO_L3N_20	E7	
20	IO_L4P_20	R7	
20	IO_L4N_VREF_20	R8	
20	IO_L5P_20	F7	

Table 2-8: **FF1738 Package—FX100T, LX110T, FX130T, LX155T, FX200T, LX220T, SX240T, and LX330T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
20	IO_L5N_20	F6	
20	IO_L6P_20	R9	
20	IO_L6N_20	T9	
20	IO_L7P_20	E5	
20	IO_L7N_20	F5	
20	IO_L8P_CC_20	V9	
20	IO_L8N_CC_20 (2)	V10	
20	IO_L9P_CC_20	F9	
20	IO_L9N_CC_20 (2)	G9	
20	IO_L10P_CC_20	G7	
20	IO_L10N_CC_20 (2)	G8	
20	IO_L11P_CC_20	U8	
20	IO_L11N_CC_20 (2)	U9	
20	IO_L12P_VRN_20	H8	
20	IO_L12N_VRP_20	H9	
20	IO_L13P_20	T10	
20	IO_L13N_20	T11	
20	IO_L14P_20	J8	
20	IO_L14N_VREF_20	J7	
20	IO_L15P_20	U11	
20	IO_L15N_20	V11	
20	IO_L16P_20	K8	
20	IO_L16N_20	K9	
20	IO_L17P_20	K7	
20	IO_L17N_20	L7	
20	IO_L18P_20	M7	
20	IO_L18N_20	M8	
20	IO_L19P_20	M9	
20	IO_L19N_20	L9	
21	IO_L0P_21	AB33	
21	IO_L0N_21	AB32	
21	IO_L1P_21	AC33	

Table 2-8: **FF1738 Package—FX100T, LX110T, FX130T, LX155T, FX200T, LX220T, SX240T, and LX330T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
21	IO_L1N_21	AD32	
21	IO_L2P_21	AD33	
21	IO_L2N_21	AE32	
21	IO_L3P_21	AE33	
21	IO_L3N_21	AE34	
21	IO_L4P_21	AV39	
21	IO_L4N_VREF_21	AV38	
21	IO_L5P_21	AU38	
21	IO_L5N_21	AU37	
21	IO_L6P_21	AT37	
21	IO_L6N_21	AR38	
21	IO_L7P_21	AR37	
21	IO_L7N_21	AT36	
21	IO_L8P_CC_21	AE35	
21	IO_L8N_CC_21 (2)	AF34	
21	IO_L9P_CC_21	AF35	
21	IO_L9N_CC_21 (2)	AF36	
21	IO_L10P_CC_21	AH34	
21	IO_L10N_CC_21 (2)	AG34	
21	IO_L11P_CC_21	AH35	
21	IO_L11N_CC_21 (2)	AG36	
21	IO_L12P_VRN_21	AP37	
21	IO_L12N_VRP_21	AP36	
21	IO_L13P_21	AP35	
21	IO_L13N_21	AN36	
21	IO_L14P_21	AM36	
21	IO_L14N_VREF_21	AN35	
21	IO_L15P_21	AN34	
21	IO_L15N_21	AM34	
21	IO_L16P_21	AH36	
21	IO_L16N_21	AJ36	
21	IO_L17P_21	AJ35	

Table 2-8: **FF1738 Package—FX100T, LX110T, FX130T, LX155T, FX200T, LX220T, SX240T, and LX330T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
21	IO_L17N_21	AK35	
21	IO_L18P_21	AL36	
21	IO_L18N_21	AL35	
21	IO_L19P_21	AL34	
21	IO_L19N_21	AK34	
23	IO_L0P_23	N33	
23	IO_L0N_23	N34	
23	IO_L1P_23	M34	
23	IO_L1N_23	M33	
23	IO_L2P_23	M32	
23	IO_L2N_23	M31	
23	IO_L3P_23	N31	
23	IO_L3N_23	P31	
23	IO_L4P_23	H34	
23	IO_L4N_VREF_23	G34	
23	IO_L5P_23	G33	
23	IO_L5N_23	H33	
23	IO_L6P_23	G32	
23	IO_L6N_23	G31	
23	IO_L7P_23	H31	
23	IO_L7N_23	J31	
23	IO_L8P_CC_23	F35	
23	IO_L8N_CC_23 (2)	E35	
23	IO_L9P_CC_23	E34	
23	IO_L9N_CC_23 (2)	F34	
23	IO_L10P_CC_23	F31	
23	IO_L10N_CC_23 (2)	F32	
23	IO_L11P_CC_23	E32	
23	IO_L11N_CC_23 (2)	E33	
23	IO_L12P_VRN_23	L34	
23	IO_L12N_VRP_23	K34	
23	IO_L13P_23	K33	

Table 2-8: **FF1738 Package—FX100T, LX110T, FX130T, LX155T, FX200T, LX220T, SX240T, and LX330T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
23	IO_L13N_23	J33	
23	IO_L14P_23	K32	
23	IO_L14N_VREF_23	J32	
23	IO_L15P_23	L32	
23	IO_L15N_23	L31	
23	IO_L16P_23	P33	
23	IO_L16N_23	P32	
23	IO_L17P_23	R33	
23	IO_L17N_23	R32	
23	IO_L18P_23	T32	
23	IO_L18N_23	U32	
23	IO_L19P_23	U31	
23	IO_L19N_23	T31	
24	IO_L0P_24	J12	
24	IO_L0N_24	H11	
24	IO_L1P_24	G12	
24	IO_L1N_24	G11	
24	IO_L2P_24	F12	
24	IO_L2N_24	F11	
24	IO_L3P_24	E10	
24	IO_L3N_24	F10	
24	IO_L4P_24	K14	
24	IO_L4N_VREF_24	K13	
24	IO_L5P_24	K12	
24	IO_L5N_24	J11	
24	IO_L6P_24	J13	
24	IO_L6N_24	H13	
24	IO_L7P_24	H10	
24	IO_L7N_24	J10	
24	IO_L8P_CC_24	H14	
24	IO_L8N_CC_24 (2)	H15	
24	IO_L9P_CC_24	K10	

Table 2-8: **FF1738 Package—FX100T, LX110T, FX130T, LX155T, FX200T, LX220T, SX240T, and LX330T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
24	IO_L9N_CC_24 (2)	L10	
24	IO_L10P_CC_24	L12	
24	IO_L10N_CC_24 (2)	L11	
24	IO_L11P_CC_24	G13	
24	IO_L11N_CC_24 (2)	G14	
24	IO_L12P_VRN_24	M11	
24	IO_L12N_VRP_24	M12	
24	IO_L13P_24	F14	
24	IO_L13N_24	E13	
24	IO_L14P_24	N11	
24	IO_L14N_VREF_24	P12	
24	IO_L15P_24	E12	
24	IO_L15N_24	D12	
24	IO_L16P_24	P11	
24	IO_L16N_24	N10	
24	IO_L17P_24	D13	
24	IO_L17N_24	E14	
24	IO_L18P_24	R10	
24	IO_L18N_24	P10	
24	IO_L19P_24	E15	
24	IO_L19N_24	F15	
25	IO_L0P_25	AG31	
25	IO_L0N_25	AF31	
25	IO_L1P_25	AF32	
25	IO_L1N_25	AG33	
25	IO_L2P_25	AH33	
25	IO_L2N_25	AG32	
25	IO_L3P_25	AH31	
25	IO_L3N_25	AJ31	
25	IO_L4P_25	AV35	
25	IO_L4N_VREF_25	AV36	
25	IO_L5P_25	AU36	

Table 2-8: **FF1738 Package—FX100T, LX110T, FX130T, LX155T, FX200T, LX220T, SX240T, and LX330T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
25	IO_L5N_25	AT35	
25	IO_L6P_25	AU34	
25	IO_L6N_25	AT34	
25	IO_L7P_25	AR35	
25	IO_L7N_25	AR34	
25	IO_L8P_CC_25	AU32	
25	IO_L8N_CC_25 (2)	AU33	
25	IO_L9P_CC_25	AV33	
25	IO_L9N_CC_25 (2)	AV34	
25	IO_L10P_CC_25	AV31	
25	IO_L10N_CC_25 (2)	AU31	
25	IO_L11P_CC_25	AT32	
25	IO_L11N_CC_25 (2)	AT31	
25	IO_L12P_VRN_25	AP31	
25	IO_L12N_VRP_25	AN31	
25	IO_L13P_25	AR32	
25	IO_L13N_25	AP32	
25	IO_L14P_25	AR33	
25	IO_L14N_VREF_25	AP33	
25	IO_L15P_25	AN33	
25	IO_L15N_25	AM33	
25	IO_L16P_25	AK33	
25	IO_L16N_25	AJ33	
25	IO_L17P_25	AJ32	
25	IO_L17N_25	AK32	
25	IO_L18P_25	AL32	
25	IO_L18N_25	AM32	
25	IO_L19P_25	AL31	
25	IO_L19N_25	AM31	
26	IO_L0P_26	AT7	
26	IO_L0N_26	AR7	
26	IO_L1P_26	AG12	

Table 2-8: **FF1738 Package—FX100T, LX110T, FX130T, LX155T, FX200T, LX220T, SX240T, and LX330T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
26	IO_L1N_26	AG11	
26	IO_L2P_26	AT6	
26	IO_L2N_26	AR5	
26	IO_L3P_26	AG9	
26	IO_L3N_26	AH9	
26	IO_L4P_26	AT5	
26	IO_L4N_VREF_26	AU6	
26	IO_L5P_26	AH10	
26	IO_L5N_26	AH11	
26	IO_L6P_26	AV6	
26	IO_L6N_26	AV5	
26	IO_L7P_26	AJ11	
26	IO_L7N_26	AJ10	
26	IO_L8P_CC_26	AM9	
26	IO_L8N_CC_26 (2)	AN9	
26	IO_L9P_CC_26	AG8	
26	IO_L9N_CC_26 (2)	AH8	
26	IO_L10P_CC_26	AK8	
26	IO_L10N_CC_26 (2)	AJ8	
26	IO_L11P_CC_26	AN8	
26	IO_L11N_CC_26 (2)	AP8	
26	IO_L12P_VRN_26	AK9	
26	IO_L12N_VRP_26	AK10	
26	IO_L13P_26	AP7	
26	IO_L13N_26	AR8	
26	IO_L14P_26	AL9	
26	IO_L14N_VREF_26	AL10	
26	IO_L15P_26	AP6	
26	IO_L15N_26	AP5	
26	IO_L16P_26	AL6	
26	IO_L16N_26	AL7	
26	IO_L17P_26	AN4	

Table 2-8: **FF1738 Package—FX100T, LX110T, FX130T, LX155T, FX200T, LX220T, SX240T, and LX330T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
26	IO_L17N_26	AN5	
26	IO_L18P_26	AN6	
26	IO_L18N_26	AM6	
26	IO_L19P_26	AM7	
26	IO_L19N_26	AM8	
27	IO_L0P_27	D31	FX100T, LX110T, LX155T, LX220T
27	IO_L0N_27	C31	FX100T, LX110T, LX155T, LX220T
27	IO_L1P_27	C30	FX100T, LX110T, LX155T, LX220T
27	IO_L1N_27	B31	FX100T, LX110T, LX155T, LX220T
27	IO_L2P_27	A30	FX100T, LX110T, LX155T, LX220T
27	IO_L2N_27	A31	FX100T, LX110T, LX155T, LX220T
27	IO_L3P_27	A32	FX100T, LX110T, LX155T, LX220T
27	IO_L3N_27	B32	FX100T, LX110T, LX155T, LX220T
27	IO_L4P_27	B33	FX100T, LX110T, LX155T, LX220T
27	IO_L4N_VREF_27	C33	FX100T, LX110T, LX155T, LX220T
27	IO_L5P_27	D32	FX100T, LX110T, LX155T, LX220T
27	IO_L5N_27	D33	FX100T, LX110T, LX155T, LX220T
27	IO_L6P_27	C34	FX100T, LX110T, LX155T, LX220T
27	IO_L6N_27	B34	FX100T, LX110T, LX155T, LX220T
27	IO_L7P_27	A34	FX100T, LX110T, LX155T, LX220T
27	IO_L7N_27	A35	FX100T, LX110T, LX155T, LX220T
27	IO_L8P_CC_27	D35	FX100T, LX110T, LX155T, LX220T

Table 2-8: **FF1738 Package—FX100T, LX110T, FX130T, LX155T, FX200T, LX220T, SX240T, and LX330T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
27	IO_L8N_CC_27 (2)	D36	FX100T, LX110T, LX155T, LX220T
27	IO_L9P_CC_27	C36	FX100T, LX110T, LX155T, LX220T
27	IO_L9N_CC_27 (2)	C35	FX100T, LX110T, LX155T, LX220T
27	IO_L10P_CC_27	A37	FX100T, LX110T, LX155T, LX220T
27	IO_L10N_CC_27 (2)	A36	FX100T, LX110T, LX155T, LX220T
27	IO_L11P_CC_27	B37	FX100T, LX110T, LX155T, LX220T
27	IO_L11N_CC_27 (2)	B36	FX100T, LX110T, LX155T, LX220T
27	IO_L12P_VRN_27	C38	FX100T, LX110T, LX155T, LX220T
27	IO_L12N_VRP_27	D38	FX100T, LX110T, LX155T, LX220T
27	IO_L13P_27	C39	FX100T, LX110T, LX155T, LX220T
27	IO_L13N_27	C40	FX100T, LX110T, LX155T, LX220T
27	IO_L14P_27	B39	FX100T, LX110T, LX155T, LX220T
27	IO_L14N_VREF_27	B38	FX100T, LX110T, LX155T, LX220T
27	IO_L15P_27	A39	FX100T, LX110T, LX155T, LX220T
27	IO_L15N_27	A40	FX100T, LX110T, LX155T, LX220T
27	IO_L16P_27	A41	FX100T, LX110T, LX155T, LX220T
27	IO_L16N_27	B41	FX100T, LX110T, LX155T, LX220T
27	IO_L17P_27	B42	FX100T, LX110T, LX155T, LX220T
27	IO_L17N_27	C41	FX100T, LX110T, LX155T, LX220T
27	IO_L18P_27	D40	FX100T, LX110T, LX155T, LX220T

Table 2-8: **FF1738 Package—FX100T, LX110T, FX130T, LX155T, FX200T, LX220T, SX240T, and LX330T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
27	IO_L18N_27	D41	FX100T, LX110T, LX155T, LX220T
27	IO_L19P_27	E42	FX100T, LX110T, LX155T, LX220T
27	IO_L19N_27	D42	FX100T, LX110T, LX155T, LX220T
29	IO_L0P_29	AY42	FX100T, LX110T, LX155T, LX220T
29	IO_L0N_29	AW42	FX100T, LX110T, LX155T, LX220T
29	IO_L1P_29	AW41	FX100T, LX110T, LX155T, LX220T
29	IO_L1N_29	AW40	FX100T, LX110T, LX155T, LX220T
29	IO_L2P_29	AY40	FX100T, LX110T, LX155T, LX220T
29	IO_L2N_29	BA41	FX100T, LX110T, LX155T, LX220T
29	IO_L3P_29	BA42	FX100T, LX110T, LX155T, LX220T
29	IO_L3N_29	BB41	FX100T, LX110T, LX155T, LX220T
29	IO_L4P_29	BA40	FX100T, LX110T, LX155T, LX220T
29	IO_L4N_VREF_29	BB39	FX100T, LX110T, LX155T, LX220T
29	IO_L5P_29	BB38	FX100T, LX110T, LX155T, LX220T
29	IO_L5N_29	BA39	FX100T, LX110T, LX155T, LX220T
29	IO_L6P_29	AY38	FX100T, LX110T, LX155T, LX220T
29	IO_L6N_29	AW37	FX100T, LX110T, LX155T, LX220T
29	IO_L7P_29	AW38	FX100T, LX110T, LX155T, LX220T
29	IO_L7N_29	AY39	FX100T, LX110T, LX155T, LX220T
29	IO_L8P_CC_29	BB37	FX100T, LX110T, LX155T, LX220T

Table 2-8: **FF1738 Package—FX100T, LX110T, FX130T, LX155T, FX200T, LX220T, SX240T, and LX330T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
29	IO_L8N_CC_29 (2)	BA37	FX100T, LX110T, LX155T, LX220T
29	IO_L9P_CC_29	AY37	FX100T, LX110T, LX155T, LX220T
29	IO_L9N_CC_29 (2)	AW36	FX100T, LX110T, LX155T, LX220T
29	IO_L10P_CC_29	BB36	FX100T, LX110T, LX155T, LX220T
29	IO_L10N_CC_29 (2)	BA36	FX100T, LX110T, LX155T, LX220T
29	IO_L11P_CC_29	AY35	FX100T, LX110T, LX155T, LX220T
29	IO_L11N_CC_29 (2)	AW35	FX100T, LX110T, LX155T, LX220T
29	IO_L12P_VRN_29	BB34	FX100T, LX110T, LX155T, LX220T
29	IO_L12N_VRP_29	BA35	FX100T, LX110T, LX155T, LX220T
29	IO_L13P_29	BB33	FX100T, LX110T, LX155T, LX220T
29	IO_L13N_29	BA34	FX100T, LX110T, LX155T, LX220T
29	IO_L14P_29	AY33	FX100T, LX110T, LX155T, LX220T
29	IO_L14N_VREF_29	AY34	FX100T, LX110T, LX155T, LX220T
29	IO_L15P_29	AW33	FX100T, LX110T, LX155T, LX220T
29	IO_L15N_29	AW32	FX100T, LX110T, LX155T, LX220T
29	IO_L16P_29	AY32	FX100T, LX110T, LX155T, LX220T
29	IO_L16N_29	BA32	FX100T, LX110T, LX155T, LX220T
29	IO_L17P_29	BB32	FX100T, LX110T, LX155T, LX220T
29	IO_L17N_29	BB31	FX100T, LX110T, LX155T, LX220T
29	IO_L18P_29	BA30	FX100T, LX110T, LX155T, LX220T

Table 2-8: **FF1738 Package—FX100T, LX110T, FX130T, LX155T, FX200T, LX220T, SX240T, and LX330T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
29	IO_L18N_29	BA31	FX100T, LX110T, LX155T, LX220T
29	IO_L19P_29	AY30	FX100T, LX110T, LX155T, LX220T
29	IO_L19N_29	AW31	FX100T, LX110T, LX155T, LX220T
31	IO_L0P_31	D20	FX100T, LX110T, FX130T, LX155T, LX220T
31	IO_L0N_31	D21	FX100T, LX110T, FX130T, LX155T, LX220T
31	IO_L1P_31	C21	FX100T, LX110T, FX130T, LX155T, LX220T
31	IO_L1N_31	C20	FX100T, LX110T, FX130T, LX155T, LX220T
31	IO_L2P_31	A20	FX100T, LX110T, FX130T, LX155T, LX220T
31	IO_L2N_31	A21	FX100T, LX110T, FX130T, LX155T, LX220T
31	IO_L3P_31	A22	FX100T, LX110T, FX130T, LX155T, LX220T
31	IO_L3N_31	B21	FX100T, LX110T, FX130T, LX155T, LX220T
31	IO_L4P_31	D22	FX100T, LX110T, FX130T, LX155T, LX220T
31	IO_L4N_VREF_31	D23	FX100T, LX110T, FX130T, LX155T, LX220T
31	IO_L5P_31	C23	FX100T, LX110T, FX130T, LX155T, LX220T
31	IO_L5N_31	B22	FX100T, LX110T, FX130T, LX155T, LX220T
31	IO_L6P_31	B23	FX100T, LX110T, FX130T, LX155T, LX220T
31	IO_L6N_31	A24	FX100T, LX110T, FX130T, LX155T, LX220T
31	IO_L7P_31	B24	FX100T, LX110T, FX130T, LX155T, LX220T
31	IO_L7N_31	C24	FX100T, LX110T, FX130T, LX155T, LX220T
31	IO_L8P_CC_31	E24	FX100T, LX110T, FX130T, LX155T, LX220T

Table 2-8: **FF1738 Package—FX100T, LX110T, FX130T, LX155T, FX200T, LX220T, SX240T, and LX330T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
31	IO_L8N_CC_31 (2)	E25	FX100T, LX110T, FX130T, LX155T, LX220T
31	IO_L9P_CC_31	D25	FX100T, LX110T, FX130T, LX155T, LX220T
31	IO_L9N_CC_31 (2)	D26	FX100T, LX110T, FX130T, LX155T, LX220T
31	IO_L10P_CC_31	E28	FX100T, LX110T, FX130T, LX155T, LX220T
31	IO_L10N_CC_31 (2)	E27	FX100T, LX110T, FX130T, LX155T, LX220T
31	IO_L11P_CC_31	D27	FX100T, LX110T, FX130T, LX155T, LX220T
31	IO_L11N_CC_31 (2)	C26	FX100T, LX110T, FX130T, LX155T, LX220T
31	IO_L12P_VRN_31	C25	FX100T, LX110T, FX130T, LX155T, LX220T
31	IO_L12N_VRP_31	B26	FX100T, LX110T, FX130T, LX155T, LX220T
31	IO_L13P_31	A26	FX100T, LX110T, FX130T, LX155T, LX220T
31	IO_L13N_31	A25	FX100T, LX110T, FX130T, LX155T, LX220T
31	IO_L14P_31	A27	FX100T, LX110T, FX130T, LX155T, LX220T
31	IO_L14N_VREF_31	B27	FX100T, LX110T, FX130T, LX155T, LX220T
31	IO_L15P_31	B28	FX100T, LX110T, FX130T, LX155T, LX220T
31	IO_L15N_31	A29	FX100T, LX110T, FX130T, LX155T, LX220T
31	IO_L16P_31	F30	FX100T, LX110T, FX130T, LX155T, LX220T
31	IO_L16N_31	E30	FX100T, LX110T, FX130T, LX155T, LX220T
31	IO_L17P_31	E29	FX100T, LX110T, FX130T, LX155T, LX220T
31	IO_L17N_31	D30	FX100T, LX110T, FX130T, LX155T, LX220T
31	IO_L18P_31	C29	FX100T, LX110T, FX130T, LX155T, LX220T

Table 2-8: **FF1738 Package—FX100T, LX110T, FX130T, LX155T, FX200T, LX220T, SX240T, and LX330T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
31	IO_L18N_31	B29	FX100T, LX110T, FX130T, LX155T, LX220T
31	IO_L19P_31	C28	FX100T, LX110T, FX130T, LX155T, LX220T
31	IO_L19N_31	D28	FX100T, LX110T, FX130T, LX155T, LX220T
33	IO_L0P_33	BB29	FX100T, LX110T, FX130T, LX155T, LX220T
33	IO_L0N_33	BB28	FX100T, LX110T, FX130T, LX155T, LX220T
33	IO_L1P_33	BB27	FX100T, LX110T, FX130T, LX155T, LX220T
33	IO_L1N_33	BA27	FX100T, LX110T, FX130T, LX155T, LX220T
33	IO_L2P_33	BB26	FX100T, LX110T, FX130T, LX155T, LX220T
33	IO_L2N_33	BA26	FX100T, LX110T, FX130T, LX155T, LX220T
33	IO_L3P_33	BA25	FX100T, LX110T, FX130T, LX155T, LX220T
33	IO_L3N_33	AY25	FX100T, LX110T, FX130T, LX155T, LX220T
33	IO_L4P_33	AW30	FX100T, LX110T, FX130T, LX155T, LX220T
33	IO_L4N_VREF_33	AV30	FX100T, LX110T, FX130T, LX155T, LX220T
33	IO_L5P_33	AV29	FX100T, LX110T, FX130T, LX155T, LX220T
33	IO_L5N_33	AW28	FX100T, LX110T, FX130T, LX155T, LX220T
33	IO_L6P_33	AY27	FX100T, LX110T, FX130T, LX155T, LX220T
33	IO_L6N_33	AY28	FX100T, LX110T, FX130T, LX155T, LX220T
33	IO_L7P_33	AY29	FX100T, LX110T, FX130T, LX155T, LX220T
33	IO_L7N_33	BA29	FX100T, LX110T, FX130T, LX155T, LX220T
33	IO_L8P_CC_33	BB24	FX100T, LX110T, FX130T, LX155T, LX220T

Table 2-8: **FF1738 Package—FX100T, LX110T, FX130T, LX155T, FX200T, LX220T, SX240T, and LX330T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
33	IO_L8N_CC_33 (2)	BA24	FX100T, LX110T, FX130T, LX155T, LX220T
33	IO_L9P_CC_33	AY24	FX100T, LX110T, FX130T, LX155T, LX220T
33	IO_L9N_CC_33 (2)	AW25	FX100T, LX110T, FX130T, LX155T, LX220T
33	IO_L10P_CC_33	AV28	FX100T, LX110T, FX130T, LX155T, LX220T
33	IO_L10N_CC_33 (2)	AW27	FX100T, LX110T, FX130T, LX155T, LX220T
33	IO_L11P_CC_33	AV26	FX100T, LX110T, FX130T, LX155T, LX220T
33	IO_L11N_CC_33 (2)	AW26	FX100T, LX110T, FX130T, LX155T, LX220T
33	IO_L12P_VRN_33	BB22	FX100T, LX110T, FX130T, LX155T, LX220T
33	IO_L12N_VRP_33	BB23	FX100T, LX110T, FX130T, LX155T, LX220T
33	IO_L13P_33	BB21	FX100T, LX110T, FX130T, LX155T, LX220T
33	IO_L13N_33	BA22	FX100T, LX110T, FX130T, LX155T, LX220T
33	IO_L14P_33	AY22	FX100T, LX110T, FX130T, LX155T, LX220T
33	IO_L14N_VREF_33	AY23	FX100T, LX110T, FX130T, LX155T, LX220T
33	IO_L15P_33	AW23	FX100T, LX110T, FX130T, LX155T, LX220T
33	IO_L15N_33	AW22	FX100T, LX110T, FX130T, LX155T, LX220T
33	IO_L16P_33	BB20	FX100T, LX110T, FX130T, LX155T, LX220T
33	IO_L16N_33	BA21	FX100T, LX110T, FX130T, LX155T, LX220T
33	IO_L17P_33	BA20	FX100T, LX110T, FX130T, LX155T, LX220T
33	IO_L17N_33	BA19	FX100T, LX110T, FX130T, LX155T, LX220T
33	IO_L18P_33	AY19	FX100T, LX110T, FX130T, LX155T, LX220T

Table 2-8: **FF1738 Package—FX100T, LX110T, FX130T, LX155T, FX200T, LX220T, SX240T, and LX330T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
33	IO_L18N_33	AY20	FX100T, LX110T, FX130T, LX155T, LX220T
33	IO_L19P_33	AW21	FX100T, LX110T, FX130T, LX155T, LX220T
33	IO_L19N_33	AW20	FX100T, LX110T, FX130T, LX155T, LX220T
34	IO_L0P_34	AW18	FX100T, LX110T, FX130T, LX155T, LX220T
34	IO_L0N_34	AV19	FX100T, LX110T, FX130T, LX155T, LX220T
34	IO_L1P_34	AL11	FX100T, LX110T, FX130T, LX155T, LX220T
34	IO_L1N_34	AL12	FX100T, LX110T, FX130T, LX155T, LX220T
34	IO_L2P_34	AV18	FX100T, LX110T, FX130T, LX155T, LX220T
34	IO_L2N_34	AU17	FX100T, LX110T, FX130T, LX155T, LX220T
34	IO_L3P_34	AM11	FX100T, LX110T, FX130T, LX155T, LX220T
34	IO_L3N_34	AM12	FX100T, LX110T, FX130T, LX155T, LX220T
34	IO_L4P_34	AV16	FX100T, LX110T, FX130T, LX155T, LX220T
34	IO_L4N_VREF_34	AU16	FX100T, LX110T, FX130T, LX155T, LX220T
34	IO_L5P_34	AN11	FX100T, LX110T, FX130T, LX155T, LX220T
34	IO_L5N_34	AN10	FX100T, LX110T, FX130T, LX155T, LX220T
34	IO_L6P_34	AV15	FX100T, LX110T, FX130T, LX155T, LX220T
34	IO_L6N_34	AV14	FX100T, LX110T, FX130T, LX155T, LX220T
34	IO_L7P_34	AP10	FX100T, LX110T, FX130T, LX155T, LX220T
34	IO_L7N_34	AR9	FX100T, LX110T, FX130T, LX155T, LX220T
34	IO_L8P_CC_34	AW13	FX100T, LX110T, FX130T, LX155T, LX220T

Table 2-8: **FF1738 Package—FX100T, LX110T, FX130T, LX155T, FX200T, LX220T, SX240T, and LX330T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
34	IO_L8N_CC_34 (2)	AV13	FX100T, LX110T, FX130T, LX155T, LX220T
34	IO_L9P_CC_34	AP11	FX100T, LX110T, FX130T, LX155T, LX220T
34	IO_L9N_CC_34 (2)	AP12	FX100T, LX110T, FX130T, LX155T, LX220T
34	IO_L10P_CC_34	AR10	FX100T, LX110T, FX130T, LX155T, LX220T
34	IO_L10N_CC_34 (2)	AT10	FX100T, LX110T, FX130T, LX155T, LX220T
34	IO_L11P_CC_34	AW12	FX100T, LX110T, FX130T, LX155T, LX220T
34	IO_L11N_CC_34 (2)	AV11	FX100T, LX110T, FX130T, LX155T, LX220T
34	IO_L12P_VRN_34	AT11	FX100T, LX110T, FX130T, LX155T, LX220T
34	IO_L12N_VRP_34	AR12	FX100T, LX110T, FX130T, LX155T, LX220T
34	IO_L13P_34	AU11	FX100T, LX110T, FX130T, LX155T, LX220T
34	IO_L13N_34	AU12	FX100T, LX110T, FX130T, LX155T, LX220T
34	IO_L14P_34	AR13	FX100T, LX110T, FX130T, LX155T, LX220T
34	IO_L14N_VREF_34	AT12	FX100T, LX110T, FX130T, LX155T, LX220T
34	IO_L15P_34	AU14	FX100T, LX110T, FX130T, LX155T, LX220T
34	IO_L15N_34	AU13	FX100T, LX110T, FX130T, LX155T, LX220T
34	IO_L16P_34	AW7	FX100T, LX110T, FX130T, LX155T, LX220T
34	IO_L16N_34	AV8	FX100T, LX110T, FX130T, LX155T, LX220T
34	IO_L17P_34	AV10	FX100T, LX110T, FX130T, LX155T, LX220T
34	IO_L17N_34	AV9	FX100T, LX110T, FX130T, LX155T, LX220T
34	IO_L18P_34	AU9	FX100T, LX110T, FX130T, LX155T, LX220T

Table 2-8: **FF1738 Package—FX100T, LX110T, FX130T, LX155T, FX200T, LX220T, SX240T, and LX330T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
34	IO_L18N_34	AT9	FX100T, LX110T, FX130T, LX155T, LX220T
34	IO_L19P_34	AU8	FX100T, LX110T, FX130T, LX155T, LX220T
34	IO_L19N_34	AU7	FX100T, LX110T, FX130T, LX155T, LX220T
NA	MGTTXP0_112	T2	
NA	MGTAVTTTX_112	AA3	
NA	MGTTXN0_112	U2	
NA	MGTRXP0_112	U1	
NA	MGTAVTTRX_112	U3	
NA	MGTRXN0_112	V1	
NA	MGTAVCCPLL_112	Y3	
NA	MGTRXN1_112	W1	
NA	MGTREFCLKN_112	V3	
NA	MGTRXP1_112	Y1	
NA	MGTREFCLKP_112	V4	
NA	MGTTXN1_112	Y2	
NA	MGTAVTTTX_112	T3	
NA	MGTTXP1_112	AA2	
NA	MGTAVTTRXC	AA5	
NA	MGTRREF_112	AB4	
NC	NC	Y5	FX100T, LX110T, FX130T, LX155T, FX200T, LX220T, SX240T, LX330T
NA	MGTTXP0_114	AB2	
NA	MGTAVTTTX_114	AB3	
NA	MGTTXN0_114	AC2	
NA	MGTRXP0_114	AC1	
NA	MGTAVTTRX_114	AC3	
NA	MGTRXN0_114	AD1	
NA	MGTAVCCPLL_114	AF3	
NA	MGTRXN1_114	AE1	
NA	MGTREFCLKN_114	AD3	

Table 2-8: **FF1738 Package—FX100T, LX110T, FX130T, LX155T, FX200T, LX220T, SX240T, and LX330T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	MGTRXP1_114	AF1	
NA	MGTREFCLKP_114	AD4	
NA	MGTTXN1_114	AF2	
NA	MGTAVTTTX_114	AG3	
NA	MGTTXP1_114	AG2	
NA	MGTTXP0_116	K2	
NA	MGTAVTTTX_116	K3	
NA	MGTTXN0_116	L2	
NA	MGTRXP0_116	L1	
NA	MGTAVTTRX_116	L3	
NA	MGTRXN0_116	M1	
NA	MGTAVCCPLL_116	P3	
NA	MGTRXN1_116	N1	
NA	MGTREFCLKN_116	M3	
NA	MGTRXP1_116	P1	
NA	MGTREFCLKP_116	M4	
NA	MGTTXN1_116	P2	
NA	MGTAVTTTX_116	R3	
NA	MGTTXP1_116	R2	
NA	MGTTXP0_118	AH2	
NA	MGTAVTTTX_118	AH3	
NA	MGTTXN0_118	AJ2	
NA	MGTRXP0_118	AJ1	
NA	MGTAVTTRX_118	AJ3	
NA	MGTRXN0_118	AK1	
NA	MGTAVCCPLL_118	AM3	
NA	MGTRXN1_118	AL1	
NA	MGTREFCLKN_118	AK3	
NA	MGTRXP1_118	AM1	
NA	MGTREFCLKP_118	AK4	
NA	MGTTXN1_118	AM2	
NA	MGTAVTTTX_118	AN3	

Table 2-8: **FF1738 Package—FX100T, LX110T, FX130T, LX155T, FX200T, LX220T, SX240T, and LX330T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	MGTTXP1_118	AN2	
NA	MGTTXP0_120	D2	
NA	MGTAVTTTX_120	D3	
NA	MGTTXN0_120	E2	
NA	MGTRXP0_120	E1	
NA	MGTAVTTRX_120	E3	
NA	MGTRXN0_120	F1	
NA	MGTAVCCPLL_120	H3	
NA	MGTRXN1_120	G1	
NA	MGTREFCLKN_120	F3	
NA	MGTRXP1_120	H1	
NA	MGTREFCLKP_120	F4	
NA	MGTTXN1_120	H2	
NA	MGTAVTTTX_120	J3	
NA	MGTTXP1_120	J2	
NA	MGTTXP0_122	AP2	
NA	MGTAVTTTX_122	AP3	
NA	MGTTXN0_122	AR2	
NA	MGTRXP0_122	AR1	
NA	MGTAVTTRX_122	AR3	
NA	MGTRXN0_122	AT1	
NA	MGTAVCCPLL_122	AV3	
NA	MGTRXN1_122	AU1	
NA	MGTREFCLKN_122	AT3	
NA	MGTRXP1_122	AV1	
NA	MGTREFCLKP_122	AT4	
NA	MGTTXN1_122	AV2	
NA	MGTAVTTTX_122	AW3	
NA	MGTTXP1_122	AW2	
NA	MGTTXP0_124	B6	
NA	MGTAVTTTX_124	C1	
NA	MGTTXN0_124	B5	

Table 2-8: **FF1738 Package—FX100T, LX110T, FX130T, LX155T, FX200T, LX220T, SX240T, and LX330T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	MGTRXP0_124	A5	
NA	MGTAVTTRX_124	C5	
NA	MGTRXN0_124	A4	
NA	MGTAVCCPLL_124	C2	
NA	MGTRXN1_124	A3	
NA	MGTREFCLKN_124	C3	
NA	MGTRXP1_124	A2	
NA	MGTREFCLKP_124	C4	
NA	MGTTXN1_124	B2	
NA	MGTAVTTTX_124	C6	
NA	MGTTXP1_124	B1	
NA	MGTTXP0_126	BA1	
NA	MGTAVTTTX_126	AY1	
NA	MGTTXN0_126	BA2	
NA	MGTRXP0_126	BB2	
NA	MGTAVTTRX_126	AY2	
NA	MGTRXN0_126	BB3	
NA	MGTAVCCPLL_126	AY5	
NA	MGTRXN1_126	BB4	
NA	MGTREFCLKN_126	AY4	
NA	MGTRXP1_126	BB5	
NA	MGTREFCLKP_126	AW4	
NA	MGTTXN1_126	BA5	
NA	MGTAVTTTX_126	AY6	
NA	MGTTXP1_126	BA6	
NA	MGTTXP0_128	B12	FX100T, LX110T, LX155T, LX220T
NA	MGTAVTTTX_128	C12	FX100T, LX110T, LX155T, LX220T
NA	MGTTXN0_128	B11	FX100T, LX110T, LX155T, LX220T
NA	MGTRXP0_128	A11	FX100T, LX110T, LX155T, LX220T

Table 2-8: **FF1738 Package—FX100T, LX110T, FX130T, LX155T, FX200T, LX220T, SX240T, and LX330T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	MGTAVTTRX_128	C11	FX100T, LX110T, LX155T, LX220T
NA	MGTRXN0_128	A10	FX100T, LX110T, LX155T, LX220T
NA	MGTAVCCPLL_128	C8	FX100T, LX110T, LX155T, LX220T
NA	MGTRXN1_128	A9	FX100T, LX110T, LX155T, LX220T
NA	MGTREFCLKN_128	C10	FX100T, LX110T, LX155T, LX220T
NA	MGTRXP1_128	A8	FX100T, LX110T, LX155T, LX220T
NA	MGTREFCLKP_128	D10	FX100T, LX110T, LX155T, LX220T
NA	MGTTXN1_128	B8	FX100T, LX110T, LX155T, LX220T
NA	MGTAVTTTX_128	C7	FX100T, LX110T, LX155T, LX220T
NA	MGTTXP1_128	B7	FX100T, LX110T, LX155T, LX220T
NA	MGTTXP0_130	BA7	FX100T, LX110T, LX155T, LX220T
NA	MGTAVTTTX_130	AY12	FX100T, LX110T, LX155T, LX220T
NA	MGTTXN0_130	BA8	FX100T, LX110T, LX155T, LX220T
NA	MGTRXP0_130	BB8	FX100T, LX110T, LX155T, LX220T
NA	MGTAVTTRX_130	AY8	FX100T, LX110T, LX155T, LX220T
NA	MGTRXN0_130	BB9	FX100T, LX110T, LX155T, LX220T
NA	MGTAVCCPLL_130	AY11	FX100T, LX110T, LX155T, LX220T
NA	MGTRXN1_130	BB10	FX100T, LX110T, LX155T, LX220T
NA	MGTREFCLKN_130	AY9	FX100T, LX110T, LX155T, LX220T
NA	MGTRXP1_130	BB11	FX100T, LX110T, LX155T, LX220T

Table 2-8: **FF1738 Package—FX100T, LX110T, FX130T, LX155T, FX200T, LX220T, SX240T, and LX330T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	MGTREFCLKP_130	AW9	FX100T, LX110T, LX155T, LX220T
NA	MGTTXN1_130	BA11	FX100T, LX110T, LX155T, LX220T
NA	MGTAVTTTX_130	AY7	FX100T, LX110T, LX155T, LX220T
NA	MGTTXP1_130	BA12	FX100T, LX110T, LX155T, LX220T
NA	MGTTXP0_132	B18	FX100T, LX110T, FX130T, LX155T, LX220T
NA	MGTAVTTTX_132	C13	FX100T, LX110T, FX130T, LX155T, LX220T
NA	MGTTXN0_132	B17	FX100T, LX110T, FX130T, LX155T, LX220T
NA	MGTRXP0_132	A17	FX100T, LX110T, FX130T, LX155T, LX220T
NA	MGTAVTTRX_132	C17	FX100T, LX110T, FX130T, LX155T, LX220T
NA	MGTRXN0_132	A16	FX100T, LX110T, FX130T, LX155T, LX220T
NA	MGTAVCCPLL_132	C14	FX100T, LX110T, FX130T, LX155T, LX220T
NA	MGTRXN1_132	A15	FX100T, LX110T, FX130T, LX155T, LX220T
NA	MGTREFCLKN_132	C16	FX100T, LX110T, FX130T, LX155T, LX220T
NA	MGTRXP1_132	A14	FX100T, LX110T, FX130T, LX155T, LX220T
NA	MGTREFCLKP_132	D16	FX100T, LX110T, FX130T, LX155T, LX220T
NA	MGTTXN1_132	B14	FX100T, LX110T, FX130T, LX155T, LX220T
NA	MGTAVTTTX_132	C18	FX100T, LX110T, FX130T, LX155T, LX220T
NA	MGTTXP1_132	B13	FX100T, LX110T, FX130T, LX155T, LX220T
NA	MGTTXP0_134	BA13	FX100T, LX110T, FX130T, LX155T, LX220T
NA	MGTAVTTTX_134	AY13	FX100T, LX110T, FX130T, LX155T, LX220T

Table 2-8: **FF1738 Package—FX100T, LX110T, FX130T, LX155T, FX200T, LX220T, SX240T, and LX330T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	MGTTXN0_134	BA14	FX100T, LX110T, FX130T, LX155T, LX220T
NA	MGTRXP0_134	BB14	FX100T, LX110T, FX130T, LX155T, LX220T
NA	MGTAVTTRX_134	AY14	FX100T, LX110T, FX130T, LX155T, LX220T
NA	MGTRXN0_134	BB15	FX100T, LX110T, FX130T, LX155T, LX220T
NA	MGTAVCCPLL_134	AY17	FX100T, LX110T, FX130T, LX155T, LX220T
NA	MGTRXN1_134	BB16	FX100T, LX110T, FX130T, LX155T, LX220T
NA	MGTREFCLKN_134	AY15	FX100T, LX110T, FX130T, LX155T, LX220T
NA	MGTRXP1_134	BB17	FX100T, LX110T, FX130T, LX155T, LX220T
NA	MGTREFCLKP_134	AW15	FX100T, LX110T, FX130T, LX155T, LX220T
NA	MGTTXN1_134	BA17	FX100T, LX110T, FX130T, LX155T, LX220T
NA	MGTAVTTTX_134	AY18	FX100T, LX110T, FX130T, LX155T, LX220T
NA	MGTTXP1_134	BA18	FX100T, LX110T, FX130T, LX155T, LX220T
NA	GND	F2	
NA	GND	G2	
NA	GND	M2	
NA	GND	N2	
NA	GND	V2	
NA	GND	W2	
NA	GND	AD2	
NA	GND	AE2	
NA	GND	AK2	
NA	GND	AL2	
NA	GND	AT2	
NA	GND	AU2	
NA	GND	B3	

Table 2-8: **FF1738 Package—FX100T, LX110T, FX130T, LX155T, FX200T, LX220T, SX240T, and LX330T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	BA3	
NA	GND	B4	
NA	GND	E4	
NA	GND	H4	
NA	GND	J4	
NA	GND	L4	
NA	GND	P4	
NA	GND	U4	
NA	GND	Y4	
NA	GND	AC4	
NA	GND	AF4	
NA	GND	AJ4	
NA	GND	AM4	
NA	GND	AP4	
NA	GND	AR4	
NA	GND	AV4	
NA	GND	BA4	
NA	GND	G5	
NA	GND	M5	
NA	GND	U5	
NA	GND	AB5	
NA	GND	AG5	
NA	GND	AM5	
NA	GND	AU5	
NA	GND	D6	
NA	GND	K6	
NA	GND	Y6	
NA	GND	AK6	
NA	GND	AR6	
NA	GND	AW6	
NA	GND	N7	
NA	GND	AC7	

Table 2-8: **FF1738 Package—FX100T, LX110T, FX130T, LX155T, FX200T, LX220T, SX240T, and LX330T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	AN7	
NA	GND	D8	
NA	GND	F8	
NA	GND	T8	
NA	GND	AF8	
NA	GND	AT8	
NA	GND	AW8	
NA	GND	B9	
NA	GND	J9	
NA	GND	W9	
NA	GND	AJ9	
NA	GND	BA9	
NA	GND	B10	
NA	GND	M10	
NA	GND	AB10	
NA	GND	AM10	
NA	GND	BA10	
NA	GND	D11	
NA	GND	E11	
NA	GND	K11	
NA	GND	R11	
NA	GND	Y11	
NA	GND	AC11	
NA	GND	AE11	
NA	GND	AR11	
NA	GND	AW11	
NA	GND	H12	
NA	GND	N12	
NA	GND	T12	
NA	GND	V12	
NA	GND	Y12	
NA	GND	AB12	

Table 2-8: **FF1738 Package—FX100T, LX110T, FX130T, LX155T, FX200T, LX220T, SX240T, and LX330T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	AD12	
NA	GND	AH12	
NA	GND	AN12	
NA	GND	AV12	
NA	GND	L13	
NA	GND	R13	
NA	GND	U13	
NA	GND	W13	
NA	GND	AA13	
NA	GND	AC13	
NA	GND	AE13	
NA	GND	AG13	
NA	GND	AJ13	
NA	GND	AL13	
NA	GND	D14	
NA	GND	P14	
NA	GND	V14	
NA	GND	Y14	
NA	GND	AB14	
NA	GND	AD14	
NA	GND	AF14	
NA	GND	AJ14	
NA	GND	AP14	
NA	GND	AW14	
NA	GND	B15	
NA	GND	G15	
NA	GND	M15	
NA	GND	U15	
NA	GND	W15	
NA	GND	AA15	
NA	GND	AC15	
NA	GND	AE15	

Table 2-8: **FF1738 Package—FX100T, LX110T, FX130T, LX155T, FX200T, LX220T, SX240T, and LX330T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	AG15	
NA	GND	AM15	
NA	GND	AU15	
NA	GND	BA15	
NA	GND	B16	
NA	GND	E16	
NA	GND	K16	
NA	GND	P16	
NA	GND	T16	
NA	GND	V16	
NA	GND	Y16	
NA	GND	AB16	
NA	GND	AD16	
NA	GND	AF16	
NA	GND	AK16	
NA	GND	BA16	
NA	GND	D17	
NA	GND	N17	
NA	GND	R17	
NA	GND	U17	
NA	GND	W17	
NA	GND	AA17	
NA	GND	AC17	
NA	GND	AE17	
NA	GND	AG17	
NA	GND	AJ17	
NA	GND	AN17	
NA	GND	AW17	
NA	GND	F18	
NA	GND	L18	
NA	GND	T18	
NA	GND	V18	

Table 2-8: **FF1738 Package—FX100T, LX110T, FX130T, LX155T, FX200T, LX220T, SX240T, and LX330T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	Y18	
NA	GND	AB18	
NA	GND	AD18	
NA	GND	AF18	
NA	GND	AH18	
NA	GND	AL18	
NA	GND	AT18	
NA	GND	A19	
NA	GND	B19	
NA	GND	C19	
NA	GND	J19	
NA	GND	P19	
NA	GND	R19	
NA	GND	U19	
NA	GND	W19	
NA	GND	AA19	
NA	GND	AC19	
NA	GND	AE19	
NA	GND	AG19	
NA	GND	AJ19	
NA	GND	AW19	
NA	GND	BB19	
NA	GND	B20	
NA	GND	M20	
NA	GND	T20	
NA	GND	V20	
NA	GND	Y20	
NA	GND	AB20	
NA	GND	AD20	
NA	GND	AF20	
NA	GND	AH20	
NA	GND	AM20	

Table 2-8: **FF1738 Package—FX100T, LX110T, FX130T, LX155T, FX200T, LX220T, SX240T, and LX330T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	E21	
NA	GND	K21	
NA	GND	R21	
NA	GND	U21	
NA	GND	W21	
NA	GND	AE21	
NA	GND	AG21	
NA	GND	AK21	
NA	GND	AR21	
NA	GND	H22	
NA	GND	P22	
NA	GND	T22	
NA	GND	V22	
NA	GND	AD22	
NA	GND	AF22	
NA	GND	AH22	
NA	GND	AN22	
NA	GND	AV22	
NA	GND	A23	
NA	GND	L23	
NA	GND	R23	
NA	GND	U23	
NA	GND	W23	
NA	GND	AA23	
NA	GND	AC23	
NA	GND	AE23	
NA	GND	AG23	
NA	GND	AJ23	
NA	GND	AL23	
NA	GND	BA23	
NA	GND	D24	
NA	GND	J24	

Table 2-8: **FF1738 Package—FX100T, LX110T, FX130T, LX155T, FX200T, LX220T, SX240T, and LX330T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	P24	
NA	GND	T24	
NA	GND	V24	
NA	GND	Y24	
NA	GND	AB24	
NA	GND	AD24	
NA	GND	AF24	
NA	GND	AH24	
NA	GND	AP24	
NA	GND	G25	
NA	GND	M25	
NA	GND	R25	
NA	GND	U25	
NA	GND	W25	
NA	GND	AA25	
NA	GND	AC25	
NA	GND	AE25	
NA	GND	AG25	
NA	GND	AJ25	
NA	GND	AM25	
NA	GND	AU25	
NA	GND	BB25	
NA	GND	K26	
NA	GND	T26	
NA	GND	V26	
NA	GND	Y26	
NA	GND	AB26	
NA	GND	AD26	
NA	GND	AF26	
NA	GND	AH26	
NA	GND	AK26	
NA	GND	AY26	

Table 2-8: **FF1738 Package—FX100T, LX110T, FX130T, LX155T, FX200T, LX220T, SX240T, and LX330T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	C27	
NA	GND	N27	
NA	GND	R27	
NA	GND	U27	
NA	GND	W27	
NA	GND	AA27	
NA	GND	AC27	
NA	GND	AE27	
NA	GND	AG27	
NA	GND	AJ27	
NA	GND	AN27	
NA	GND	A28	
NA	GND	F28	
NA	GND	L28	
NA	GND	T28	
NA	GND	V28	
NA	GND	Y28	
NA	GND	AB28	
NA	GND	AD28	
NA	GND	AF28	
NA	GND	AH28	
NA	GND	AT28	
NA	GND	J29	
NA	GND	P29	
NA	GND	U29	
NA	GND	W29	
NA	GND	AA29	
NA	GND	AC29	
NA	GND	AE29	
NA	GND	AJ29	
NA	GND	AP29	
NA	GND	AW29	

Table 2-8: **FF1738 Package—FX100T, LX110T, FX130T, LX155T, FX200T, LX220T, SX240T, and LX330T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	B30	
NA	GND	M30	
NA	GND	V30	
NA	GND	Y30	
NA	GND	AB30	
NA	GND	AD30	
NA	GND	AM30	
NA	GND	BB30	
NA	GND	E31	
NA	GND	K31	
NA	GND	R31	
NA	GND	W31	
NA	GND	AA31	
NA	GND	AC31	
NA	GND	AE31	
NA	GND	AK31	
NA	GND	AR31	
NA	GND	H32	
NA	GND	N32	
NA	GND	V32	
NA	GND	AC32	
NA	GND	AH32	
NA	GND	AN32	
NA	GND	AV32	
NA	GND	A33	
NA	GND	L33	
NA	GND	T33	
NA	GND	AA33	
NA	GND	AF33	
NA	GND	AL33	
NA	GND	BA33	
NA	GND	D34	

Table 2-8: **FF1738 Package—FX100T, LX110T, FX130T, LX155T, FX200T, LX220T, SX240T, and LX330T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	P34	
NA	GND	W34	
NA	GND	AD34	
NA	GND	AP34	
NA	GND	G35	
NA	GND	M35	
NA	GND	U35	
NA	GND	AG35	
NA	GND	AU35	
NA	GND	BB35	
NA	GND	K36	
NA	GND	Y36	
NA	GND	AK36	
NA	GND	AY36	
NA	GND	C37	
NA	GND	N37	
NA	GND	AC37	
NA	GND	AN37	
NA	GND	A38	
NA	GND	F38	
NA	GND	T38	
NA	GND	AF38	
NA	GND	AT38	
NA	GND	BA38	
NA	GND	J39	
NA	GND	W39	
NA	GND	AJ39	
NA	GND	AW39	
NA	GND	B40	
NA	GND	M40	
NA	GND	AB40	
NA	GND	AM40	

Table 2-8: **FF1738 Package—FX100T, LX110T, FX130T, LX155T, FX200T, LX220T, SX240T, and LX330T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	BB40	
NA	GND	E41	
NA	GND	R41	
NA	GND	AE41	
NA	GND	AR41	
NA	GND	AY41	
NA	GND	C42	
NA	GND	H42	
NA	GND	N42	
NA	GND	V42	
NA	GND	AC42	
NA	GND	AH42	
NA	GND	AN42	
NA	GND	AV42	
NA	VCCAUX	R12	
NA	VCCAUX	U12	
NA	VCCAUX	W12	
NA	VCCAUX	AA12	
NA	VCCAUX	AC12	
NA	VCCAUX	AE12	
NA	VCCAUX	AJ12	
NA	VCCAUX	T13	
NA	VCCAUX	AF13	
NA	VCCAUX	AH13	
NA	VCCAUX	T29	
NA	VCCAUX	AF29	
NA	VCCAUX	U30	
NA	VCCAUX	W30	
NA	VCCAUX	AA30	
NA	VCCAUX	AC30	
NA	VCCAUX	AE30	
NA	VCCAUX	Y31	

Table 2-8: **FF1738 Package—FX100T, LX110T, FX130T, LX155T, FX200T, LX220T, SX240T, and LX330T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	VCCAUX	AB31	
NA	VCCAUX	AD31	
NA	VCCINT	V13	
NA	VCCINT	Y13	
NA	VCCINT	AB13	
NA	VCCINT	AD13	
NA	VCCINT	U14	
NA	VCCINT	W14	
NA	VCCINT	AA14	
NA	VCCINT	AC14	
NA	VCCINT	AE14	
NA	VCCINT	AG14	
NA	VCCINT	T15	
NA	VCCINT	V15	
NA	VCCINT	Y15	
NA	VCCINT	AB15	
NA	VCCINT	AD15	
NA	VCCINT	AF15	
NA	VCCINT	R16	
NA	VCCINT	U16	
NA	VCCINT	W16	
NA	VCCINT	AA16	
NA	VCCINT	AC16	
NA	VCCINT	AE16	
NA	VCCINT	AG16	
NA	VCCINT	T17	
NA	VCCINT	V17	
NA	VCCINT	Y17	
NA	VCCINT	AB17	
NA	VCCINT	AD17	
NA	VCCINT	AF17	
NA	VCCINT	AH17	

Table 2-8: **FF1738 Package—FX100T, LX110T, FX130T, LX155T, FX200T, LX220T, SX240T, and LX330T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	VCCINT	R18	
NA	VCCINT	U18	
NA	VCCINT	W18	
NA	VCCINT	AA18	
NA	VCCINT	AC18	
NA	VCCINT	AE18	
NA	VCCINT	AG18	
NA	VCCINT	AJ18	
NA	VCCINT	T19	
NA	VCCINT	V19	
NA	VCCINT	Y19	
NA	VCCINT	AB19	
NA	VCCINT	AD19	
NA	VCCINT	AF19	
NA	VCCINT	AH19	
NA	VCCINT	R20	
NA	VCCINT	U20	
NA	VCCINT	W20	
NA	VCCINT	AA20	
NA	VCCINT	AC20	
NA	VCCINT	AE20	
NA	VCCINT	AG20	
NA	VCCINT	AJ20	
NA	VCCINT	P21	
NA	VCCINT	T21	
NA	VCCINT	V21	
NA	VCCINT	AD21	
NA	VCCINT	AF21	
NA	VCCINT	AH21	
NA	VCCINT	R22	
NA	VCCINT	U22	
NA	VCCINT	W22	

Table 2-8: **FF1738 Package—FX100T, LX110T, FX130T, LX155T, FX200T, LX220T, SX240T, and LX330T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	VCCINT	AE22	
NA	VCCINT	AG22	
NA	VCCINT	P23	
NA	VCCINT	T23	
NA	VCCINT	V23	
NA	VCCINT	Y23	
NA	VCCINT	AB23	
NA	VCCINT	AD23	
NA	VCCINT	AF23	
NA	VCCINT	AH23	
NA	VCCINT	R24	
NA	VCCINT	U24	
NA	VCCINT	W24	
NA	VCCINT	AA24	
NA	VCCINT	AC24	
NA	VCCINT	AE24	
NA	VCCINT	AG24	
NA	VCCINT	AJ24	
NA	VCCINT	T25	
NA	VCCINT	V25	
NA	VCCINT	Y25	
NA	VCCINT	AB25	
NA	VCCINT	AD25	
NA	VCCINT	AF25	
NA	VCCINT	AH25	
NA	VCCINT	R26	
NA	VCCINT	U26	
NA	VCCINT	W26	
NA	VCCINT	AA26	
NA	VCCINT	AC26	
NA	VCCINT	AE26	
NA	VCCINT	AG26	

Table 2-8: **FF1738 Package—FX100T, LX110T, FX130T, LX155T, FX200T, LX220T, SX240T, and LX330T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	VCCINT	T27	
NA	VCCINT	V27	
NA	VCCINT	Y27	
NA	VCCINT	AB27	
NA	VCCINT	AD27	
NA	VCCINT	AF27	
NA	VCCINT	AH27	
NA	VCCINT	R28	
NA	VCCINT	U28	
NA	VCCINT	W28	
NA	VCCINT	AA28	
NA	VCCINT	AC28	
NA	VCCINT	AE28	
NA	VCCINT	AG28	
NA	VCCINT	V29	
NA	VCCINT	Y29	
NA	VCCINT	AB29	
NA	VCCINT	AD29	
0	VCCO_0	AL28	
0	VCCO_0	AG30	
1	VCCO_1	F13	
1	VCCO_1	J14	
2	VCCO_2	AR26	
2	VCCO_2	AV27	
3	VCCO_3	E26	
3	VCCO_3	H27	
4	VCCO_4	AT13	
4	VCCO_4	AR16	
5	VCCO_5	C22	
5	VCCO_5	F23	
5	VCCO_5	B25	
6	VCCO_6	AY21	

Table 2-8: **FF1738 Package—FX100T, LX110T, FX130T, LX155T, FX200T, LX220T, SX240T, and LX330T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
6	VCCO_6	AT23	
6	VCCO_6	AW24	
7	VCCO_7	H17	
7	VCCO_7	D19	
7	VCCO_7	G20	
8	VCCO_8	AV17	
8	VCCO_8	AP19	
8	VCCO_8	AU20	
11	VCCO_11	V37	
11	VCCO_11	AA38	
11	VCCO_11	Y41	
12	VCCO_12	V7	
12	VCCO_12	AA8	
12	VCCO_12	U10	
13	VCCO_13	AB35	
13	VCCO_13	AE36	
13	VCCO_13	AD39	
15	VCCO_15	R36	
15	VCCO_15	P39	
15	VCCO_15	U40	
17	VCCO_17	AH37	
17	VCCO_17	AG40	
17	VCCO_17	AK41	
18	VCCO_18	AE6	
18	VCCO_18	AD9	
18	VCCO_18	AG10	
19	VCCO_19	L38	
19	VCCO_19	G40	
19	VCCO_19	K41	
20	VCCO_20	R6	
20	VCCO_20	L8	
20	VCCO_20	P9	

Table 2-8: **FF1738 Package—FX100T, LX110T, FX130T, LX155T, FX200T, LX220T, SX240T, and LX330T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
21	VCCO_21	AJ34	
21	VCCO_21	AM35	
21	VCCO_21	AL38	
23	VCCO_23	E36	
23	VCCO_23	H37	
23	VCCO_23	D39	
24	VCCO_24	E6	
24	VCCO_24	H7	
24	VCCO_24	G10	
25	VCCO_25	AR36	
25	VCCO_25	AP39	
25	VCCO_25	AU40	
26	VCCO_26	AH7	
26	VCCO_26	AL8	
26	VCCO_26	AK11	
27	VCCO_27	F33	
27	VCCO_27	J34	
27	VCCO_27	B35	
29	VCCO_29	AT33	
29	VCCO_29	AW34	
29	VCCO_29	AV37	
31	VCCO_31	D29	
31	VCCO_31	G30	
31	VCCO_31	C32	
33	VCCO_33	BA28	
33	VCCO_33	AU30	
33	VCCO_33	AY31	
34	VCCO_34	AV7	
34	VCCO_34	AP9	
34	VCCO_34	AU10	
NA	MGTAVCC_112	W3	
NA	MGTAVCC_112	W4	

Table 2-8: **FF1738 Package—FX100T, LX110T, FX130T, LX155T, FX200T, LX220T, SX240T, and LX330T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	MGTAVCC_114	AE3	
NA	MGTAVCC_114	AE4	
NA	MGTAVCC_116	N3	
NA	MGTAVCC_116	N4	
NA	MGTAVCC_118	AL3	
NA	MGTAVCC_118	AL4	
NA	MGTAVCC_120	G3	
NA	MGTAVCC_120	G4	
NA	MGTAVCC_122	AU3	
NA	MGTAVCC_122	AU4	
NA	MGTAVCC_124	D4	
NA	MGTAVCC_124	D5	
NA	MGTAVCC_126	AW5	
NA	MGTAVCC_126	AY3	
NA	MGTAVCC_128	C9	LX110T, LX155T, LX220T, FX100T
NA	MGTAVCC_128	D9	LX110T, LX155T, LX220T, FX100T
NA	MGTAVCC_130	AW10	LX110T, LX155T, LX220T, FX100T
NA	MGTAVCC_130	AY10	LX110T, LX155T, LX220T, FX100T
NA	MGTAVCC_132	C15	LX110T, LX155T, LX220T, FX100T, FX130T
NA	MGTAVCC_132	D15	LX110T, LX155T, LX220T, FX100T, FX130T
NA	MGTAVCC_134	AW16	LX110T, LX155T, LX220T, FX100T, FX130T
NA	MGTAVCC_134	AY16	LX110T, LX155T, LX220T, FX100T, FX130T
NA	FLOAT	AA4	

Notes:

1. Do not connect a single-ended clock to the N-side of the differential clock pair of pins, for example, IO_L3N_GC_3.
2. Do not connect a single-ended clock to the N-side of clock capable pins, for example, IO_L8N_CC_11.
3. RSVD pins must be tied to GND (logic 0).

FF1759 Package—TX150T and TX240T

Table 2-9: **FF1759 Package—TX150T and TX240T**

Bank	Pin Description	Pin Number	No Connect (NC)
0	DXP_0	AC22	
0	DXN_0	AC21	
0	AVDD_0	Y22	
0	AVSS_0	Y21	
0	VP_0	AA22	
0	VN_0	AB21	
0	VREFP_0	AB22	
0	VREFN_0	AA21	
0	VBATT_0	R28	
0	PROGRAM_B_0	R29	
0	HSWAPEN_0	T29	
0	D_IN_0	R15	
0	DONE_0	R14	
0	CCLK_0	AJ16	
0	INIT_B_0	T14	
0	CS_B_0	T30	
0	RDWR_B_0	P15	
0	RSVD(3)	U29	
0	RSVD(3)	AF29	
0	TCK_0	AF16	
0	M0_0	AJ28	
0	M2_0	AH28	
0	M1_0	AJ27	
0	TMS_0	AF15	
0	TDI_0	AG16	
0	D_OUT_BUSY_0	AG29	
0	TDO_0	AH16	
1	IO_L0P_A19_1	P26	
1	IO_L0N_A18_1	P25	
1	IO_L1P_A17_1	N19	
1	IO_L1N_A16_1	P18	

Table 2-9: **FF1759 Package—TX150T and TX240T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
1	IO_L2P_A15_D31_1	N26	
1	IO_L2N_A14_D30_1	N25	
1	IO_L3P_A13_D29_1	N18	
1	IO_L3N_A12_D28_1	P17	
1	IO_L4P_A11_D27_1	N28	
1	IO_L4N_VREF_A10_D26_1	P27	
1	IO_L5P_A9_D25_1	L14	
1	IO_L5N_A8_D24_1	M14	
1	IO_L6P_A7_D23_1	M29	
1	IO_L6N_A6_D22_1	N29	
1	IO_L7P_A5_D21_1	M16	
1	IO_L7N_A4_D20_1	N16	
1	IO_L8P_CC_A3_D19_1	P28	
1	IO_L8N_CC_A2_D18_1(2)	R27	
1	IO_L9P_CC_A1_D17_1	N15	
1	IO_L9N_CC_A0_D16_1(2)	N14	
2	IO_L0P_CC_RS1_2	AJ17	
2	IO_L0N_CC_RS0_2(2)	AK17	
2	IO_L1P_CC_A25_2	AK28	
2	IO_L1N_CC_A24_2(2)	AK27	
2	IO_L2P_A23_2	AK18	
2	IO_L2N_A22_2	AJ18	
2	IO_L3P_A21_2	AL27	
2	IO_L3N_A20_2	AM27	
2	IO_L4P_FCS_B_2	AL17	
2	IO_L4N_VREF_FOE_B_MOSI_2	AM17	
2	IO_L5P_FWE_B_2	AR27	
2	IO_L5N_CSO_B_2	AP27	
2	IO_L6P_D7_2	AM18	
2	IO_L6N_D6_2	AM19	
2	IO_L7P_D5_2	AP26	
2	IO_L7N_D4_2	AN26	
2	IO_L8P_D3_2	AL19	

Table 2-9: **FF1759 Package—TX150T and TX240T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
2	IO_L8N_D2_FS2_2	AK19	
2	IO_L9P_D1_FS1_2	AP25	
2	IO_L9N_D0_FS0_2	AR25	
3	IO_L0P_CC_GC_3	L19	
3	IO_L0N_CC_GC_3(1)(2)	M19	
3	IO_L1P_CC_GC_3	N24	
3	IO_L1N_CC_GC_3(1)(2)	M24	
3	IO_L2P_GC_VRN_3	J15	
3	IO_L2N_GC_VRP_3(1)	J16	
3	IO_L3P_GC_3	M26	
3	IO_L3N_GC_3(1)	L25	
3	IO_L4P_GC_3	L15	
3	IO_L4N_GC_VREF_3(1)	K15	
3	IO_L5P_GC_3	L26	
3	IO_L5N_GC_3(1)	L27	
3	IO_L6P_GC_3	M17	
3	IO_L6N_GC_3(1)	M18	
3	IO_L7P_GC_3	K27	
3	IO_L7N_GC_3(1)	K28	
3	IO_L8P_GC_3	L16	
3	IO_L8N_GC_3(1)	L17	
3	IO_L9P_GC_3	M28	
3	IO_L9N_GC_3(1)	M27	
4	IO_L0P_GC_D15_4	AL26	
4	IO_L0N_GC_D14_4(1)	AM26	
4	IO_L1P_GC_D13_4	AN20	
4	IO_L1N_GC_D12_4(1)	AN19	
4	IO_L2P_GC_D11_4	AN25	
4	IO_L2N_GC_D10_4(1)	AM24	
4	IO_L3P_GC_D9_4	AR20	
4	IO_L3N_GC_D8_4(1)	AT20	
4	IO_L4P_GC_4	AJ25	
4	IO_L4N_GC_VREF_4(1)	AK25	

Table 2-9: **FF1759 Package—TX150T and TX240T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
4	IO_L5P_GC_4	AP21	
4	IO_L5N_GC_4(1)	AP20	
4	IO_L6P_GC_4	AL25	
4	IO_L6N_GC_4(1)	AL24	
4	IO_L7P_GC_VRN_4	AL21	
4	IO_L7N_GC_VRP_4(1)	AM21	
4	IO_L8P_CC_GC_4	AK23	
4	IO_L8N_CC_GC_4(1)(2)	AK24	
4	IO_L9P_CC_GC_4	AK20	
4	IO_L9N_CC_GC_4(1)(2)	AL20	
5	IO_L0P_5	K23	
5	IO_L0N_5	J23	
5	IO_L1P_5	E20	
5	IO_L1N_5	F20	
5	IO_L2P_5	K24	
5	IO_L2N_5	L24	
5	IO_L3P_5	H20	
5	IO_L3N_5	H19	
5	IO_L4P_5	H23	
5	IO_L4N_VREF_5	H24	
5	IO_L5P_5	F19	
5	IO_L5N_5	G19	
5	IO_L6P_5	G24	
5	IO_L6N_5	H25	
5	IO_L7P_5	G18	
5	IO_L7N_5	G17	
5	IO_L8P_CC_5	F26	
5	IO_L8N_CC_5(2)	G26	
5	IO_L9P_CC_5	J17	
5	IO_L9N_CC_5(2)	K17	
5	IO_L10P_CC_5	K18	
5	IO_L10N_CC_5(2)	K19	
5	IO_L11P_CC_5	K25	

Table 2-9: **FF1759 Package—TX150T and TX240T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
5	IO_L11N_CC_5[2]	J25	
5	IO_L12P_VRN_5	J18	
5	IO_L12N_VRP_5	H18	
5	IO_L13P_5	G27	
5	IO_L13N_5	F27	
5	IO_L14P_5	E19	
5	IO_L14N_VREF_5	E18	
5	IO_L15P_5	J26	
5	IO_L15N_5	H26	
5	IO_L16P_5	F17	
5	IO_L16N_5	F16	
5	IO_L17P_5	H28	
5	IO_L17N_5	G28	
5	IO_L18P_5	H16	
5	IO_L18N_5	G16	
5	IO_L19P_5	J28	
5	IO_L19N_5	J27	
6	IO_L0P_6	AR24	
6	IO_L0N_6	AT24	
6	IO_L1P_6	AV18	
6	IO_L1N_6	AV19	
6	IO_L2P_6	AV24	
6	IO_L2N_6	AU24	
6	IO_L3P_6	BA22	
6	IO_L3N_6	BB21	
6	IO_L4P_6	BB22	
6	IO_L4N_VREF_6	BB23	
6	IO_L5P_6	BA21	
6	IO_L5N_6	AY22	
6	IO_L6P_6	AV23	
6	IO_L6N_6	AU23	
6	IO_L7P_6	AT19	
6	IO_L7N_6	AU19	

Table 2-9: **FF1759 Package—TX150T and TX240T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
6	IO_L8P_CC_6	AM23	
6	IO_L8N_CC_6(2)	AN24	
6	IO_L9P_CC_6	AV20	
6	IO_L9N_CC_6(2)	AW20	
6	IO_L10P_CC_6	AN21	
6	IO_L10N_CC_6(2)	AM22	
6	IO_L11P_CC_6	AW23	
6	IO_L11N_CC_6(2)	AY23	
6	IO_L12P_VRN_6	AL22	
6	IO_L12N_VRP_6	AK22	
6	IO_L13P_6	AN23	
6	IO_L13N_6	AP23	
6	IO_L14P_6	BA20	
6	IO_L14N_VREF_6	AY20	
6	IO_L15P_6	AR23	
6	IO_L15N_6	AT22	
6	IO_L16P_6	AW21	
6	IO_L16N_6	AW22	
6	IO_L17P_6	AR22	
6	IO_L17N_6	AP22	
6	IO_L18P_6	AV21	
6	IO_L18N_6	AU22	
6	IO_L19P_6	AU21	
6	IO_L19N_6	AT21	
7	IO_L0P_7	J22	
7	IO_L0N_7	J21	
7	IO_L1P_7	N21	
7	IO_L1N_7	M21	
7	IO_L2P_7	M22	
7	IO_L2N_7	L22	
7	IO_L3P_7	D23	
7	IO_L3N_7	E22	
7	IO_L4P_7	D22	

Table 2-9: **FF1759 Package—TX150T and TX240T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
7	IO_L4N_VREF_7	C23	
7	IO_L5P_7	F22	
7	IO_L5N_7	G22	
7	IO_L6P_7	C21	
7	IO_L6N_7	D21	
7	IO_L7P_7	K22	
7	IO_L7N_7	L21	
7	IO_L8P_CC_7	B22	
7	IO_L8N_CC_7(2)	B23	
7	IO_L9P_CC_7	F21	
7	IO_L9N_CC_7(2)	G21	
7	IO_L10P_CC_7	J20	
7	IO_L10N_CC_7(2)	H21	
7	IO_L11P_CC_7	B21	
7	IO_L11N_CC_7(2)	A22	
7	IO_L12P_VRN_7	D20	
7	IO_L12N_VRP_7	C20	
7	IO_L13P_7	G23	
7	IO_L13N_7	F24	
7	IO_L14P_7	A20	
7	IO_L14N_VREF_7	A21	
7	IO_L15P_7	M23	
7	IO_L15N_7	N23	
7	IO_L16P_7	L20	
7	IO_L16N_7	K20	
7	IO_L17P_7	E24	
7	IO_L17N_7	E23	
7	IO_L18P_7	P21	
7	IO_L18N_7	P22	
7	IO_L19P_7	F25	
7	IO_L19N_7	E25	
11	IO_L0P_11	Y30	
11	IO_L0N_11	Y29	

Table 2-9: **FF1759 Package—TX150T and TX240T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
11	IO_L1P_11	W35	
11	IO_L1N_11	W36	
11	IO_L2P_11	AA37	
11	IO_L2N_11	Y37	
11	IO_L3P_11	W37	
11	IO_L3N_11	V36	
11	IO_L4P_11	AA36	
11	IO_L4N_VREF_11	AB37	
11	IO_L5P_11	W33	
11	IO_L5N_11	W32	
11	IO_L6P_11	Y32	
11	IO_L6N_11	AA32	
11	IO_L7P_11	V35	
11	IO_L7N_11	V34	
11	IO_L8P_CC_11	Y33	
11	IO_L8N_CC_11(2)	Y34	
11	IO_L9P_CC_11	U37	
11	IO_L9N_CC_11(2)	T37	
11	IO_L10P_CC_SM15P_11	W30	
11	IO_L10N_CC_SM15N_11(2)	W31	
11	IO_L11P_CC_SM14P_11	AA30	
11	IO_L11N_CC_SM14N_11(2)	AA31	
11	IO_L12P_VRN_11	T35	
11	IO_L12N_VRP_11	T36	
11	IO_L13P_11	AA35	
11	IO_L13N_11	Y35	
11	IO_L14P_11	U33	
11	IO_L14N_VREF_11	U34	
11	IO_L15P_SM13P_11	AC36	
11	IO_L15N_SM13N_11	AB36	
11	IO_L16P_SM12P_11	U32	
11	IO_L16N_SM12N_11	V33	
11	IO_L17P_SM11P_11	AB34	

Table 2-9: **FF1759 Package—TX150T and TX240T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
11	IO_L17N_SM11N_11	AA34	
11	IO_L18P_SM10P_11	U31	
11	IO_L18N_SM10N_11	V31	
11	IO_L19P_SM9P_11	AB32	
11	IO_L19N_SM9N_11	AB31	
12	IO_L0P_12	R5	
12	IO_L0N_12	P5	
12	IO_L1P_12	Y7	
12	IO_L1N_12	Y8	
12	IO_L2P_12	T6	
12	IO_L2N_12	T5	
12	IO_L3P_12	AA9	
12	IO_L3N_12	Y10	
12	IO_L4P_12	V6	
12	IO_L4N_VREF_12	U6	
12	IO_L5P_12	AA7	
12	IO_L5N_12	AA6	
12	IO_L6P_12	W8	
12	IO_L6N_12	Y9	
12	IO_L7P_12	AB6	
12	IO_L7N_12	AC6	
12	IO_L8P_CC_12	W7	
12	IO_L8N_CC_12(2)	W6	
12	IO_L9P_CC_12	AB8	
12	IO_L9N_CC_12(2)	AB7	
12	IO_L10P_CC_12	AA11	
12	IO_L10N_CC_12(2)	AA10	
12	IO_L11P_CC_12	U7	
12	IO_L11N_CC_12(2)	T7	
12	IO_L12P_VRN_12	AC8	
12	IO_L12N_VRP_12	AB9	
12	IO_L13P_12	W11	
12	IO_L13N_12	W10	

Table 2-9: **FF1759 Package—TX150T and TX240T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
12	IO_L14P_12	AC9	
12	IO_L14N_VREF_12	AD8	
12	IO_L15P_12	V8	
12	IO_L15N_12	V9	
12	IO_L16P_12	AD11	
12	IO_L16N_12	AC10	
12	IO_L17P_12	R7	
12	IO_L17N_12	P7	
12	IO_L18P_12	AC11	
12	IO_L18N_12	AB11	
12	IO_L19P_12	P6	
12	IO_L19N_12	N6	
13	IO_L0P_SM8P_13	AC35	
13	IO_L0N_SM8N_13	AC34	
13	IO_L1P_SM7P_13	AG32	
13	IO_L1N_SM7N_13	AG31	
13	IO_L2P_SM6P_13	AB33	
13	IO_L2N_SM6N_13	AC33	
13	IO_L3P_SM5P_13	AG34	
13	IO_L3N_SM5N_13	AG33	
13	IO_L4P_13	AD37	
13	IO_L4N_VREF_13	AD36	
13	IO_L5P_SM4P_13	AF32	
13	IO_L5N_SM4N_13	AF31	
13	IO_L6P_SM3P_13	AD35	
13	IO_L6N_SM3N_13	AE35	
13	IO_L7P_SM2P_13	AL37	
13	IO_L7N_SM2N_13	AL36	
13	IO_L8P_CC_SM1P_13	AC31	
13	IO_L8N_CC_SM1N_13(2)	AC30	
13	IO_L9P_CC_SM0P_13	AM38	
13	IO_L9N_CC_SM0N_13(2)	AN38	
13	IO_L10P_CC_13	AF34	

Table 2-9: **FF1759 Package—TX150T and TX240T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
13	IO_L10N_CC_13[2]	AE34	
13	IO_L11P_CC_13	AF37	
13	IO_L11N_CC_13[2]	AE37	
13	IO_L12P_VRN_13	AE33	
13	IO_L12N_VRP_13	AE32	
13	IO_L13P_13	AH38	
13	IO_L13N_13	AG38	
13	IO_L14P_13	AK37	
13	IO_L14N_VREF_13	AJ37	
13	IO_L15P_13	AD32	
13	IO_L15N_13	AD33	
13	IO_L16P_13	AD31	
13	IO_L16N_13	AD30	
13	IO_L17P_13	AF36	
13	IO_L17N_13	AF35	
13	IO_L18P_13	AJ36	
13	IO_L18N_13	AH36	
13	IO_L19P_13	AG36	
13	IO_L19N_13	AG37	
14	IO_L0P_14	AG12	
14	IO_L0N_14	AF12	
14	IO_L1P_14	AD7	
14	IO_L1N_14	AD6	
14	IO_L2P_14	AF11	
14	IO_L2N_14	AG11	
14	IO_L3P_14	AE8	
14	IO_L3N_14	AF7	
14	IO_L4P_14	AH11	
14	IO_L4N_VREF_14	AH10	
14	IO_L5P_14	AF5	
14	IO_L5N_14	AF6	
14	IO_L6P_14	AK9	
14	IO_L6N_14	AL9	

Table 2-9: **FF1759 Package—TX150T and TX240T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
14	IO_L7P_14	AG6	
14	IO_L7N_14	AH5	
14	IO_L8P_CC_14	AF10	
14	IO_L8N_CC_14(2)	AG9	
14	IO_L9P_CC_14	AG7	
14	IO_L9N_CC_14(2)	AH6	
14	IO_L10P_CC_14	AG8	
14	IO_L10N_CC_14(2)	AH8	
14	IO_L11P_CC_14	AK8	
14	IO_L11N_CC_14(2)	AL7	
14	IO_L12P_VRN_14	AJ6	
14	IO_L12N_VRP_14	AJ7	
14	IO_L13P_14	AH9	
14	IO_L13N_14	AJ8	
14	IO_L14P_14	AK7	
14	IO_L14N_VREF_14	AL6	
14	IO_L15P_14	AP5	
14	IO_L15N_14	AP6	
14	IO_L16P_14	AF9	
14	IO_L16N_14	AE9	
14	IO_L17P_14	AD10	
14	IO_L17N_14	AE10	
14	IO_L18P_14	AM5	
14	IO_L18N_14	AN5	
14	IO_L19P_14	AM6	
14	IO_L19N_14	AM7	
23	IO_L0P_23	J33	
23	IO_L0N_23	H34	
23	IO_L1P_23	R37	
23	IO_L1N_23	P37	
23	IO_L2P_23	H35	
23	IO_L2N_23	H36	
23	IO_L3P_23	R38	

Table 2-9: **FF1759 Package—TX150T and TX240T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
23	IO_L3N_23	P38	
23	IO_L4P_23	G37	
23	IO_L4N_VREF_23	H38	
23	IO_L5P_23	R35	
23	IO_L5N_23	P36	
23	IO_L6P_23	K34	
23	IO_L6N_23	K33	
23	IO_L7P_23	P35	
23	IO_L7N_23	N35	
23	IO_L8P_CC_23	J37	
23	IO_L8N_CC_23(2)	J38	
23	IO_L9P_CC_23	R34	
23	IO_L9N_CC_23(2)	T34	
23	IO_L10P_CC_23	N36	
23	IO_L10N_CC_23(2)	M36	
23	IO_L11P_CC_23	P33	
23	IO_L11N_CC_23(2)	N33	
23	IO_L12P_VRN_23	L35	
23	IO_L12N_VRP_23	L36	
23	IO_L13P_23	R33	
23	IO_L13N_23	R32	
23	IO_L14P_23	N34	
23	IO_L14N_VREF_23	M34	
23	IO_L15P_23	J36	
23	IO_L15N_23	J35	
23	IO_L16P_23	M37	
23	IO_L16N_23	L37	
23	IO_L17P_23	K37	
23	IO_L17N_23	K38	
23	IO_L18P_23	T31	
23	IO_L18N_23	T32	
23	IO_L19P_23	L34	
23	IO_L19N_23	K35	

Table 2-9: **FF1759 Package—TX150T and TX240T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
24	IO_L0P_24	V11	
24	IO_L0N_24	U12	
24	IO_L1P_24	G7	
24	IO_L1N_24	G8	
24	IO_L2P_24	V10	
24	IO_L2N_24	U11	
24	IO_L3P_24	E7	
24	IO_L3N_24	E8	
24	IO_L4P_24	L6	
24	IO_L4N_VREF_24	K5	
24	IO_L5P_24	G6	
24	IO_L5N_24	F6	
24	IO_L6P_24	U9	
24	IO_L6N_24	U8	
24	IO_L7P_24	H6	
24	IO_L7N_24	H5	
24	IO_L8P_CC_24	R8	
24	IO_L8N_CC_24(2)	T9	
24	IO_L9P_CC_24	J8	
24	IO_L9N_CC_24(2)	H8	
24	IO_L10P_CC_24	P10	
24	IO_L10N_CC_24(2)	R10	
24	IO_L11P_CC_24	R9	
24	IO_L11N_CC_24(2)	P8	
24	IO_L12P_VRN_24	K9	
24	IO_L12N_VRP_24	L9	
24	IO_L13P_24	T11	
24	IO_L13N_24	T10	
24	IO_L14P_24	J6	
24	IO_L14N_VREF_24	J5	
24	IO_L15P_24	M8	
24	IO_L15N_24	N8	
24	IO_L16P_24	N9	

Table 2-9: **FF1759 Package—TX150T and TX240T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
24	IO_L16N_24	M9	
24	IO_L17P_24	M7	
24	IO_L17N_24	M6	
24	IO_L18P_24	J7	
24	IO_L18N_24	K8	
24	IO_L19P_24	K7	
24	IO_L19N_24	L7	
25	IO_L0P_25	AJ33	
25	IO_L0N_25	AK34	
25	IO_L1P_25	AT36	
25	IO_L1N_25	AU37	
25	IO_L2P_25	AV36	
25	IO_L2N_25	AU36	
25	IO_L3P_25	AJ31	
25	IO_L3N_25	AJ32	
25	IO_L4P_25	AR35	
25	IO_L4N_VREF_25	AT35	
25	IO_L5P_25	AT37	
25	IO_L5N_25	AR37	
25	IO_L6P_25	AM34	
25	IO_L6N_25	AN34	
25	IO_L7P_25	AP36	
25	IO_L7N_25	AP35	
25	IO_L8P_CC_25	AN33	
25	IO_L8N_CC_25(2)	AM33	
25	IO_L9P_CC_25	AL34	
25	IO_L9N_CC_25(2)	AK35	
25	IO_L10P_CC_25	AH34	
25	IO_L10N_CC_25(2)	AH33	
25	IO_L11P_CC_25	AP32	
25	IO_L11N_CC_25(2)	AP33	
25	IO_L12P_VRN_25	AH35	
25	IO_L12N_VRP_25	AJ35	

Table 2-9: **FF1759 Package—TX150T and TX240T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
25	IO_L13P_25	AK32	
25	IO_L13N_25	AK33	
25	IO_L14P_25	AP37	
25	IO_L14N_VREF_25	AP38	
25	IO_L15P_25	AN31	
25	IO_L15N_25	AP31	
25	IO_L16P_25	AN36	
25	IO_L16N_25	AN35	
25	IO_L17P_25	AM31	
25	IO_L17N_25	AM32	
25	IO_L18P_25	AL35	
25	IO_L18N_25	AM36	
25	IO_L19P_25	AL31	
25	IO_L19N_25	AL32	
26	IO_L0P_26	AR8	
26	IO_L0N_26	AR9	
26	IO_L1P_26	AR10	
26	IO_L1N_26	AT9	
26	IO_L2P_26	AL10	
26	IO_L2N_26	AK10	
26	IO_L3P_26	AP10	
26	IO_L3N_26	AN11	
26	IO_L4P_26	AJ10	
26	IO_L4N_VREF_26	AJ11	
26	IO_L5P_26	AP11	
26	IO_L5N_26	AP12	
26	IO_L6P_26	AN9	
26	IO_L6N_26	AN10	
26	IO_L7P_26	AM11	
26	IO_L7N_26	AL11	
26	IO_L8P_CC_26	AR7	
26	IO_L8N_CC_26(2)	AT7	
26	IO_L9P_CC_26	AJ12	

Table 2-9: **FF1759 Package—TX150T and TX240T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
26	IO_L9N_CC_26[2]	AK12	
26	IO_L10P_CC_26	AM12	
26	IO_L10N_CC_26[2]	AL12	
26	IO_L11P_CC_26	AU8	
26	IO_L11N_CC_26[2]	AV7	
26	IO_L12P_VRN_26	AU9	
26	IO_L12N_VRP_26	AT10	
26	IO_L13P_26	AU6	
26	IO_L13N_26	AT6	
26	IO_L14P_26	AU11	
26	IO_L14N_VREF_26	AV11	
26	IO_L15P_26	AP8	
26	IO_L15N_26	AN8	
26	IO_L16P_26	AP13	
26	IO_L16N_26	AR12	
26	IO_L17P_26	AM9	
26	IO_L17N_26	AM8	
26	IO_L18P_26	AM13	
26	IO_L18N_26	AN13	
26	IO_L19P_26	AR6	
26	IO_L19N_26	AP7	
27	IO_L0P_27	L30	
27	IO_L0N_27	K30	
27	IO_L1P_27	J32	
27	IO_L1N_27	H33	
27	IO_L2P_27	F35	
27	IO_L2N_27	G36	
27	IO_L3P_27	F34	
27	IO_L3N_27	G34	
27	IO_L4P_27	E36	
27	IO_L4N_VREF_27	E35	
27	IO_L5P_27	G32	
27	IO_L5N_27	F32	

Table 2-9: **FF1759 Package—TX150T and TX240T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
27	IO_L6P_27	E37	
27	IO_L6N_27	F37	
27	IO_L7P_27	H31	
27	IO_L7N_27	J31	
27	IO_L8P_CC_27	L31	
27	IO_L8N_CC_27(2)	K32	
27	IO_L9P_CC_27	K29	
27	IO_L9N_CC_27(2)	L29	
27	IO_L10P_CC_27	J30	
27	IO_L10N_CC_27(2)	H30	
27	IO_L11P_CC_27	M33	
27	IO_L11N_CC_27(2)	L32	
27	IO_L12P_VRN_27	G31	
27	IO_L12N_VRP_27	F31	
27	IO_L13P_27	M31	
27	IO_L13N_27	M32	
27	IO_L14P_27	F30	
27	IO_L14N_VREF_27	E30	
27	IO_L15P_27	N31	
27	IO_L15N_27	N30	
27	IO_L16P_27	E29	
27	IO_L16N_27	F29	
27	IO_L17P_27	P31	
27	IO_L17N_27	P32	
27	IO_L18P_27	G29	
27	IO_L18N_27	H29	
27	IO_L19P_27	P30	
27	IO_L19N_27	R30	
28	IO_L0P_28	F10	
28	IO_L0N_28	F9	
28	IO_L1P_28	J11	
28	IO_L1N_28	H10	
28	IO_L2P_28	G11	

Table 2-9: **FF1759 Package—TX150T and TX240T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
28	IO_L2N_28	F11	
28	IO_L3P_28	G9	
28	IO_L3N_28	H9	
28	IO_L4P_28	E12	
28	IO_L4N_VREF_28	E13	
28	IO_L5P_28	J10	
28	IO_L5N_28	K10	
28	IO_L6P_28	K14	
28	IO_L6N_28	J13	
28	IO_L7P_28	K13	
28	IO_L7N_28	K12	
28	IO_L8P_CC_28	H11	
28	IO_L8N_CC_28(2)	J12	
28	IO_L9P_CC_28	L12	
28	IO_L9N_CC_28(2)	M12	
28	IO_L10P_CC_28	L10	
28	IO_L10N_CC_28(2)	L11	
28	IO_L11P_CC_28	G12	
28	IO_L11N_CC_28(2)	F12	
28	IO_L12P_VRN_28	N13	
28	IO_L12N_VRP_28	M13	
28	IO_L13P_28	H13	
28	IO_L13N_28	G13	
28	IO_L14P_28	M11	
28	IO_L14N_VREF_28	N10	
28	IO_L15P_28	E14	
28	IO_L15N_28	F14	
28	IO_L16P_28	P11	
28	IO_L16N_28	N11	
28	IO_L17P_28	F15	
28	IO_L17N_28	G14	
28	IO_L18P_28	P12	
28	IO_L18N_28	R12	

Table 2-9: **FF1759 Package—TX150T and TX240T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
28	IO_L19P_28	H14	
28	IO_L19N_28	H15	
29	IO_L0P_29	AH30	
29	IO_L0N_29	AH29	
29	IO_L1P_29	AN28	
29	IO_L1N_29	AP28	
29	IO_L2P_29	AH31	
29	IO_L2N_29	AJ30	
29	IO_L3P_29	AT26	
29	IO_L3N_29	AT25	
29	IO_L4P_29	AK29	
29	IO_L4N_VREF_29	AK30	
29	IO_L5P_29	AV26	
29	IO_L5N_29	AV25	
29	IO_L6P_29	AU34	
29	IO_L6N_29	AT34	
29	IO_L7P_29	AU27	
29	IO_L7N_29	AT27	
29	IO_L8P_CC_29	AR34	
29	IO_L8N_CC_29(2)	AR33	
29	IO_L9P_CC_29	AM28	
29	IO_L9N_CC_29(2)	AN29	
29	IO_L10P_CC_29	AR28	
29	IO_L10N_CC_29(2)	AR29	
29	IO_L11P_CC_29	AU32	
29	IO_L11N_CC_29(2)	AU33	
29	IO_L12P_VRN_29	AR30	
29	IO_L12N_VRP_29	AP30	
29	IO_L13P_29	AR32	
29	IO_L13N_29	AT32	
29	IO_L14P_29	AT29	
29	IO_L14N_VREF_29	AU28	
29	IO_L15P_29	AM29	

Table 2-9: **FF1759 Package—TX150T and TX240T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
29	IO_L15N_29	AN30	
29	IO_L16P_29	AU29	
29	IO_L16N_29	AV30	
29	IO_L17P_29	AL29	
29	IO_L17N_29	AL30	
29	IO_L18P_29	AV31	
29	IO_L18N_29	AU31	
29	IO_L19P_29	AT30	
29	IO_L19N_29	AT31	
30	IO_L0P_30	AR19	
30	IO_L0N_30	AR18	
30	IO_L1P_30	AJ15	
30	IO_L1N_30	AH15	
30	IO_L2P_30	AN18	
30	IO_L2N_30	AP18	
30	IO_L3P_30	AH14	
30	IO_L3N_30	AG13	
30	IO_L4P_30	AL16	
30	IO_L4N_VREF_30	AM16	
30	IO_L5P_30	AH13	
30	IO_L5N_30	AJ13	
30	IO_L6P_30	AU18	
30	IO_L6N_30	AU17	
30	IO_L7P_30	AK13	
30	IO_L7N_30	AK14	
30	IO_L8P_CC_30	AT17	
30	IO_L8N_CC_30(2)	AR17	
30	IO_L9P_CC_30	AT12	
30	IO_L9N_CC_30(2)	AR13	
30	IO_L10P_CC_30	AN14	
30	IO_L10N_CC_30(2)	AN15	
30	IO_L11P_CC_30	AN16	
30	IO_L11N_CC_30(2)	AP17	

Table 2-9: **FF1759 Package—TX150T and TX240T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
30	IO_L12P_VRN_30	AU13	
30	IO_L12N_VRP_30	AT14	
30	IO_L13P_30	AT16	
30	IO_L13N_30	AU16	
30	IO_L14P_30	AP15	
30	IO_L14N_VREF_30	AR14	
30	IO_L15P_30	AR15	
30	IO_L15N_30	AP16	
30	IO_L16P_30	AM14	
30	IO_L16N_30	AL14	
30	IO_L17P_30	AU14	
30	IO_L17N_30	AT15	
30	IO_L18P_30	AU12	
30	IO_L18N_30	AV13	
30	IO_L19P_30	AK15	
30	IO_L19N_30	AL15	
NA	MGTTXP0_111	T41	
NA	MGTAVTTTX_111	AA40	
NA	MGTTXN0_111	U41	
NA	MGTAVCC_111	W40	
NA	MGTRXP0_111	U42	
NA	MGTAVTTRX_111	U40	
NA	MGTRXN0_111	V42	
NA	MGTAVCCPLL_111	Y40	
NA	MGTRXN1_111	W42	
NA	MGTREFCLKN_111	V40	
NA	MGTRXP1_111	Y42	
NA	MGTREFCLKP_111	V39	
NA	MGTTXN1_111	Y41	
NA	MGTTXP1_111	AA41	
NA	MGTAVTTRXC_L	AA39	
NA	MGTRREF_111	AB39	
NA	MGTTXP0_112	T2	

Table 2-9: **FF1759 Package—TX150T and TX240T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	MGTAVTTTX_112	AA3	
NA	MGTTXN0_112	U2	
NA	MGTAVCC_112	W3	
NA	MGTRXP0_112	U1	
NA	MGTAVTTRX_112	U3	
NA	MGTRXN0_112	V1	
NA	MGTAVCCPLL_112	Y3	
NA	MGTRXN1_112	W1	
NA	MGTREFCLKN_112	V3	
NA	MGTRXP1_112	Y1	
NA	MGTREFCLKP_112	V4	
NA	MGTTXN1_112	Y2	
NA	MGTTXP1_112	AA2	
NA	MGTAVTTRXC_R	AA4	
NA	MGTRREF_112	AB4	
NA	MGTTXP0_113	AB41	
NA	MGTAVTTTX_113	AG40	
NA	MGTTXN0_113	AC41	
NA	MGTAVCC_113	AE40	
NA	MGTRXP0_113	AC42	
NA	MGTAVTTRX_113	AC40	
NA	MGTRXN0_113	AD42	
NA	MGTAVCCPLL_113	AF40	
NA	MGTRXN1_113	AE42	
NA	MGTREFCLKN_113	AD40	
NA	MGTRXP1_113	AF42	
NA	MGTREFCLKP_113	AD39	
NA	MGTTXN1_113	AF41	
NA	MGTTXP1_113	AG41	
NA	MGTTXP0_114	AB2	
NA	MGTAVTTTX_114	AG3	
NA	MGTTXN0_114	AC2	
NA	MGTAVCC_114	AE3	

Table 2-9: **FF1759 Package—TX150T and TX240T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	MGTRXP0_114	AC1	
NA	MGTAVTTRX_114	AC3	
NA	MGTRXN0_114	AD1	
NA	MGTAVCCPLL_114	AF3	
NA	MGTRXN1_114	AE1	
NA	MGTREFCLKN_114	AD3	
NA	MGTRXP1_114	AF1	
NA	MGTREFCLKP_114	AD4	
NA	MGTTXN1_114	AF2	
NA	MGTTXP1_114	AG2	
NA	MGTTXP0_115	K41	
NA	MGTAVTTTX_115	R40	
NA	MGTTXN0_115	L41	
NA	MGTAVCC_115	N40	
NA	MGTRXP0_115	L42	
NA	MGTAVTTRX_115	L40	
NA	MGTRXN0_115	M42	
NA	MGTAVCCPLL_115	P40	
NA	MGTRXN1_115	N42	
NA	MGTREFCLKN_115	M40	
NA	MGTRXP1_115	P42	
NA	MGTREFCLKP_115	M39	
NA	MGTTXN1_115	P41	
NA	MGTTXP1_115	R41	
NA	MGTTXP0_116	K2	
NA	MGTAVTTTX_116	R3	
NA	MGTTXN0_116	L2	
NA	MGTAVCC_116	N3	
NA	MGTRXP0_116	L1	
NA	MGTAVTTRX_116	L3	
NA	MGTRXN0_116	M1	
NA	MGTAVCCPLL_116	P3	
NA	MGTRXN1_116	N1	

Table 2-9: **FF1759 Package—TX150T and TX240T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	MGTREFCLKN_116	M3	
NA	MGTRXP1_116	P1	
NA	MGTREFCLKP_116	M4	
NA	MGTTXN1_116	P2	
NA	MGTTXP1_116	R2	
NA	MGTTXP0_117	AH41	
NA	MGTAVTTTX_117	AN40	
NA	MGTTXN0_117	AJ41	
NA	MGTAVCC_117	AL40	
NA	MGTRXP0_117	AJ42	
NA	MGTAVTTRX_117	AJ40	
NA	MGTRXN0_117	AK42	
NA	MGTAVCCPLL_117	AM40	
NA	MGTRXN1_117	AL42	
NA	MGTREFCLKN_117	AK40	
NA	MGTRXP1_117	AM42	
NA	MGTREFCLKP_117	AK39	
NA	MGTTXN1_117	AM41	
NA	MGTTXP1_117	AN41	
NA	MGTTXP0_118	AH2	
NA	MGTAVTTTX_118	AN3	
NA	MGTTXN0_118	AJ2	
NA	MGTAVCC_118	AL3	
NA	MGTRXP0_118	AJ1	
NA	MGTAVTTRX_118	AJ3	
NA	MGTRXN0_118	AK1	
NA	MGTAVCCPLL_118	AM3	
NA	MGTRXN1_118	AL1	
NA	MGTREFCLKN_118	AK3	
NA	MGTRXP1_118	AM1	
NA	MGTREFCLKP_118	AK4	
NA	MGTTXN1_118	AM2	
NA	MGTTXP1_118	AN2	

Table 2-9: **FF1759 Package—TX150T and TX240T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	MGTTXP0_119	D41	
NA	MGTAVTTTX_119	J40	
NA	MGTTXN0_119	E41	
NA	MGTAVCC_119	G40	
NA	MGTRXP0_119	E42	
NA	MGTAVTTRX_119	E40	
NA	MGTRXN0_119	F42	
NA	MGTAVCCPLL_119	H40	
NA	MGTRXN1_119	G42	
NA	MGTREFCLKN_119	F40	
NA	MGTRXP1_119	H42	
NA	MGTREFCLKP_119	F39	
NA	MGTTXN1_119	H41	
NA	MGTTXP1_119	J41	
NA	MGTTXP0_120	D2	
NA	MGTAVTTTX_120	J3	
NA	MGTTXN0_120	E2	
NA	MGTAVCC_120	G3	
NA	MGTRXP0_120	E1	
NA	MGTAVTTRX_120	E3	
NA	MGTRXN0_120	F1	
NA	MGTAVCCPLL_120	H3	
NA	MGTRXN1_120	G1	
NA	MGTREFCLKN_120	F3	
NA	MGTRXP1_120	H1	
NA	MGTREFCLKP_120	F4	
NA	MGTTXN1_120	H2	
NA	MGTTXP1_120	J2	
NA	MGTTXP0_121	AP41	
NA	MGTAVTTTX_121	AW40	
NA	MGTTXN0_121	AR41	
NA	MGTAVCC_121	AU40	
NA	MGTRXP0_121	AR42	

Table 2-9: **FF1759 Package—TX150T and TX240T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	MGTAVTTRX_121	AR40	
NA	MGTRXN0_121	AT42	
NA	MGTAVCCPLL_121	AV40	
NA	MGTRXN1_121	AU42	
NA	MGTREFCLKN_121	AT40	
NA	MGTRXP1_121	AV42	
NA	MGTREFCLKP_121	AT39	
NA	MGTTXN1_121	AV41	
NA	MGTTXP1_121	AW41	
NA	MGTTXP0_122	AP2	
NA	MGTAVTTTX_122	AW3	
NA	MGTTXN0_122	AR2	
NA	MGTAVCC_122	AU3	
NA	MGTRXP0_122	AR1	
NA	MGTAVTTRX_122	AR3	
NA	MGTRXN0_122	AT1	
NA	MGTAVCCPLL_122	AV3	
NA	MGTRXN1_122	AU1	
NA	MGTREFCLKN_122	AT3	
NA	MGTRXP1_122	AV1	
NA	MGTREFCLKP_122	AT4	
NA	MGTTXN1_122	AV2	
NA	MGTTXP1_122	AW2	
NA	MGTTXP0_123	B37	
NA	MGTAVTTTX_123	C42	
NA	MGTTXN0_123	B38	
NA	MGTAVCC_123	D39	
NA	MGTRXP0_123	A38	
NA	MGTAVTTRX_123	C38	
NA	MGTRXN0_123	A39	
NA	MGTAVCCPLL_123	C41	
NA	MGTRXN1_123	A40	
NA	MGTREFCLKN_123	C40	

Table 2-9: **FF1759 Package—TX150T and TX240T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	MGTRXP1_123	A41	
NA	MGTREFCLKP_123	C39	
NA	MGTTXN1_123	B41	
NA	MGTTXP1_123	B42	
NA	MGTTXP0_124	B6	
NA	MGTAVTTTX_124	C1	
NA	MGTTXN0_124	B5	
NA	MGTAVCC_124	D4	
NA	MGTRXP0_124	A5	
NA	MGTAVTTRX_124	C5	
NA	MGTRXN0_124	A4	
NA	MGTAVCCPLL_124	C2	
NA	MGTRXN1_124	A3	
NA	MGTREFCLKN_124	C3	
NA	MGTRXP1_124	A2	
NA	MGTREFCLKP_124	C4	
NA	MGTTXN1_124	B2	
NA	MGTTXP1_124	B1	
NA	MGTTXP0_125	BA42	
NA	MGTAVTTTX_125	AY37	
NA	MGTTXN0_125	BA41	
NA	MGTAVCC_125	AW38	
NA	MGTRXP0_125	BB41	
NA	MGTAVTTRX_125	AY41	
NA	MGTRXN0_125	BB40	
NA	MGTAVCCPLL_125	AY38	
NA	MGTRXN1_125	BB39	
NA	MGTREFCLKN_125	AY39	
NA	MGTRXP1_125	BB38	
NA	MGTREFCLKP_125	AW39	
NA	MGTTXN1_125	BA38	
NA	MGTTXP1_125	BA37	
NA	MGTTXP0_126	BA1	

Table 2-9: **FF1759 Package—TX150T and TX240T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	MGTAVTTTX_126	AY6	
NA	MGTTXN0_126	BA2	
NA	MGTAVCC_126	AW5	
NA	MGTRXP0_126	BB2	
NA	MGTAVTTRX_126	AY2	
NA	MGTRXN0_126	BB3	
NA	MGTAVCCPLL_126	AY5	
NA	MGTRXN1_126	BB4	
NA	MGTREFCLKN_126	AY4	
NA	MGTRXP1_126	BB5	
NA	MGTREFCLKP_126	AW4	
NA	MGTTXN1_126	BA5	
NA	MGTTXP1_126	BA6	
NA	MGTTXP0_127	B31	
NA	MGTAVTTTX_127	C36	
NA	MGTTXN0_127	B32	
NA	MGTAVCC_127	C34	
NA	MGTRXP0_127	A32	
NA	MGTAVTTRX_127	C32	
NA	MGTRXN0_127	A33	
NA	MGTAVCCPLL_127	C35	
NA	MGTRXN1_127	A34	
NA	MGTREFCLKN_127	C33	
NA	MGTRXP1_127	A35	
NA	MGTREFCLKP_127	D33	
NA	MGTTXN1_127	B35	
NA	MGTTXP1_127	B36	
NA	MGTTXP0_128	B12	
NA	MGTAVTTTX_128	C7	
NA	MGTTXN0_128	B11	
NA	MGTAVCC_128	C9	
NA	MGTRXP0_128	A11	
NA	MGTAVTTRX_128	C11	

Table 2-9: **FF1759 Package—TX150T and TX240T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	MGTRXN0_128	A10	
NA	MGTAVCCPLL_128	C8	
NA	MGTRXN1_128	A9	
NA	MGTREFCLKN_128	C10	
NA	MGTRXP1_128	A8	
NA	MGTREFCLKP_128	D10	
NA	MGTTXN1_128	B8	
NA	MGTTXP1_128	B7	
NA	MGTTXP0_129	BA36	
NA	MGTAVTTTX_129	AY31	
NA	MGTTXN0_129	BA35	
NA	MGTAVCC_129	AY33	
NA	MGTRXP0_129	BB35	
NA	MGTAVTTRX_129	AY35	
NA	MGTRXN0_129	BB34	
NA	MGTAVCCPLL_129	AY32	
NA	MGTRXN1_129	BB33	
NA	MGTREFCLKN_129	AY34	
NA	MGTRXP1_129	BB32	
NA	MGTREFCLKP_129	AW34	
NA	MGTTXN1_129	BA32	
NA	MGTTXP1_129	BA31	
NA	MGTTXP0_130	BA7	
NA	MGTAVTTTX_130	AY12	
NA	MGTTXN0_130	BA8	
NA	MGTAVCC_130	AY10	
NA	MGTRXP0_130	BB8	
NA	MGTAVTTRX_130	AY8	
NA	MGTRXN0_130	BB9	
NA	MGTAVCCPLL_130	AY11	
NA	MGTRXN1_130	BB10	
NA	MGTREFCLKN_130	AY9	
NA	MGTRXP1_130	BB11	

Table 2-9: **FF1759 Package—TX150T and TX240T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	MGTREFCLKP_130	AW9	
NA	MGTTXN1_130	BA11	
NA	MGTTXP1_130	BA12	
NA	MGTTXP0_131	B25	TX150T
NA	MGTAVTTTX_131	C30	TX150T
NA	MGTTXN0_131	B26	TX150T
NA	MGTAVCC_131	C28	TX150T
NA	MGTRXP0_131	A26	TX150T
NA	MGTAVTTRX_131	C26	TX150T
NA	MGTRXN0_131	A27	TX150T
NA	MGTAVCCPLL_131	C29	TX150T
NA	MGTRXN1_131	A28	TX150T
NA	MGTREFCLKN_131	C27	TX150T
NA	MGTRXP1_131	A29	TX150T
NA	MGTREFCLKP_131	D27	TX150T
NA	MGTTXN1_131	B29	TX150T
NA	MGTTXP1_131	B30	TX150T
NA	MGTTXP0_132	B18	TX150T
NA	MGTAVTTTX_132	C13	TX150T
NA	MGTTXN0_132	B17	TX150T
NA	MGTAVCC_132	C15	TX150T
NA	MGTRXP0_132	A17	TX150T
NA	MGTAVTTRX_132	C17	TX150T
NA	MGTRXN0_132	A16	TX150T
NA	MGTAVCCPLL_132	C14	TX150T
NA	MGTRXN1_132	A15	TX150T
NA	MGTREFCLKN_132	C16	TX150T
NA	MGTRXP1_132	A14	TX150T
NA	MGTREFCLKP_132	D16	TX150T
NA	MGTTXN1_132	B14	TX150T
NA	MGTTXP1_132	B13	TX150T
NA	MGTTXP0_133	BA30	TX150T
NA	MGTAVTTTX_133	AY25	TX150T

Table 2-9: **FF1759 Package—TX150T and TX240T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	MGTTXN0_133	BA29	TX150T
NA	MGTAVCC_133	AY27	TX150T
NA	MGTRXP0_133	BB29	TX150T
NA	MGTAVTTRX_133	AY29	TX150T
NA	MGTRXN0_133	BB28	TX150T
NA	MGTAVCCPLL_133	AY26	TX150T
NA	MGTRXN1_133	BB27	TX150T
NA	MGTREFCLKN_133	AY28	TX150T
NA	MGTRXP1_133	BB26	TX150T
NA	MGTREFCLKP_133	AW28	TX150T
NA	MGTTXN1_133	BA26	TX150T
NA	MGTTXP1_133	BA25	TX150T
NA	MGTTXP0_134	BA13	TX150T
NA	MGTAVTTTX_134	AY18	TX150T
NA	MGTTXN0_134	BA14	TX150T
NA	MGTAVCC_134	AY16	TX150T
NA	MGTRXP0_134	BB14	TX150T
NA	MGTAVTTRX_134	AY14	TX150T
NA	MGTRXN0_134	BB15	TX150T
NA	MGTAVCCPLL_134	AY17	TX150T
NA	MGTRXN1_134	BB16	TX150T
NA	MGTREFCLKN_134	AY15	TX150T
NA	MGTRXP1_134	BB17	TX150T
NA	MGTREFCLKP_134	AW15	TX150T
NA	MGTTXN1_134	BA17	TX150T
NA	MGTTXP1_134	BA18	TX150T
NA	GND	A6	
NA	GND	A7	
NA	GND	A12	
NA	GND	A13	
NA	GND	A18	
NA	GND	A19	
NA	GND	A23	

Table 2-9: **FF1759 Package—TX150T and TX240T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	A24	
NA	GND	A25	
NA	GND	A30	
NA	GND	A31	
NA	GND	A36	
NA	GND	A37	
NA	GND	AA1	
NA	GND	AA5	
NA	GND	AA13	
NA	GND	AA15	
NA	GND	AA17	
NA	GND	AA19	
NA	GND	AA23	
NA	GND	AA25	
NA	GND	AA27	
NA	GND	AA29	
NA	GND	AA33	
NA	GND	AA38	
NA	GND	AA42	
NA	GND	AB1	
NA	GND	AB3	
NA	GND	AB5	
NA	GND	AB10	
NA	GND	AB12	
NA	GND	AB14	
NA	GND	AB16	
NA	GND	AB18	
NA	GND	AB20	
NA	GND	AB24	
NA	GND	AB26	
NA	GND	AB28	
NA	GND	AB30	
NA	GND	AB38	

Table 2-9: **FF1759 Package—TX150T and TX240T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	AB40	
NA	GND	AB42	
NA	GND	AC4	
NA	GND	AC5	
NA	GND	AC7	
NA	GND	AC13	
NA	GND	AC15	
NA	GND	AC17	
NA	GND	AC19	
NA	GND	AC23	
NA	GND	AC25	
NA	GND	AC27	
NA	GND	AC29	
NA	GND	AC37	
NA	GND	AC38	
NA	GND	AC39	
NA	GND	AD2	
NA	GND	AD5	
NA	GND	AD12	
NA	GND	AD14	
NA	GND	AD16	
NA	GND	AD18	
NA	GND	AD20	
NA	GND	AD22	
NA	GND	AD24	
NA	GND	AD26	
NA	GND	AD28	
NA	GND	AD34	
NA	GND	AD38	
NA	GND	AD41	
NA	GND	AE2	
NA	GND	AE4	
NA	GND	AE5	

Table 2-9: **FF1759 Package—TX150T and TX240T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	AE6	
NA	GND	AE11	
NA	GND	AE13	
NA	GND	AE15	
NA	GND	AE17	
NA	GND	AE19	
NA	GND	AE21	
NA	GND	AE23	
NA	GND	AE25	
NA	GND	AE27	
NA	GND	AE29	
NA	GND	AE31	
NA	GND	AE38	
NA	GND	AE39	
NA	GND	AE41	
NA	GND	AF4	
NA	GND	AF8	
NA	GND	AF18	
NA	GND	AF20	
NA	GND	AF22	
NA	GND	AF24	
NA	GND	AF26	
NA	GND	AF28	
NA	GND	AF30	
NA	GND	AF38	
NA	GND	AF39	
NA	GND	AG1	
NA	GND	AG4	
NA	GND	AG5	
NA	GND	AG15	
NA	GND	AG17	
NA	GND	AG19	
NA	GND	AG21	

Table 2-9: **FF1759 Package—TX150T and TX240T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	AG23	
NA	GND	AG25	
NA	GND	AG27	
NA	GND	AG35	
NA	GND	AG39	
NA	GND	AG42	
NA	GND	AH1	
NA	GND	AH3	
NA	GND	AH4	
NA	GND	AH12	
NA	GND	AH18	
NA	GND	AH20	
NA	GND	AH22	
NA	GND	AH24	
NA	GND	AH26	
NA	GND	AH32	
NA	GND	AH39	
NA	GND	AH40	
NA	GND	AH42	
NA	GND	AJ4	
NA	GND	AJ5	
NA	GND	AJ9	
NA	GND	AJ19	
NA	GND	AJ21	
NA	GND	AJ23	
NA	GND	AJ29	
NA	GND	AJ38	
NA	GND	AJ39	
NA	GND	AK2	
NA	GND	AK5	
NA	GND	AK6	
NA	GND	AK16	
NA	GND	AK26	

Table 2-9: **FF1759 Package—TX150T and TX240T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	AK36	
NA	GND	AK38	
NA	GND	AK41	
NA	GND	AL2	
NA	GND	AL4	
NA	GND	AL5	
NA	GND	AL13	
NA	GND	AL23	
NA	GND	AL33	
NA	GND	AL38	
NA	GND	AL39	
NA	GND	AL41	
NA	GND	AM4	
NA	GND	AM10	
NA	GND	AM20	
NA	GND	AM30	
NA	GND	AM39	
NA	GND	AN1	
NA	GND	AN4	
NA	GND	AN7	
NA	GND	AN17	
NA	GND	AN27	
NA	GND	AN37	
NA	GND	AN39	
NA	GND	AN42	
NA	GND	AP1	
NA	GND	AP3	
NA	GND	AP4	
NA	GND	AP14	
NA	GND	AP24	
NA	GND	AP34	
NA	GND	AP39	
NA	GND	AP40	

Table 2-9: **FF1759 Package—TX150T and TX240T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	AP42	
NA	GND	AR4	
NA	GND	AR5	
NA	GND	AR11	
NA	GND	AR21	
NA	GND	AR31	
NA	GND	AR38	
NA	GND	AR39	
NA	GND	AT2	
NA	GND	AT5	
NA	GND	AT8	
NA	GND	AT18	
NA	GND	AT28	
NA	GND	AT38	
NA	GND	AT41	
NA	GND	AU2	
NA	GND	AU4	
NA	GND	AU5	
NA	GND	AU10	
NA	GND	AU15	
NA	GND	AU25	
NA	GND	AU35	
NA	GND	AU38	
NA	GND	AU39	
NA	GND	AU41	
NA	GND	AV4	
NA	GND	AV5	
NA	GND	AV6	
NA	GND	AV8	
NA	GND	AV9	
NA	GND	AV10	
NA	GND	AV12	
NA	GND	AV14	

Table 2-9: **FF1759 Package—TX150T and TX240T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	AV15	
NA	GND	AV16	
NA	GND	AV17	
NA	GND	AV22	
NA	GND	AV27	
NA	GND	AV28	
NA	GND	AV29	
NA	GND	AV32	
NA	GND	AV33	
NA	GND	AV34	
NA	GND	AV35	
NA	GND	AV37	
NA	GND	AV38	
NA	GND	AV39	
NA	GND	AW1	
NA	GND	AW6	
NA	GND	AW7	
NA	GND	AW8	
NA	GND	AW10	
NA	GND	AW11	
NA	GND	AW12	
NA	GND	AW13	
NA	GND	AW14	
NA	GND	AW16	
NA	GND	AW17	
NA	GND	AW18	
NA	GND	AW19	
NA	GND	AW24	
NA	GND	AW25	
NA	GND	AW26	
NA	GND	AW27	
NA	GND	AW29	
NA	GND	AW30	

Table 2-9: **FF1759 Package—TX150T and TX240T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	AW31	
NA	GND	AW32	
NA	GND	AW33	
NA	GND	AW35	
NA	GND	AW36	
NA	GND	AW37	
NA	GND	AW42	
NA	GND	AY1	
NA	GND	AY3	
NA	GND	AY7	
NA	GND	AY13	
NA	GND	AY19	
NA	GND	AY24	
NA	GND	AY30	
NA	GND	AY36	
NA	GND	AY40	
NA	GND	AY42	
NA	GND	B3	
NA	GND	B4	
NA	GND	B9	
NA	GND	B10	
NA	GND	B15	
NA	GND	B16	
NA	GND	B19	
NA	GND	B20	
NA	GND	B24	
NA	GND	B27	
NA	GND	B28	
NA	GND	B33	
NA	GND	B34	
NA	GND	B39	
NA	GND	B40	
NA	GND	BA3	

Table 2-9: **FF1759 Package—TX150T and TX240T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	BA4	
NA	GND	BA9	
NA	GND	BA10	
NA	GND	BA15	
NA	GND	BA16	
NA	GND	BA19	
NA	GND	BA23	
NA	GND	BA24	
NA	GND	BA27	
NA	GND	BA28	
NA	GND	BA33	
NA	GND	BA34	
NA	GND	BA39	
NA	GND	BA40	
NA	GND	BB6	
NA	GND	BB7	
NA	GND	BB12	
NA	GND	BB13	
NA	GND	BB18	
NA	GND	BB19	
NA	GND	BB20	
NA	GND	BB24	
NA	GND	BB25	
NA	GND	BB30	
NA	GND	BB31	
NA	GND	BB36	
NA	GND	BB37	
NA	GND	C6	
NA	GND	C12	
NA	GND	C18	
NA	GND	C19	
NA	GND	C24	
NA	GND	C25	

Table 2-9: **FF1759 Package—TX150T and TX240T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	C31	
NA	GND	C37	
NA	GND	D1	
NA	GND	D3	
NA	GND	D5	
NA	GND	D6	
NA	GND	D7	
NA	GND	D8	
NA	GND	D9	
NA	GND	D11	
NA	GND	D12	
NA	GND	D13	
NA	GND	D14	
NA	GND	D15	
NA	GND	D17	
NA	GND	D18	
NA	GND	D19	
NA	GND	D24	
NA	GND	D25	
NA	GND	D26	
NA	GND	D28	
NA	GND	D29	
NA	GND	D30	
NA	GND	D31	
NA	GND	D32	
NA	GND	D34	
NA	GND	D35	
NA	GND	D36	
NA	GND	D37	
NA	GND	D38	
NA	GND	D40	
NA	GND	D42	
NA	GND	E4	

Table 2-9: **FF1759 Package—TX150T and TX240T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	E5	
NA	GND	E6	
NA	GND	E9	
NA	GND	E10	
NA	GND	E11	
NA	GND	E15	
NA	GND	E16	
NA	GND	E17	
NA	GND	E21	
NA	GND	E26	
NA	GND	E27	
NA	GND	E28	
NA	GND	E31	
NA	GND	E32	
NA	GND	E33	
NA	GND	E34	
NA	GND	E38	
NA	GND	E39	
NA	GND	F2	
NA	GND	F5	
NA	GND	F8	
NA	GND	F18	
NA	GND	F28	
NA	GND	F33	
NA	GND	F38	
NA	GND	F41	
NA	GND	G2	
NA	GND	G4	
NA	GND	G5	
NA	GND	G15	
NA	GND	G25	
NA	GND	G35	
NA	GND	G38	

Table 2-9: **FF1759 Package—TX150T and TX240T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	G39	
NA	GND	G41	
NA	GND	H4	
NA	GND	H12	
NA	GND	H22	
NA	GND	H32	
NA	GND	H39	
NA	GND	J1	
NA	GND	J4	
NA	GND	J9	
NA	GND	J19	
NA	GND	J29	
NA	GND	J39	
NA	GND	J42	
NA	GND	K1	
NA	GND	K3	
NA	GND	K4	
NA	GND	K6	
NA	GND	K16	
NA	GND	K26	
NA	GND	K36	
NA	GND	K39	
NA	GND	K40	
NA	GND	K42	
NA	GND	L4	
NA	GND	L5	
NA	GND	L13	
NA	GND	L23	
NA	GND	L33	
NA	GND	L38	
NA	GND	L39	
NA	GND	M2	
NA	GND	M5	

Table 2-9: **FF1759 Package—TX150T and TX240T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	M10	
NA	GND	M20	
NA	GND	M30	
NA	GND	M38	
NA	GND	M41	
NA	GND	N2	
NA	GND	N4	
NA	GND	N5	
NA	GND	N7	
NA	GND	N17	
NA	GND	N27	
NA	GND	N37	
NA	GND	N38	
NA	GND	N39	
NA	GND	N41	
NA	GND	P4	
NA	GND	P14	
NA	GND	P16	
NA	GND	P20	
NA	GND	P24	
NA	GND	P34	
NA	GND	P39	
NA	GND	R1	
NA	GND	R4	
NA	GND	R11	
NA	GND	R13	
NA	GND	R17	
NA	GND	R19	
NA	GND	R21	
NA	GND	R23	
NA	GND	R25	
NA	GND	R31	
NA	GND	R39	

Table 2-9: **FF1759 Package—TX150T and TX240T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	R42	
NA	GND	T1	
NA	GND	T3	
NA	GND	T4	
NA	GND	T8	
NA	GND	T12	
NA	GND	T16	
NA	GND	T18	
NA	GND	T20	
NA	GND	T22	
NA	GND	T24	
NA	GND	T26	
NA	GND	T28	
NA	GND	T38	
NA	GND	T39	
NA	GND	T40	
NA	GND	T42	
NA	GND	U4	
NA	GND	U5	
NA	GND	U13	
NA	GND	U15	
NA	GND	U17	
NA	GND	U19	
NA	GND	U21	
NA	GND	U23	
NA	GND	U25	
NA	GND	U27	
NA	GND	U35	
NA	GND	U38	
NA	GND	U39	
NA	GND	V2	
NA	GND	V5	
NA	GND	V12	

Table 2-9: **FF1759 Package—TX150T and TX240T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	V14	
NA	GND	V16	
NA	GND	V18	
NA	GND	V20	
NA	GND	V22	
NA	GND	V24	
NA	GND	V26	
NA	GND	V28	
NA	GND	V30	
NA	GND	V32	
NA	GND	V37	
NA	GND	V38	
NA	GND	V41	
NA	GND	W2	
NA	GND	W4	
NA	GND	W5	
NA	GND	W9	
NA	GND	W13	
NA	GND	W15	
NA	GND	W17	
NA	GND	W19	
NA	GND	W21	
NA	GND	W23	
NA	GND	W25	
NA	GND	W27	
NA	GND	W29	
NA	GND	W38	
NA	GND	W39	
NA	GND	W41	
NA	GND	Y4	
NA	GND	Y5	
NA	GND	Y6	
NA	GND	Y12	

Table 2-9: **FF1759 Package—TX150T and TX240T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	Y14	
NA	GND	Y16	
NA	GND	Y18	
NA	GND	Y20	
NA	GND	Y24	
NA	GND	Y26	
NA	GND	Y28	
NA	GND	Y36	
NA	GND	Y38	
NA	GND	Y39	
NA	VCCAUX	AA12	
NA	VCCAUX	AA28	
NA	VCCAUX	AB29	
NA	VCCAUX	AC12	
NA	VCCAUX	AD13	
NA	VCCAUX	AD29	
NA	VCCAUX	AE12	
NA	VCCAUX	AE30	
NA	VCCAUX	AF13	
NA	VCCAUX	AG28	
NA	VCCAUX	AG30	
NA	VCCAUX	T13	
NA	VCCAUX	U28	
NA	VCCAUX	V13	
NA	VCCAUX	V29	
NA	VCCAUX	W12	
NA	VCCAUX	W28	
NA	VCCAUX	Y13	
NA	VCCINT	AA14	
NA	VCCINT	AA16	
NA	VCCINT	AA18	
NA	VCCINT	AA20	
NA	VCCINT	AA24	

Table 2-9: **FF1759 Package—TX150T and TX240T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	VCCINT	AA26	
NA	VCCINT	AB13	
NA	VCCINT	AB15	
NA	VCCINT	AB17	
NA	VCCINT	AB19	
NA	VCCINT	AB23	
NA	VCCINT	AB25	
NA	VCCINT	AB27	
NA	VCCINT	AC14	
NA	VCCINT	AC16	
NA	VCCINT	AC18	
NA	VCCINT	AC20	
NA	VCCINT	AC24	
NA	VCCINT	AC26	
NA	VCCINT	AC28	
NA	VCCINT	AD15	
NA	VCCINT	AD17	
NA	VCCINT	AD19	
NA	VCCINT	AD21	
NA	VCCINT	AD23	
NA	VCCINT	AD25	
NA	VCCINT	AD27	
NA	VCCINT	AE14	
NA	VCCINT	AE16	
NA	VCCINT	AE18	
NA	VCCINT	AE20	
NA	VCCINT	AE22	
NA	VCCINT	AE24	
NA	VCCINT	AE26	
NA	VCCINT	AE28	
NA	VCCINT	AF17	
NA	VCCINT	AF19	
NA	VCCINT	AF21	

Table 2-9: **FF1759 Package—TX150T and TX240T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	VCCINT	AF23	
NA	VCCINT	AF25	
NA	VCCINT	AF27	
NA	VCCINT	AG18	
NA	VCCINT	AG20	
NA	VCCINT	AG22	
NA	VCCINT	AG24	
NA	VCCINT	AG26	
NA	VCCINT	AH19	
NA	VCCINT	AH21	
NA	VCCINT	AH23	
NA	VCCINT	AH25	
NA	VCCINT	AH27	
NA	VCCINT	AJ20	
NA	VCCINT	AJ22	
NA	VCCINT	AJ26	
NA	VCCINT	N20	
NA	VCCINT	P23	
NA	VCCINT	R18	
NA	VCCINT	R20	
NA	VCCINT	R22	
NA	VCCINT	R24	
NA	VCCINT	T15	
NA	VCCINT	T17	
NA	VCCINT	T19	
NA	VCCINT	T21	
NA	VCCINT	T23	
NA	VCCINT	T25	
NA	VCCINT	T27	
NA	VCCINT	U14	
NA	VCCINT	U16	
NA	VCCINT	U18	
NA	VCCINT	U20	

Table 2-9: **FF1759 Package—TX150T and TX240T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	VCCINT	U22	
NA	VCCINT	U24	
NA	VCCINT	U26	
NA	VCCINT	V15	
NA	VCCINT	V17	
NA	VCCINT	V19	
NA	VCCINT	V21	
NA	VCCINT	V23	
NA	VCCINT	V25	
NA	VCCINT	V27	
NA	VCCINT	W14	
NA	VCCINT	W16	
NA	VCCINT	W18	
NA	VCCINT	W20	
NA	VCCINT	W22	
NA	VCCINT	W24	
NA	VCCINT	W26	
NA	VCCINT	Y15	
NA	VCCINT	Y17	
NA	VCCINT	Y19	
NA	VCCINT	Y23	
NA	VCCINT	Y25	
NA	VCCINT	Y27	
0	VCCO_0	P13	
0	VCCO_0	R16	
1	VCCO_1	M15	
1	VCCO_1	P19	
1	VCCO_1	P29	
1	VCCO_1	R26	
2	VCCO_2	AH17	
2	VCCO_2	AL18	
2	VCCO_2	AL28	
2	VCCO_2	AR26	

Table 2-9: **FF1759 Package—TX150T and TX240T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
3	VCCO_3	J14	
3	VCCO_3	L18	
3	VCCO_3	L28	
3	VCCO_3	M25	
4	VCCO_4	AJ24	
4	VCCO_4	AK21	
4	VCCO_4	AM25	
4	VCCO_4	AP19	
5	VCCO_5	G20	
5	VCCO_5	H17	
5	VCCO_5	H27	
5	VCCO_5	J24	
6	VCCO_6	AN22	
6	VCCO_6	AT23	
6	VCCO_6	AU20	
6	VCCO_6	AY21	
7	VCCO_7	C22	
7	VCCO_7	F23	
7	VCCO_7	K21	
7	VCCO_7	N22	
11	VCCO_11	AB35	
11	VCCO_11	U30	
11	VCCO_11	U36	
11	VCCO_11	W34	
11	VCCO_11	Y31	
12	VCCO_12	AA8	
12	VCCO_12	AD9	
12	VCCO_12	R6	
12	VCCO_12	V7	
12	VCCO_12	Y11	
13	VCCO_13	AC32	
13	VCCO_13	AE36	
13	VCCO_13	AF33	

Table 2-9: **FF1759 Package—TX150T and TX240T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
13	VCCO_13	AH37	
13	VCCO_13	AM37	
14	VCCO_14	AE7	
14	VCCO_14	AG10	
14	VCCO_14	AH7	
14	VCCO_14	AL8	
14	VCCO_14	AN6	
23	VCCO_23	H37	
23	VCCO_23	J34	
23	VCCO_23	M35	
23	VCCO_23	R36	
23	VCCO_23	T33	
24	VCCO_24	F7	
24	VCCO_24	H7	
24	VCCO_24	L8	
24	VCCO_24	P9	
24	VCCO_24	U10	
25	VCCO_25	AJ34	
25	VCCO_25	AM35	
25	VCCO_25	AN32	
25	VCCO_25	AR36	
26	VCCO_26	AK11	
26	VCCO_26	AN12	
26	VCCO_26	AP9	
26	VCCO_26	AT11	
26	VCCO_26	AU7	
27	VCCO_27	F36	
27	VCCO_27	G30	
27	VCCO_27	G33	
27	VCCO_27	K31	
27	VCCO_27	N32	
28	VCCO_28	F13	
28	VCCO_28	G10	

Table 2-9: **FF1759 Package—TX150T and TX240T *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
28	VCCO_28	K11	
28	VCCO_28	N12	
29	VCCO_29	AK31	
29	VCCO_29	AP29	
29	VCCO_29	AT33	
29	VCCO_29	AU26	
29	VCCO_29	AU30	
30	VCCO_30	AJ14	
30	VCCO_30	AM15	
30	VCCO_30	AR16	
30	VCCO_30	AT13	
NA	RSVD(3)	AF14	
NA	RSVD(3)	AG14	

Notes:

1. Do not connect a single-ended clock to the N-side of the differential clock pair of pins, for example, IO_L3N_GC_3.
2. Do not connect a single-ended clock to the N-side of clock capable pins, for example, IO_L8N_CC_11.
3. RSVD pins must be tied to GND (logic 0).

FF1760 Package—LX110, LX155, LX220, and LX330

Table 2-10: **FF1760 Package—LX110, LX155, LX220, and LX330**

Bank	Pin Description	Pin Number	No Connect (NC)
0	DXP_0	AC22	
0	DXN_0	AC21	
0	AVDD_0	Y22	
0	AVSS_0	Y21	
0	VP_0	AA22	
0	VN_0	AB21	
0	VREFP_0	AB22	
0	VREFN_0	AA21	
0	VBATT_0	R29	
0	PROGRAM_B_0	T29	
0	HSWAPEN_0	T14	
0	D_IN_0	R14	
0	DONE_0	T15	
0	CCLK_0	AF15	
0	INIT_B_0	U14	
0	CS_B_0	T30	
0	RDWR_B_0	R30	
0	RSVD(3)	V31	
0	RSVD(3)	AD31	
0	TCK_0	AE30	
0	M0_0	AG29	
0	M2_0	AH28	
0	M1_0	AF30	
0	TMS_0	AF14	
0	TDI_0	AG14	
0	D_OUT_BUSY_0	AH15	
0	TDO_0	AH14	
1	IO_L0P_A19_1	R28	
1	IO_L0N_A18_1	R27	
1	IO_L1P_A17_1	M13	
1	IO_L1N_A16_1	N13	

Table 2-10: **FF1760 Package—LX110, LX155, LX220, and LX330 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
1	IO_L2P_A15_D31_1	P27	
1	IO_L2N_A14_D30_1	P26	
1	IO_L3P_A13_D29_1	P17	
1	IO_L3N_A12_D28_1	R17	
1	IO_L4P_A11_D27_1	N28	
1	IO_L4N_VREF_A10_D26_1	P28	
1	IO_L5P_A9_D25_1	N15	
1	IO_L5N_A8_D24_1	P15	
1	IO_L6P_A7_D23_1	N29	
1	IO_L6N_A6_D22_1	M29	
1	IO_L7P_A5_D21_1	N14	
1	IO_L7N_A4_D20_1	P13	
1	IO_L8P_CC_A3_D19_1	P30	
1	IO_L8N_CC_A2_D18_1 (2)	N30	
1	IO_L9P_CC_A1_D17_1	P16	
1	IO_L9N_CC_A0_D16_1 (2)	R15	
2	IO_L0P_CC_RS1_2	AH16	
2	IO_L0N_CC_RS0_2 (2)	AJ15	
2	IO_L1P_CC_A25_2	AH30	
2	IO_L1N_CC_A24_2 (2)	AH29	
2	IO_L2P_A23_2	AJ16	
2	IO_L2N_A22_2	AJ17	
2	IO_L3P_A21_2	AK30	
2	IO_L3N_A20_2	AJ30	
2	IO_L4P_FCS_B_2	AK14	
2	IO_L4N_VREF_FOE_B_MOSI_2	AK15	
2	IO_L5P_FWE_B_2	AL29	
2	IO_L5N_CSO_B_2	AL30	
2	IO_L6P_D7_2	AJ13	
2	IO_L6N_D6_2	AK13	
2	IO_L7P_D5_2	AJ28	
2	IO_L7N_D4_2	AK29	
2	IO_L8P_D3_2	AL15	

Table 2-10: **FF1760 Package—LX110, LX155, LX220, and LX330 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
2	IO_L8N_D2_FS2_2	AL14	
2	IO_L9P_D1_FS1_2	AJ26	
2	IO_L9N_D0_FS0_2	AJ27	
3	IO_L0P_CC_GC_3	K15	
3	IO_L0N_CC_GC_3 (1)(2)	K14	
3	IO_L1P_CC_GC_3	M27	
3	IO_L1N_CC_GC_3 (1)(2)	N26	
3	IO_L2P_GC_VRN_3	K13	
3	IO_L2N_GC_VRP_3 (1)	J13	
3	IO_L3P_GC_3	L27	
3	IO_L3N_GC_3 (1)	M28	
3	IO_L4P_GC_3	L15	
3	IO_L4N_GC_VREF_3 (1)	L16	
3	IO_L5P_GC_3	K28	
3	IO_L5N_GC_3 (1)	K29	
3	IO_L6P_GC_3	M14	
3	IO_L6N_GC_3 (1)	L14	
3	IO_L7P_GC_3	J30	
3	IO_L7N_GC_3 (1)	K30	
3	IO_L8P_GC_3	N16	
3	IO_L8N_GC_3 (1)	M16	
3	IO_L9P_GC_3	L29	
3	IO_L9N_GC_3 (1)	L30	
4	IO_L0P_GC_D15_4	AK28	
4	IO_L0N_GC_D14_4 (1)	AK27	
4	IO_L1P_GC_D13_4	AL16	
4	IO_L1N_GC_D12_4 (1)	AK17	
4	IO_L2P_GC_D11_4	AM29	
4	IO_L2N_GC_D10_4 (1)	AN30	
4	IO_L3P_GC_D9_4	AN16	
4	IO_L3N_GC_D8_4 (1)	AM16	
4	IO_L4P_GC_4	AP30	
4	IO_L4N_GC_VREF_4 (1)	AN29	

Table 2-10: **FF1760 Package—LX110, LX155, LX220, and LX330 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
4	IO_L5P_GC_4	AM13	
4	IO_L5N_GC_4 (1)	AM14	
4	IO_L6P_GC_4	AM28	
4	IO_L6N_GC_4 (1)	AN28	
4	IO_L7P_GC_VRN_4	AN15	
4	IO_L7N_GC_VRP_4 (1)	AN14	
4	IO_L8P_CC_GC_4	AL27	
4	IO_L8N_CC_GC_4 (1)(2)	AM27	
4	IO_L9P_CC_GC_4	AP13	
4	IO_L9N_CC_GC_4 (1)(2)	AN13	
5	IO_L0P_5	M24	
5	IO_L0N_5	N24	
5	IO_L1P_5	G14	
5	IO_L1N_5	H14	
5	IO_L2P_5	L25	
5	IO_L2N_5	L24	
5	IO_L3P_5	H16	
5	IO_L3N_5	G16	
5	IO_L4P_5	K25	
5	IO_L4N_VREF_5	K24	
5	IO_L5P_5	J17	
5	IO_L5N_5	J16	
5	IO_L6P_5	M26	
5	IO_L6N_5	L26	
5	IO_L7P_5	H15	
5	IO_L7N_5	J15	
5	IO_L8P_CC_5	P25	
5	IO_L8N_CC_5 (2)	N25	
5	IO_L9P_CC_5	K19	
5	IO_L9N_CC_5 (2)	L19	
5	IO_L10P_CC_5	M18	
5	IO_L10N_CC_5 (2)	M19	
5	IO_L11P_CC_5	J26	

Table 2-10: **FF1760 Package—LX110, LX155, LX220, and LX330 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
5	IO_L11N_CC_5[2]	J27	
5	IO_L12P_VRN_5	K17	
5	IO_L12N_VRP_5	K18	
5	IO_L13P_5	J28	
5	IO_L13N_5	K27	
5	IO_L14P_5	M17	
5	IO_L14N_VREF_5	L17	
5	IO_L15P_5	G27	
5	IO_L15N_5	H28	
5	IO_L16P_5	N18	
5	IO_L16N_5	N19	
5	IO_L17P_5	G28	
5	IO_L17N_5	G29	
5	IO_L18P_5	R18	
5	IO_L18N_5	P18	
5	IO_L19P_5	H29	
5	IO_L19N_5	H30	
6	IO_L0P_6	AL26	
6	IO_L0N_6	AM26	
6	IO_L1P_6	AK18	
6	IO_L1N_6	AL17	
6	IO_L2P_6	AP28	
6	IO_L2N_6	AP27	
6	IO_L3P_6	AM18	
6	IO_L3N_6	AM17	
6	IO_L4P_6	AN26	
6	IO_L4N_VREF_6	AN25	
6	IO_L5P_6	AN18	
6	IO_L5N_6	AP17	
6	IO_L6P_6	AP26	
6	IO_L6N_6	AR27	
6	IO_L7P_6	AN19	
6	IO_L7N_6	AP18	

Table 2-10: **FF1760 Package—LX110, LX155, LX220, and LX330 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
6	IO_L8P_CC_6	AR28	
6	IO_L8N_CC_6 (2)	AR29	
6	IO_L9P_CC_6	AR15	
6	IO_L9N_CC_6 (2)	AP15	
6	IO_L10P_CC_6	AR13	
6	IO_L10N_CC_6 (2)	AR14	
6	IO_L11P_CC_6	AT30	
6	IO_L11N_CC_6 (2)	AR30	
6	IO_L12P_VRN_6	AP16	
6	IO_L12N_VRP_6	AR17	
6	IO_L13P_6	AU29	
6	IO_L13N_6	AT29	
6	IO_L14P_6	AT14	
6	IO_L14N_VREF_6	AT15	
6	IO_L15P_6	AL25	
6	IO_L15N_6	AM24	
6	IO_L16P_6	AK19	
6	IO_L16N_6	AJ18	
6	IO_L17P_6	AJ25	
6	IO_L17N_6	AK24	
6	IO_L18P_6	AL19	
6	IO_L18N_6	AM19	
6	IO_L19P_6	AL24	
6	IO_L19N_6	AK25	
7	IO_L0P_7	M23	LX110, LX155, LX220
7	IO_L0N_7	N23	LX110, LX155, LX220
7	IO_L1P_7	P20	LX110, LX155, LX220
7	IO_L1N_7	N20	LX110, LX155, LX220
7	IO_L2P_7	P23	LX110, LX155, LX220
7	IO_L2N_7	P22	LX110, LX155, LX220
7	IO_L3P_7	P21	LX110, LX155, LX220
7	IO_L3N_7	N21	LX110, LX155, LX220
7	IO_L4P_7	L22	LX110, LX155, LX220

Table 2-10: **FF1760 Package—LX110, LX155, LX220, and LX330 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
7	IO_L4N_VREF_7	M22	LX110, LX155, LX220
7	IO_L5P_7	N22	LX110, LX155, LX220
7	IO_L5N_7	M21	LX110, LX155, LX220
7	IO_L6P_7	K22	LX110, LX155, LX220
7	IO_L6N_7	K23	LX110, LX155, LX220
7	IO_L7P_7	J21	LX110, LX155, LX220
7	IO_L7N_7	H21	LX110, LX155, LX220
7	IO_L8P_CC_7	J22	LX110, LX155, LX220
7	IO_L8N_CC_7 (2)	J23	LX110, LX155, LX220
7	IO_L9P_CC_7	G21	LX110, LX155, LX220
7	IO_L9N_CC_7 (2)	H20	LX110, LX155, LX220
7	IO_L10P_CC_7	H19	LX110, LX155, LX220
7	IO_L10N_CC_7 (2)	G19	LX110, LX155, LX220
7	IO_L11P_CC_7	G22	LX110, LX155, LX220
7	IO_L11N_CC_7 (2)	F22	LX110, LX155, LX220
7	IO_L12P_VRN_7	G17	LX110, LX155, LX220
7	IO_L12N_VRP_7	G18	LX110, LX155, LX220
7	IO_L13P_7	H23	LX110, LX155, LX220
7	IO_L13N_7	G23	LX110, LX155, LX220
7	IO_L14P_7	J18	LX110, LX155, LX220
7	IO_L14N_VREF_7	H18	LX110, LX155, LX220
7	IO_L15P_7	H24	LX110, LX155, LX220
7	IO_L15N_7	G24	LX110, LX155, LX220
7	IO_L16P_7	K20	LX110, LX155, LX220
7	IO_L16N_7	J20	LX110, LX155, LX220
7	IO_L17P_7	H25	LX110, LX155, LX220
7	IO_L17N_7	J25	LX110, LX155, LX220
7	IO_L18P_7	L20	LX110, LX155, LX220
7	IO_L18N_7	L21	LX110, LX155, LX220
7	IO_L19P_7	G26	LX110, LX155, LX220
7	IO_L19N_7	H26	LX110, LX155, LX220
8	IO_L0P_8	AJ23	LX110, LX155, LX220
8	IO_L0N_8	AJ22	LX110, LX155, LX220

Table 2-10: **FF1760 Package—LX110, LX155, LX220, and LX330 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
8	IO_L1P_8	AJ21	LX110, LX155, LX220
8	IO_L1N_8	AJ20	LX110, LX155, LX220
8	IO_L2P_8	AK23	LX110, LX155, LX220
8	IO_L2N_8	AK22	LX110, LX155, LX220
8	IO_L3P_8	AK20	LX110, LX155, LX220
8	IO_L3N_8	AL20	LX110, LX155, LX220
8	IO_L4P_8	AP25	LX110, LX155, LX220
8	IO_L4N_VREF_8	AR25	LX110, LX155, LX220
8	IO_L5P_8	AM21	LX110, LX155, LX220
8	IO_L5N_8	AL21	LX110, LX155, LX220
8	IO_L6P_8	AT27	LX110, LX155, LX220
8	IO_L6N_8	AT26	LX110, LX155, LX220
8	IO_L7P_8	AP20	LX110, LX155, LX220
8	IO_L7N_8	AN20	LX110, LX155, LX220
8	IO_L8P_CC_8	AT25	LX110, LX155, LX220
8	IO_L8N_CC_8 (2)	AT24	LX110, LX155, LX220
8	IO_L9P_CC_8	AN21	LX110, LX155, LX220
8	IO_L9N_CC_8 (2)	AP21	LX110, LX155, LX220
8	IO_L10P_CC_8	AR18	LX110, LX155, LX220
8	IO_L10N_CC_8 (2)	AR19	LX110, LX155, LX220
8	IO_L11P_CC_8	AR23	LX110, LX155, LX220
8	IO_L11N_CC_8 (2)	AR24	LX110, LX155, LX220
8	IO_L12P_VRN_8	AT16	LX110, LX155, LX220
8	IO_L12N_VRP_8	AT17	LX110, LX155, LX220
8	IO_L13P_8	AP23	LX110, LX155, LX220
8	IO_L13N_8	AN24	LX110, LX155, LX220
8	IO_L14P_8	AR20	LX110, LX155, LX220
8	IO_L14N_VREF_8	AT19	LX110, LX155, LX220
8	IO_L15P_8	AM23	LX110, LX155, LX220
8	IO_L15N_8	AN23	LX110, LX155, LX220
8	IO_L16P_8	AT20	LX110, LX155, LX220
8	IO_L16N_8	AT21	LX110, LX155, LX220
8	IO_L17P_8	AL22	LX110, LX155, LX220

Table 2-10: **FF1760 Package—LX110, LX155, LX220, and LX330 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
8	IO_L17N_8	AM22	LX110, LX155, LX220
8	IO_L18P_8	AU21	LX110, LX155, LX220
8	IO_L18N_8	AT22	LX110, LX155, LX220
8	IO_L19P_8	AR22	LX110, LX155, LX220
8	IO_L19N_8	AP22	LX110, LX155, LX220
11	IO_L0P_11	F42	
11	IO_L0N_11	G42	
11	IO_L1P_11	F41	
11	IO_L1N_11	G41	
11	IO_L2P_11	H41	
11	IO_L2N_11	J41	
11	IO_L3P_11	J42	
11	IO_L3N_11	K42	
11	IO_L4P_11	L40	
11	IO_L4N_VREF_11	L41	
11	IO_L5P_11	L42	
11	IO_L5N_11	M41	
11	IO_L6P_11	M42	
11	IO_L6N_11	N41	
11	IO_L7P_11	N40	
11	IO_L7N_11	P40	
11	IO_L8P_CC_11	W40	
11	IO_L8N_CC_11 (2)	Y40	
11	IO_L9P_CC_11	AA40	
11	IO_L9N_CC_11 (2)	AA39	
11	IO_L10P_CC_SM15P_11	Y39	
11	IO_L10N_CC_SM15N_11 (2)	Y38	
11	IO_L11P_CC_SM14P_11	Y37	
11	IO_L11N_CC_SM14N_11 (2)	AA37	
11	IO_L12P_VRN_11	R42	
11	IO_L12N_VRP_11	P42	
11	IO_L13P_11	P41	
11	IO_L13N_11	R40	

Table 2-10: **FF1760 Package—LX110, LX155, LX220, and LX330 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
11	IO_L14P_11	T40	
11	IO_L14N_VREF_11	T41	
11	IO_L15P_SM13P_11	T42	
11	IO_L15N_SM13N_11	U41	
11	IO_L16P_SM12P_11	U42	
11	IO_L16N_SM12N_11	V41	
11	IO_L17P_SM11P_11	V40	
11	IO_L17N_SM11N_11	W41	
11	IO_L18P_SM10P_11	W42	
11	IO_L18N_SM10N_11	Y42	
11	IO_L19P_SM9P_11	AA42	
11	IO_L19N_SM9N_11	AA41	
12	IO_L0P_12	E2	
12	IO_L0N_12	F2	
12	IO_L1P_12	G2	
12	IO_L1N_12	F1	
12	IO_L2P_12	J2	
12	IO_L2N_12	J1	
12	IO_L3P_12	G1	
12	IO_L3N_12	H1	
12	IO_L4P_12	L2	
12	IO_L4N_VREF_12	M2	
12	IO_L5P_12	K2	
12	IO_L5N_12	L1	
12	IO_L6P_12	M1	
12	IO_L6N_12	N1	
12	IO_L7P_12	M3	
12	IO_L7N_12	N3	
12	IO_L8P_CC_12	P3	
12	IO_L8N_CC_12 (2)	R3	
12	IO_L9P_CC_12	P2	
12	IO_L9N_CC_12 (2)	P1	
12	IO_L10P_CC_12	R2	

Table 2-10: **FF1760 Package—LX110, LX155, LX220, and LX330 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
12	IO_L10N_CC_12 (2)	T2	
12	IO_L11P_CC_12	U1	
12	IO_L11N_CC_12 (2)	T1	
12	IO_L12P_VRN_12	U3	
12	IO_L12N_VRP_12	U2	
12	IO_L13P_12	V3	
12	IO_L13N_12	V4	
12	IO_L14P_12	W2	
12	IO_L14N_VREF_12	W3	
12	IO_L15P_12	W1	
12	IO_L15N_12	V1	
12	IO_L16P_12	AA4	
12	IO_L16N_12	Y4	
12	IO_L17P_12	Y5	
12	IO_L17N_12	AA5	
12	IO_L18P_12	AA1	
12	IO_L18N_12	AA2	
12	IO_L19P_12	Y2	
12	IO_L19N_12	Y3	
13	IO_L0P_SM8P_13	AB41	
13	IO_L0N_SM8N_13	AB42	
13	IO_L1P_SM7P_13	AC41	
13	IO_L1N_SM7N_13	AD42	
13	IO_L2P_SM6P_13	AE42	
13	IO_L2N_SM6N_13	AD41	
13	IO_L3P_SM5P_13	AF41	
13	IO_L3N_SM5N_13	AF42	
13	IO_L4P_13	AF40	
13	IO_L4N_VREF_13	AG41	
13	IO_L5P_SM4P_13	AG42	
13	IO_L5N_SM4N_13	AH41	
13	IO_L6P_SM3P_13	AJ42	
13	IO_L6N_SM3N_13	AJ41	

Table 2-10: **FF1760 Package—LX110, LX155, LX220, and LX330 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
13	IO_L7P_SM2P_13	AH40	
13	IO_L7N_SM2N_13	AJ40	
13	IO_L8P_CC_SM1P_13	AB37	
13	IO_L8N_CC_SM1N_13 (2)	AB38	
13	IO_L9P_CC_SM0P_13	AB39	
13	IO_L9N_CC_SM0N_13 (2)	AC38	
13	IO_L10P_CC_13	AE40	
13	IO_L10N_CC_13 (2)	AD40	
13	IO_L11P_CC_13	AC40	
13	IO_L11N_CC_13 (2)	AC39	
13	IO_L12P_VRN_13	AK40	
13	IO_L12N_VRP_13	AL40	
13	IO_L13P_13	AL41	
13	IO_L13N_13	AK42	
13	IO_L14P_13	AL42	
13	IO_L14N_VREF_13	AM42	
13	IO_L15P_13	AM41	
13	IO_L15N_13	AN41	
13	IO_L16P_13	AP42	
13	IO_L16N_13	AP41	
13	IO_L17P_13	AR42	
13	IO_L17N_13	AT42	
13	IO_L18P_13	AT41	
13	IO_L18N_13	AU41	
13	IO_L19P_13	AU42	
13	IO_L19N_13	AV41	
14	IO_L0P_14	AB6	
14	IO_L0N_14	AC6	
14	IO_L1P_14	AC4	
14	IO_L1N_14	AC5	
14	IO_L2P_14	AC3	
14	IO_L2N_14	AD3	
14	IO_L3P_14	AB3	

Table 2-10: **FF1760 Package—LX110, LX155, LX220, and LX330 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
14	IO_L3N_14	AB4	
14	IO_L4P_14	AD2	
14	IO_L4N_VREF_14	AE3	
14	IO_L5P_14	AB2	
14	IO_L5N_14	AB1	
14	IO_L6P_14	AC1	
14	IO_L6N_14	AD1	
14	IO_L7P_14	AE2	
14	IO_L7N_14	AF1	
14	IO_L8P_CC_14	AF2	
14	IO_L8N_CC_14 (2)	AG2	
14	IO_L9P_CC_14	AG3	
14	IO_L9N_CC_14 (2)	AH3	
14	IO_L10P_CC_14	AJ2	
14	IO_L10N_CC_14 (2)	AJ3	
14	IO_L11P_CC_14	AH1	
14	IO_L11N_CC_14 (2)	AG1	
14	IO_L12P_VRN_14	AL2	
14	IO_L12N_VRP_14	AK3	
14	IO_L13P_14	AK2	
14	IO_L13N_14	AJ1	
14	IO_L14P_14	AM3	
14	IO_L14N_VREF_14	AM2	
14	IO_L15P_14	AM1	
14	IO_L15N_14	AL1	
14	IO_L16P_14	AR2	
14	IO_L16N_14	AP2	
14	IO_L17P_14	AP1	
14	IO_L17N_14	AN1	
14	IO_L18P_14	AT1	
14	IO_L18N_14	AT2	
14	IO_L19P_14	AU2	
14	IO_L19N_14	AU1	

Table 2-10: **FF1760 Package—LX110, LX155, LX220, and LX330 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
15	IO_L0P_15	H38	
15	IO_L0N_15	H39	
15	IO_L1P_15	G38	
15	IO_L1N_15	G39	
15	IO_L2P_15	F39	
15	IO_L2N_15	F40	
15	IO_L3P_15	E39	
15	IO_L3N_15	E40	
15	IO_L4P_15	R39	
15	IO_L4N_VREF_15	R38	
15	IO_L5P_15	R37	
15	IO_L5N_15	P37	
15	IO_L6P_15	P38	
15	IO_L6N_15	N38	
15	IO_L7P_15	N39	
15	IO_L7N_15	M39	
15	IO_L8P_CC_15	M38	
15	IO_L8N_CC_15 (2)	L39	
15	IO_L9P_CC_15	K38	
15	IO_L9N_CC_15 (2)	J38	
15	IO_L10P_CC_15	H40	
15	IO_L10N_CC_15 (2)	J40	
15	IO_L11P_CC_15	K40	
15	IO_L11N_CC_15 (2)	K39	
15	IO_L12P_VRN_15	V38	
15	IO_L12N_VRP_15	U37	
15	IO_L13P_15	T37	
15	IO_L13N_15	U38	
15	IO_L14P_15	T39	
15	IO_L14N_VREF_15	U39	
15	IO_L15P_15	V39	
15	IO_L15N_15	W38	
15	IO_L16P_15	AA35	

Table 2-10: **FF1760 Package—LX110, LX155, LX220, and LX330 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
15	IO_L16N_15	AA36	
15	IO_L17P_15	AA34	
15	IO_L17N_15	Y34	
15	IO_L18P_15	Y35	
15	IO_L18N_15	W35	
15	IO_L19P_15	W36	
15	IO_L19N_15	W37	
16	IO_L0P_16	G4	
16	IO_L0N_16	F4	
16	IO_L1P_16	E3	
16	IO_L1N_16	E4	
16	IO_L2P_16	H4	
16	IO_L2N_16	J3	
16	IO_L3P_16	H3	
16	IO_L3N_16	G3	
16	IO_L4P_16	L5	
16	IO_L4N_VREF_16	L4	
16	IO_L5P_16	K3	
16	IO_L5N_16	K4	
16	IO_L6P_16	N5	
16	IO_L6N_16	P5	
16	IO_L7P_16	N4	
16	IO_L7N_16	M4	
16	IO_L8P_CC_16	T6	
16	IO_L8N_CC_16 (2)	T5	
16	IO_L9P_CC_16	R5	
16	IO_L9N_CC_16 (2)	R4	
16	IO_L10P_CC_16	U4	
16	IO_L10N_CC_16 (2)	T4	
16	IO_L11P_CC_16	U6	
16	IO_L11N_CC_16 (2)	V5	
16	IO_L12P_VRN_16	W7	
16	IO_L12N_VRP_16	W8	

Table 2-10: **FF1760 Package—LX110, LX155, LX220, and LX330 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
16	IO_L13P_16	W5	
16	IO_L13N_16	V6	
16	IO_L14P_16	Y7	
16	IO_L14N_VREF_16	W6	
16	IO_L15P_16	AA7	
16	IO_L15N_16	AA6	
16	IO_L16P_16	Y8	
16	IO_L16N_16	AA9	
16	IO_L17P_16	Y10	
16	IO_L17N_16	Y9	
16	IO_L18P_16	W11	
16	IO_L18N_16	W10	
16	IO_L19P_16	AA11	
16	IO_L19N_16	AA10	
17	IO_L0P_17	AB34	
17	IO_L0N_17	AC34	
17	IO_L1P_17	AC35	
17	IO_L1N_17	AB36	
17	IO_L2P_17	AC36	
17	IO_L2N_17	AD35	
17	IO_L3P_17	AD36	
17	IO_L3N_17	AD37	
17	IO_L4P_17	AE37	
17	IO_L4N_VREF_17	AD38	
17	IO_L5P_17	AE39	
17	IO_L5N_17	AE38	
17	IO_L6P_17	AF39	
17	IO_L6N_17	AG38	
17	IO_L7P_17	AG37	
17	IO_L7N_17	AF37	
17	IO_L8P_CC_17	AN40	
17	IO_L8N_CC_17 (2)	AP40	
17	IO_L9P_CC_17	AR40	

Table 2-10: **FF1760 Package—LX110, LX155, LX220, and LX330 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
17	IO_L9N_CC_17(2)	AT40	
17	IO_L10P_CC_17	AV40	
17	IO_L10N_CC_17(2)	AU39	
17	IO_L11P_CC_17	AT39	
17	IO_L11N_CC_17(2)	AR39	
17	IO_L12P_VRN_17	AG39	
17	IO_L12N_VRP_17	AH39	
17	IO_L13P_17	AJ38	
17	IO_L13N_17	AK39	
17	IO_L14P_17	AK38	
17	IO_L14N_VREF_17	AK37	
17	IO_L15P_17	AJ37	
17	IO_L15N_17	AH38	
17	IO_L16P_17	AL39	
17	IO_L16N_17	AM39	
17	IO_L17P_17	AN39	
17	IO_L17N_17	AP38	
17	IO_L18P_17	AN38	
17	IO_L18N_17	AM38	
17	IO_L19P_17	AM37	
17	IO_L19N_17	AL37	
18	IO_L0P_18	AB11	
18	IO_L0N_18	AC11	
18	IO_L1P_18	AD11	
18	IO_L1N_18	AD10	
18	IO_L2P_18	AC10	
18	IO_L2N_18	AC9	
18	IO_L3P_18	AB8	
18	IO_L3N_18	AB9	
18	IO_L4P_18	AC8	
18	IO_L4N_VREF_18	AB7	
18	IO_L5P_18	AD5	
18	IO_L5N_18	AE5	

Table 2-10: **FF1760 Package—LX110, LX155, LX220, and LX330 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
18	IO_L6P_18	AD6	
18	IO_L6N_18	AE7	
18	IO_L7P_18	AD7	
18	IO_L7N_18	AD8	
18	IO_L8P_CC_18	AE4	
18	IO_L8N_CC_18 (2)	AF4	
18	IO_L9P_CC_18	AF6	
18	IO_L9N_CC_18 (2)	AF5	
18	IO_L10P_CC_18	AG6	
18	IO_L10N_CC_18 (2)	AH6	
18	IO_L11P_CC_18	AH4	
18	IO_L11N_CC_18 (2)	AG4	
18	IO_L12P_VRN_18	AJ5	
18	IO_L12N_VRP_18	AK4	
18	IO_L13P_18	AJ6	
18	IO_L13N_18	AH5	
18	IO_L14P_18	AL6	
18	IO_L14N_VREF_18	AL5	
18	IO_L15P_18	AK5	
18	IO_L15N_18	AL4	
18	IO_L16P_18	AP3	
18	IO_L16N_18	AN3	
18	IO_L17P_18	AN4	
18	IO_L17N_18	AM4	
18	IO_L18P_18	AR3	
18	IO_L18N_18	AR4	
18	IO_L19P_18	AM6	
18	IO_L19N_18	AN5	
19	IO_L0P_19	R34	
19	IO_L0N_19	P35	
19	IO_L1P_19	N35	
19	IO_L1N_19	M36	
19	IO_L2P_19	L37	

Table 2-10: **FF1760 Package—LX110, LX155, LX220, and LX330 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
19	IO_L2N_19	M37	
19	IO_L3P_19	N36	
19	IO_L3N_19	P36	
19	IO_L4P_19	L36	
19	IO_L4N_VREF_19	L35	
19	IO_L5P_19	K35	
19	IO_L5N_19	J35	
19	IO_L6P_19	H35	
19	IO_L6N_19	J36	
19	IO_L7P_19	K37	
19	IO_L7N_19	J37	
19	IO_L8P_CC_19	U34	
19	IO_L8N_CC_19(2)	T35	
19	IO_L9P_CC_19	T34	
19	IO_L9N_CC_19(2)	U33	
19	IO_L10P_CC_19	R35	
19	IO_L10N_CC_19(2)	T36	
19	IO_L11P_CC_19	U36	
19	IO_L11N_CC_19(2)	V36	
19	IO_L12P_VRN_19	H36	
19	IO_L12N_VRP_19	G37	
19	IO_L13P_19	F36	
19	IO_L13N_19	G36	
19	IO_L14P_19	F37	
19	IO_L14N_VREF_19	E37	
19	IO_L15P_19	E38	
19	IO_L15N_19	D37	
19	IO_L16P_19	V35	
19	IO_L16N_19	V34	
19	IO_L17P_19	V33	
19	IO_L17N_19	W33	
19	IO_L18P_19	Y33	
19	IO_L18N_19	W32	

Table 2-10: **FF1760 Package—LX110, LX155, LX220, and LX330 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
19	IO_L19P_19	Y32	
19	IO_L19N_19	AA32	
20	IO_L0P_20	G6	
20	IO_L0N_20	F6	
20	IO_L1P_20	F5	
20	IO_L1N_20	E5	
20	IO_L2P_20	G7	
20	IO_L2N_20	H6	
20	IO_L3P_20	J5	
20	IO_L3N_20	H5	
20	IO_L4P_20	J7	
20	IO_L4N_VREF_20	K7	
20	IO_L5P_20	K5	
20	IO_L5N_20	J6	
20	IO_L6P_20	M7	
20	IO_L6N_20	M6	
20	IO_L7P_20	L7	
20	IO_L7N_20	L6	
20	IO_L8P_CC_20	P8	
20	IO_L8N_CC_20 (2)	N9	
20	IO_L9P_CC_20	M8	
20	IO_L9N_CC_20 (2)	M9	
20	IO_L10P_CC_20	P7	
20	IO_L10N_CC_20 (2)	N8	
20	IO_L11P_CC_20	N6	
20	IO_L11N_CC_20 (2)	P6	
20	IO_L12P_VRN_20	T10	
20	IO_L12N_VRP_20	R10	
20	IO_L13P_20	R9	
20	IO_L13N_20	T9	
20	IO_L14P_20	R7	
20	IO_L14N_VREF_20	R8	
20	IO_L15P_20	U7	

Table 2-10: **FF1760 Package—LX110, LX155, LX220, and LX330 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
20	IO_L15N_20	T7	
20	IO_L16P_20	U8	
20	IO_L16N_20	U9	
20	IO_L17P_20	U11	
20	IO_L17N_20	T11	
20	IO_L18P_20	V9	
20	IO_L18N_20	V8	
20	IO_L19P_20	V11	
20	IO_L19N_20	V10	
21	IO_L0P_21	AB33	
21	IO_L0N_21	AB32	
21	IO_L1P_21	AC33	
21	IO_L1N_21	AD32	
21	IO_L2P_21	AD33	
21	IO_L2N_21	AE32	
21	IO_L3P_21	AE33	
21	IO_L3N_21	AE34	
21	IO_L4P_21	AV39	
21	IO_L4N_VREF_21	AV38	
21	IO_L5P_21	AU38	
21	IO_L5N_21	AU37	
21	IO_L6P_21	AT37	
21	IO_L6N_21	AR38	
21	IO_L7P_21	AR37	
21	IO_L7N_21	AT36	
21	IO_L8P_CC_21	AE35	
21	IO_L8N_CC_21 (2)	AF34	
21	IO_L9P_CC_21	AF35	
21	IO_L9N_CC_21 (2)	AF36	
21	IO_L10P_CC_21	AH34	
21	IO_L10N_CC_21 (2)	AG34	
21	IO_L11P_CC_21	AH35	
21	IO_L11N_CC_21 (2)	AG36	

Table 2-10: **FF1760 Package—LX110, LX155, LX220, and LX330 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
21	IO_L12P_VRN_21	AP37	
21	IO_L12N_VRP_21	AP36	
21	IO_L13P_21	AP35	
21	IO_L13N_21	AN36	
21	IO_L14P_21	AM36	
21	IO_L14N_VREF_21	AN35	
21	IO_L15P_21	AN34	
21	IO_L15N_21	AM34	
21	IO_L16P_21	AH36	
21	IO_L16N_21	AJ36	
21	IO_L17P_21	AJ35	
21	IO_L17N_21	AK35	
21	IO_L18P_21	AL36	
21	IO_L18N_21	AL35	
21	IO_L19P_21	AL34	
21	IO_L19N_21	AK34	
22	IO_L0P_22	AF11	
22	IO_L0N_22	AE10	
22	IO_L1P_22	AE9	
22	IO_L1N_22	AE8	
22	IO_L2P_22	AF10	
22	IO_L2N_22	AF9	
22	IO_L3P_22	AG7	
22	IO_L3N_22	AF7	
22	IO_L4P_22	AH8	
22	IO_L4N_VREF_22	AG8	
22	IO_L5P_22	AJ7	
22	IO_L5N_22	AK7	
22	IO_L6P_22	AH9	
22	IO_L6N_22	AJ8	
22	IO_L7P_22	AH10	
22	IO_L7N_22	AG9	
22	IO_L8P_CC_22	AG12	

Table 2-10: **FF1760 Package—LX110, LX155, LX220, and LX330 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
22	IO_L8N_CC_22(2)	AF12	
22	IO_L9P_CC_22	AH11	
22	IO_L9N_CC_22(2)	AG11	
22	IO_L10P_CC_22	AK8	
22	IO_L10N_CC_22(2)	AL7	
22	IO_L11P_CC_22	AL9	
22	IO_L11N_CC_22(2)	AK9	
22	IO_L12P_VRN_22	AM7	
22	IO_L12N_VRP_22	AN6	
22	IO_L13P_22	AN8	
22	IO_L13N_22	AM8	
22	IO_L14P_22	AR5	
22	IO_L14N_VREF_22	AP5	
22	IO_L15P_22	AP7	
22	IO_L15N_22	AP6	
22	IO_L16P_22	AV5	
22	IO_L16N_22	AV4	
22	IO_L17P_22	AU4	
22	IO_L17N_22	AT4	
22	IO_L18P_22	AT5	
22	IO_L18N_22	AT6	
22	IO_L19P_22	AV3	
22	IO_L19N_22	AU3	
23	IO_L0P_23	N33	
23	IO_L0N_23	N34	
23	IO_L1P_23	M34	
23	IO_L1N_23	M33	
23	IO_L2P_23	M32	
23	IO_L2N_23	M31	
23	IO_L3P_23	N31	
23	IO_L3N_23	P31	
23	IO_L4P_23	H34	
23	IO_L4N_VREF_23	G34	

Table 2-10: **FF1760 Package—LX110, LX155, LX220, and LX330 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
23	IO_L5P_23	G33	
23	IO_L5N_23	H33	
23	IO_L6P_23	G32	
23	IO_L6N_23	G31	
23	IO_L7P_23	H31	
23	IO_L7N_23	J31	
23	IO_L8P_CC_23	F35	
23	IO_L8N_CC_23 (2)	E35	
23	IO_L9P_CC_23	E34	
23	IO_L9N_CC_23 (2)	F34	
23	IO_L10P_CC_23	F31	
23	IO_L10N_CC_23 (2)	F32	
23	IO_L11P_CC_23	E32	
23	IO_L11N_CC_23 (2)	E33	
23	IO_L12P_VRN_23	L34	
23	IO_L12N_VRP_23	K34	
23	IO_L13P_23	K33	
23	IO_L13N_23	J33	
23	IO_L14P_23	K32	
23	IO_L14N_VREF_23	J32	
23	IO_L15P_23	L32	
23	IO_L15N_23	L31	
23	IO_L16P_23	P33	
23	IO_L16N_23	P32	
23	IO_L17P_23	R33	
23	IO_L17N_23	R32	
23	IO_L18P_23	T32	
23	IO_L18N_23	U32	
23	IO_L19P_23	U31	
23	IO_L19N_23	T31	
24	IO_L0P_24	P12	
24	IO_L0N_24	P11	
24	IO_L1P_24	P10	

Table 2-10: **FF1760 Package—LX110, LX155, LX220, and LX330 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
24	IO_L1N_24	N10	
24	IO_L2P_24	M12	
24	IO_L2N_24	L12	
24	IO_L3P_24	N11	
24	IO_L3N_24	M11	
24	IO_L4P_24	L9	
24	IO_L4N_VREF_24	K10	
24	IO_L5P_24	L11	
24	IO_L5N_24	L10	
24	IO_L6P_24	K12	
24	IO_L6N_24	J12	
24	IO_L7P_24	J10	
24	IO_L7N_24	J11	
24	IO_L8P_CC_24	H13	
24	IO_L8N_CC_24 (2)	G13	
24	IO_L9P_CC_24	H11	
24	IO_L9N_CC_24 (2)	G12	
24	IO_L10P_CC_24	E12	
24	IO_L10N_CC_24 (2)	E13	
24	IO_L11P_CC_24	F12	
24	IO_L11N_CC_24 (2)	G11	
24	IO_L12P_VRN_24	F10	
24	IO_L12N_VRP_24	F11	
24	IO_L13P_24	H9	
24	IO_L13N_24	H10	
24	IO_L14P_24	E10	
24	IO_L14N_VREF_24	E9	
24	IO_L15P_24	F9	
24	IO_L15N_24	G9	
24	IO_L16P_24	H8	
24	IO_L16N_24	J8	
24	IO_L17P_24	K8	
24	IO_L17N_24	K9	

Table 2-10: **FF1760 Package—LX110, LX155, LX220, and LX330 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
24	IO_L18P_24	E7	
24	IO_L18N_24	E8	
24	IO_L19P_24	F7	
24	IO_L19N_24	G8	
25	IO_L0P_25	AG31	
25	IO_L0N_25	AF31	
25	IO_L1P_25	AF32	
25	IO_L1N_25	AG33	
25	IO_L2P_25	AH33	
25	IO_L2N_25	AG32	
25	IO_L3P_25	AH31	
25	IO_L3N_25	AJ31	
25	IO_L4P_25	AV35	
25	IO_L4N_VREF_25	AV36	
25	IO_L5P_25	AU36	
25	IO_L5N_25	AT35	
25	IO_L6P_25	AU34	
25	IO_L6N_25	AT34	
25	IO_L7P_25	AR35	
25	IO_L7N_25	AR34	
25	IO_L8P_CC_25	AU32	
25	IO_L8N_CC_25 (2)	AU33	
25	IO_L9P_CC_25	AV33	
25	IO_L9N_CC_25 (2)	AV34	
25	IO_L10P_CC_25	AV31	
25	IO_L10N_CC_25 (2)	AU31	
25	IO_L11P_CC_25	AT32	
25	IO_L11N_CC_25 (2)	AT31	
25	IO_L12P_VRN_25	AP31	
25	IO_L12N_VRP_25	AN31	
25	IO_L13P_25	AR32	
25	IO_L13N_25	AP32	
25	IO_L14P_25	AR33	

Table 2-10: **FF1760 Package—LX110, LX155, LX220, and LX330 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
25	IO_L14N_VREF_25	AP33	
25	IO_L15P_25	AN33	
25	IO_L15N_25	AM33	
25	IO_L16P_25	AK33	
25	IO_L16N_25	AJ33	
25	IO_L17P_25	AJ32	
25	IO_L17N_25	AK32	
25	IO_L18P_25	AL32	
25	IO_L18N_25	AM32	
25	IO_L19P_25	AL31	
25	IO_L19N_25	AM31	
26	IO_L0P_26	AV6	
26	IO_L0N_26	AU7	
26	IO_L1P_26	AU8	
26	IO_L1N_26	AV8	
26	IO_L2P_26	AT7	
26	IO_L2N_26	AU6	
26	IO_L3P_26	AR7	
26	IO_L3N_26	AR8	
26	IO_L4P_26	AU9	
26	IO_L4N_VREF_26	AT9	
26	IO_L5P_26	AV10	
26	IO_L5N_26	AV9	
26	IO_L6P_26	AU13	
26	IO_L6N_26	AU12	
26	IO_L7P_26	AV11	
26	IO_L7N_26	AU11	
26	IO_L8P_CC_26	AT10	
26	IO_L8N_CC_26 (2)	AT11	
26	IO_L9P_CC_26	AR9	
26	IO_L9N_CC_26 (2)	AR10	
26	IO_L10P_CC_26	AR12	
26	IO_L10N_CC_26 (2)	AT12	

Table 2-10: **FF1760 Package—LX110, LX155, LX220, and LX330 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
26	IO_L11P_CC_26	AP11	
26	IO_L11N_CC_26 (2)	AP12	
26	IO_L12P_VRN_26	AN9	
26	IO_L12N_VRP_26	AP8	
26	IO_L13P_26	AM9	
26	IO_L13N_26	AN10	
26	IO_L14P_26	AN11	
26	IO_L14N_VREF_26	AP10	
26	IO_L15P_26	AM12	
26	IO_L15N_26	AM11	
26	IO_L16P_26	AL11	
26	IO_L16N_26	AL12	
26	IO_L17P_26	AK10	
26	IO_L17N_26	AL10	
26	IO_L18P_26	AJ10	
26	IO_L18N_26	AJ11	
26	IO_L19P_26	AJ12	
26	IO_L19N_26	AK12	
27	IO_L0P_27	D31	LX110, LX155, LX220
27	IO_L0N_27	C31	LX110, LX155, LX220
27	IO_L1P_27	B31	LX110, LX155, LX220
27	IO_L1N_27	C30	LX110, LX155, LX220
27	IO_L2P_27	A30	LX110, LX155, LX220
27	IO_L2N_27	A31	LX110, LX155, LX220
27	IO_L3P_27	A32	LX110, LX155, LX220
27	IO_L3N_27	B32	LX110, LX155, LX220
27	IO_L4P_27	B33	LX110, LX155, LX220
27	IO_L4N_VREF_27	C33	LX110, LX155, LX220
27	IO_L5P_27	D32	LX110, LX155, LX220
27	IO_L5N_27	D33	LX110, LX155, LX220
27	IO_L6P_27	C34	LX110, LX155, LX220
27	IO_L6N_27	B34	LX110, LX155, LX220
27	IO_L7P_27	A34	LX110, LX155, LX220

Table 2-10: **FF1760 Package—LX110, LX155, LX220, and LX330 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
27	IO_L7N_27	A35	LX110, LX155, LX220
27	IO_L8P_CC_27	D35	LX110, LX155, LX220
27	IO_L8N_CC_27 (2)	D36	LX110, LX155, LX220
27	IO_L9P_CC_27	C36	LX110, LX155, LX220
27	IO_L9N_CC_27 (2)	C35	LX110, LX155, LX220
27	IO_L10P_CC_27	A37	LX110, LX155, LX220
27	IO_L10N_CC_27 (2)	A36	LX110, LX155, LX220
27	IO_L11P_CC_27	B37	LX110, LX155, LX220
27	IO_L11N_CC_27 (2)	B36	LX110, LX155, LX220
27	IO_L12P_VRN_27	C38	LX110, LX155, LX220
27	IO_L12N_VRP_27	D38	LX110, LX155, LX220
27	IO_L13P_27	C39	LX110, LX155, LX220
27	IO_L13N_27	C40	LX110, LX155, LX220
27	IO_L14P_27	B39	LX110, LX155, LX220
27	IO_L14N_VREF_27	B38	LX110, LX155, LX220
27	IO_L15P_27	A39	LX110, LX155, LX220
27	IO_L15N_27	A40	LX110, LX155, LX220
27	IO_L16P_27	A41	LX110, LX155, LX220
27	IO_L16N_27	B41	LX110, LX155, LX220
27	IO_L17P_27	B42	LX110, LX155, LX220
27	IO_L17N_27	C41	LX110, LX155, LX220
27	IO_L18P_27	D40	LX110, LX155, LX220
27	IO_L18N_27	D41	LX110, LX155, LX220
27	IO_L19P_27	E42	LX110, LX155, LX220
27	IO_L19N_27	D42	LX110, LX155, LX220
28	IO_L0P_28	C13	LX110, LX155, LX220
28	IO_L0N_28	D13	LX110, LX155, LX220
28	IO_L1P_28	B11	LX110, LX155, LX220
28	IO_L1N_28	C11	LX110, LX155, LX220
28	IO_L2P_28	B12	LX110, LX155, LX220
28	IO_L2N_28	A12	LX110, LX155, LX220
28	IO_L3P_28	D11	LX110, LX155, LX220
28	IO_L3N_28	D12	LX110, LX155, LX220

Table 2-10: **FF1760 Package—LX110, LX155, LX220, and LX330 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
28	IO_L4P_28	C9	LX110, LX155, LX220
28	IO_L4N_VREF_28	D8	LX110, LX155, LX220
28	IO_L5P_28	A11	LX110, LX155, LX220
28	IO_L5N_28	A10	LX110, LX155, LX220
28	IO_L6P_28	C10	LX110, LX155, LX220
28	IO_L6N_28	D10	LX110, LX155, LX220
28	IO_L7P_28	A9	LX110, LX155, LX220
28	IO_L7N_28	B9	LX110, LX155, LX220
28	IO_L8P_CC_28	C8	LX110, LX155, LX220
28	IO_L8N_CC_28 (2)	B8	LX110, LX155, LX220
28	IO_L9P_CC_28	B6	LX110, LX155, LX220
28	IO_L9N_CC_28 (2)	C6	LX110, LX155, LX220
28	IO_L10P_CC_28	D7	LX110, LX155, LX220
28	IO_L10N_CC_28 (2)	D6	LX110, LX155, LX220
28	IO_L11P_CC_28	A7	LX110, LX155, LX220
28	IO_L11N_CC_28 (2)	B7	LX110, LX155, LX220
28	IO_L12P_VRN_28	A5	LX110, LX155, LX220
28	IO_L12N_VRP_28	A6	LX110, LX155, LX220
28	IO_L13P_28	B4	LX110, LX155, LX220
28	IO_L13N_28	A4	LX110, LX155, LX220
28	IO_L14P_28	C5	LX110, LX155, LX220
28	IO_L14N_VREF_28	D5	LX110, LX155, LX220
28	IO_L15P_28	D3	LX110, LX155, LX220
28	IO_L15N_28	C4	LX110, LX155, LX220
28	IO_L16P_28	B3	LX110, LX155, LX220
28	IO_L16N_28	C3	LX110, LX155, LX220
28	IO_L17P_28	C1	LX110, LX155, LX220
28	IO_L17N_28	B1	LX110, LX155, LX220
28	IO_L18P_28	A2	LX110, LX155, LX220
28	IO_L18N_28	B2	LX110, LX155, LX220
28	IO_L19P_28	D1	LX110, LX155, LX220
28	IO_L19N_28	D2	LX110, LX155, LX220
29	IO_L0P_29	AY42	LX110, LX155, LX220

Table 2-10: **FF1760 Package—LX110, LX155, LX220, and LX330 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
29	IO_L0N_29	AW42	LX110, LX155, LX220
29	IO_L1P_29	AW41	LX110, LX155, LX220
29	IO_L1N_29	AW40	LX110, LX155, LX220
29	IO_L2P_29	AY40	LX110, LX155, LX220
29	IO_L2N_29	BA41	LX110, LX155, LX220
29	IO_L3P_29	BA42	LX110, LX155, LX220
29	IO_L3N_29	BB41	LX110, LX155, LX220
29	IO_L4P_29	BA40	LX110, LX155, LX220
29	IO_L4N_VREF_29	BB39	LX110, LX155, LX220
29	IO_L5P_29	BB38	LX110, LX155, LX220
29	IO_L5N_29	BA39	LX110, LX155, LX220
29	IO_L6P_29	AY38	LX110, LX155, LX220
29	IO_L6N_29	AW37	LX110, LX155, LX220
29	IO_L7P_29	AW38	LX110, LX155, LX220
29	IO_L7N_29	AY39	LX110, LX155, LX220
29	IO_L8P_CC_29	BB37	LX110, LX155, LX220
29	IO_L8N_CC_29 (2)	BA37	LX110, LX155, LX220
29	IO_L9P_CC_29	AY37	LX110, LX155, LX220
29	IO_L9N_CC_29 (2)	AW36	LX110, LX155, LX220
29	IO_L10P_CC_29	BB36	LX110, LX155, LX220
29	IO_L10N_CC_29 (2)	BA36	LX110, LX155, LX220
29	IO_L11P_CC_29	AY35	LX110, LX155, LX220
29	IO_L11N_CC_29 (2)	AW35	LX110, LX155, LX220
29	IO_L12P_VRN_29	BB34	LX110, LX155, LX220
29	IO_L12N_VRP_29	BA35	LX110, LX155, LX220
29	IO_L13P_29	BB33	LX110, LX155, LX220
29	IO_L13N_29	BA34	LX110, LX155, LX220
29	IO_L14P_29	AY33	LX110, LX155, LX220
29	IO_L14N_VREF_29	AY34	LX110, LX155, LX220
29	IO_L15P_29	AW33	LX110, LX155, LX220
29	IO_L15N_29	AW32	LX110, LX155, LX220
29	IO_L16P_29	AY32	LX110, LX155, LX220
29	IO_L16N_29	BA32	LX110, LX155, LX220

Table 2-10: **FF1760 Package—LX110, LX155, LX220, and LX330 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
29	IO_L17P_29	BB32	LX110, LX155, LX220
29	IO_L17N_29	BB31	LX110, LX155, LX220
29	IO_L18P_29	BA30	LX110, LX155, LX220
29	IO_L18N_29	BA31	LX110, LX155, LX220
29	IO_L19P_29	AY30	LX110, LX155, LX220
29	IO_L19N_29	AW31	LX110, LX155, LX220
30	IO_L0P_30	AV1	LX110, LX155, LX220
30	IO_L0N_30	AW1	LX110, LX155, LX220
30	IO_L1P_30	AW2	LX110, LX155, LX220
30	IO_L1N_30	AY2	LX110, LX155, LX220
30	IO_L2P_30	BA1	LX110, LX155, LX220
30	IO_L2N_30	BA2	LX110, LX155, LX220
30	IO_L3P_30	AY3	LX110, LX155, LX220
30	IO_L3N_30	AW3	LX110, LX155, LX220
30	IO_L4P_30	BB2	LX110, LX155, LX220
30	IO_L4N_VREF_30	BB3	LX110, LX155, LX220
30	IO_L5P_30	AY5	LX110, LX155, LX220
30	IO_L5N_30	AW5	LX110, LX155, LX220
30	IO_L6P_30	AY4	LX110, LX155, LX220
30	IO_L6N_30	BA4	LX110, LX155, LX220
30	IO_L7P_30	BA5	LX110, LX155, LX220
30	IO_L7N_30	BB4	LX110, LX155, LX220
30	IO_L8P_CC_30	BB7	LX110, LX155, LX220
30	IO_L8N_CC_30 (2)	BA7	LX110, LX155, LX220
30	IO_L9P_CC_30	AW7	LX110, LX155, LX220
30	IO_L9N_CC_30 (2)	AW6	LX110, LX155, LX220
30	IO_L10P_CC_30	BB6	LX110, LX155, LX220
30	IO_L10N_CC_30 (2)	BA6	LX110, LX155, LX220
30	IO_L11P_CC_30	AY7	LX110, LX155, LX220
30	IO_L11N_CC_30 (2)	AW8	LX110, LX155, LX220
30	IO_L12P_VRN_30	BB8	LX110, LX155, LX220
30	IO_L12N_VRP_30	BA9	LX110, LX155, LX220
30	IO_L13P_30	AY10	LX110, LX155, LX220

Table 2-10: **FF1760 Package—LX110, LX155, LX220, and LX330 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
30	IO_L13N_30	AW10	LX110, LX155, LX220
30	IO_L14P_30	BB9	LX110, LX155, LX220
30	IO_L14N_VREF_30	BA10	LX110, LX155, LX220
30	IO_L15P_30	AY8	LX110, LX155, LX220
30	IO_L15N_30	AY9	LX110, LX155, LX220
30	IO_L16P_30	AW11	LX110, LX155, LX220
30	IO_L16N_30	AW12	LX110, LX155, LX220
30	IO_L17P_30	BA12	LX110, LX155, LX220
30	IO_L17N_30	BB12	LX110, LX155, LX220
30	IO_L18P_30	BB11	LX110, LX155, LX220
30	IO_L18N_30	BA11	LX110, LX155, LX220
30	IO_L19P_30	AY13	LX110, LX155, LX220
30	IO_L19N_30	AY12	LX110, LX155, LX220
31	IO_L0P_31	E14	LX110, LX155, LX220
31	IO_L0N_31	D15	LX110, LX155, LX220
31	IO_L1P_31	E15	LX110, LX155, LX220
31	IO_L1N_31	F14	LX110, LX155, LX220
31	IO_L2P_31	D16	LX110, LX155, LX220
31	IO_L2N_31	D17	LX110, LX155, LX220
31	IO_L3P_31	F16	LX110, LX155, LX220
31	IO_L3N_31	F15	LX110, LX155, LX220
31	IO_L4P_31	F17	LX110, LX155, LX220
31	IO_L4N_VREF_31	E17	LX110, LX155, LX220
31	IO_L5P_31	E20	LX110, LX155, LX220
31	IO_L5N_31	F20	LX110, LX155, LX220
31	IO_L6P_31	D18	LX110, LX155, LX220
31	IO_L6N_31	E18	LX110, LX155, LX220
31	IO_L7P_31	E19	LX110, LX155, LX220
31	IO_L7N_31	F19	LX110, LX155, LX220
31	IO_L8P_CC_31	D22	LX110, LX155, LX220
31	IO_L8N_CC_31 (2)	D23	LX110, LX155, LX220
31	IO_L9P_CC_31	D21	LX110, LX155, LX220
31	IO_L9N_CC_31 (2)	D20	LX110, LX155, LX220

Table 2-10: **FF1760 Package—LX110, LX155, LX220, and LX330 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
31	IO_L10P_CC_31	F21	LX110, LX155, LX220
31	IO_L10N_CC_31 (2)	E22	LX110, LX155, LX220
31	IO_L11P_CC_31	E23	LX110, LX155, LX220
31	IO_L11N_CC_31 (2)	F24	LX110, LX155, LX220
31	IO_L12P_VRN_31	D25	LX110, LX155, LX220
31	IO_L12N_VRP_31	D26	LX110, LX155, LX220
31	IO_L13P_31	E24	LX110, LX155, LX220
31	IO_L13N_31	E25	LX110, LX155, LX220
31	IO_L14P_31	F27	LX110, LX155, LX220
31	IO_L14N_VREF_31	E27	LX110, LX155, LX220
31	IO_L15P_31	F26	LX110, LX155, LX220
31	IO_L15N_31	F25	LX110, LX155, LX220
31	IO_L16P_31	E29	LX110, LX155, LX220
31	IO_L16N_31	E28	LX110, LX155, LX220
31	IO_L17P_31	D27	LX110, LX155, LX220
31	IO_L17N_31	D28	LX110, LX155, LX220
31	IO_L18P_31	F30	LX110, LX155, LX220
31	IO_L18N_31	F29	LX110, LX155, LX220
31	IO_L19P_31	D30	LX110, LX155, LX220
31	IO_L19N_31	E30	LX110, LX155, LX220
32	IO_L0P_32	A29	LX110, LX155, LX220
32	IO_L0N_32	B29	LX110, LX155, LX220
32	IO_L1P_32	B27	LX110, LX155, LX220
32	IO_L1N_32	A26	LX110, LX155, LX220
32	IO_L2P_32	C29	LX110, LX155, LX220
32	IO_L2N_32	C28	LX110, LX155, LX220
32	IO_L3P_32	B28	LX110, LX155, LX220
32	IO_L3N_32	A27	LX110, LX155, LX220
32	IO_L4P_32	B24	LX110, LX155, LX220
32	IO_L4N_VREF_32	A25	LX110, LX155, LX220
32	IO_L5P_32	C24	LX110, LX155, LX220
32	IO_L5N_32	C25	LX110, LX155, LX220
32	IO_L6P_32	B23	LX110, LX155, LX220

Table 2-10: **FF1760 Package—LX110, LX155, LX220, and LX330 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
32	IO_L6N_32	A24	LX110, LX155, LX220
32	IO_L7P_32	C26	LX110, LX155, LX220
32	IO_L7N_32	B26	LX110, LX155, LX220
32	IO_L8P_CC_32	C23	LX110, LX155, LX220
32	IO_L8N_CC_32 (2)	B22	LX110, LX155, LX220
32	IO_L9P_CC_32	C21	LX110, LX155, LX220
32	IO_L9N_CC_32 (2)	C20	LX110, LX155, LX220
32	IO_L10P_CC_32	A20	LX110, LX155, LX220
32	IO_L10N_CC_32 (2)	B21	LX110, LX155, LX220
32	IO_L11P_CC_32	A21	LX110, LX155, LX220
32	IO_L11N_CC_32 (2)	A22	LX110, LX155, LX220
32	IO_L12P_VRN_32	A19	LX110, LX155, LX220
32	IO_L12N_VRP_32	B19	LX110, LX155, LX220
32	IO_L13P_32	C18	LX110, LX155, LX220
32	IO_L13N_32	C19	LX110, LX155, LX220
32	IO_L14P_32	A16	LX110, LX155, LX220
32	IO_L14N_VREF_32	A17	LX110, LX155, LX220
32	IO_L15P_32	B17	LX110, LX155, LX220
32	IO_L15N_32	B18	LX110, LX155, LX220
32	IO_L16P_32	A14	LX110, LX155, LX220
32	IO_L16N_32	A15	LX110, LX155, LX220
32	IO_L17P_32	B16	LX110, LX155, LX220
32	IO_L17N_32	C16	LX110, LX155, LX220
32	IO_L18P_32	C14	LX110, LX155, LX220
32	IO_L18N_32	C15	LX110, LX155, LX220
32	IO_L19P_32	B13	LX110, LX155, LX220
32	IO_L19N_32	B14	LX110, LX155, LX220
33	IO_L0P_33	AV29	LX110, LX155, LX220
33	IO_L0N_33	AW28	LX110, LX155, LX220
33	IO_L1P_33	AV26	LX110, LX155, LX220
33	IO_L1N_33	AU26	LX110, LX155, LX220
33	IO_L2P_33	AV30	LX110, LX155, LX220
33	IO_L2N_33	AW30	LX110, LX155, LX220

Table 2-10: **FF1760 Package—LX110, LX155, LX220, and LX330 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
33	IO_L3P_33	AV25	LX110, LX155, LX220
33	IO_L3N_33	AU24	LX110, LX155, LX220
33	IO_L4P_33	AU28	LX110, LX155, LX220
33	IO_L4N_VREF_33	AU27	LX110, LX155, LX220
33	IO_L5P_33	AW23	LX110, LX155, LX220
33	IO_L5N_33	AW22	LX110, LX155, LX220
33	IO_L6P_33	AW27	LX110, LX155, LX220
33	IO_L6N_33	AV28	LX110, LX155, LX220
33	IO_L7P_33	AV24	LX110, LX155, LX220
33	IO_L7N_33	AV23	LX110, LX155, LX220
33	IO_L8P_CC_33	AW26	LX110, LX155, LX220
33	IO_L8N_CC_33 (2)	AW25	LX110, LX155, LX220
33	IO_L9P_CC_33	AU23	LX110, LX155, LX220
33	IO_L9N_CC_33 (2)	AU22	LX110, LX155, LX220
33	IO_L10P_CC_33	AV21	LX110, LX155, LX220
33	IO_L10N_CC_33 (2)	AV20	LX110, LX155, LX220
33	IO_L11P_CC_33	AW21	LX110, LX155, LX220
33	IO_L11N_CC_33 (2)	AW20	LX110, LX155, LX220
33	IO_L12P_VRN_33	AU18	LX110, LX155, LX220
33	IO_L12N_VRP_33	AU19	LX110, LX155, LX220
33	IO_L13P_33	AW18	LX110, LX155, LX220
33	IO_L13N_33	AV19	LX110, LX155, LX220
33	IO_L14P_33	AU17	LX110, LX155, LX220
33	IO_L14N_VREF_33	AU16	LX110, LX155, LX220
33	IO_L15P_33	AW17	LX110, LX155, LX220
33	IO_L15N_33	AV18	LX110, LX155, LX220
33	IO_L16P_33	AV13	LX110, LX155, LX220
33	IO_L16N_33	AW13	LX110, LX155, LX220
33	IO_L17P_33	AW16	LX110, LX155, LX220
33	IO_L17N_33	AV16	LX110, LX155, LX220
33	IO_L18P_33	AU14	LX110, LX155, LX220
33	IO_L18N_33	AV14	LX110, LX155, LX220
33	IO_L19P_33	AW15	LX110, LX155, LX220

Table 2-10: **FF1760 Package—LX110, LX155, LX220, and LX330 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
33	IO_L19N_33	AV15	LX110, LX155, LX220
34	IO_L0P_34	BB13	LX110, LX155, LX220
34	IO_L0N_34	BA14	LX110, LX155, LX220
34	IO_L1P_34	AY14	LX110, LX155, LX220
34	IO_L1N_34	AY15	LX110, LX155, LX220
34	IO_L2P_34	BB16	LX110, LX155, LX220
34	IO_L2N_34	BA16	LX110, LX155, LX220
34	IO_L3P_34	BA15	LX110, LX155, LX220
34	IO_L3N_34	BB14	LX110, LX155, LX220
34	IO_L4P_34	BB18	LX110, LX155, LX220
34	IO_L4N_VREF_34	BB19	LX110, LX155, LX220
34	IO_L5P_34	BB17	LX110, LX155, LX220
34	IO_L5N_34	BA17	LX110, LX155, LX220
34	IO_L6P_34	AY19	LX110, LX155, LX220
34	IO_L6N_34	BA19	LX110, LX155, LX220
34	IO_L7P_34	AY17	LX110, LX155, LX220
34	IO_L7N_34	AY18	LX110, LX155, LX220
34	IO_L8P_CC_34	BA21	LX110, LX155, LX220
34	IO_L8N_CC_34 (2)	BA22	LX110, LX155, LX220
34	IO_L9P_CC_34	BB21	LX110, LX155, LX220
34	IO_L9N_CC_34 (2)	BB22	LX110, LX155, LX220
34	IO_L10P_CC_34	BA20	LX110, LX155, LX220
34	IO_L10N_CC_34 (2)	AY20	LX110, LX155, LX220
34	IO_L11P_CC_34	AY22	LX110, LX155, LX220
34	IO_L11N_CC_34 (2)	AY23	LX110, LX155, LX220
34	IO_L12P_VRN_34	AY25	LX110, LX155, LX220
34	IO_L12N_VRP_34	AY24	LX110, LX155, LX220
34	IO_L13P_34	BB23	LX110, LX155, LX220
34	IO_L13N_34	BA24	LX110, LX155, LX220
34	IO_L14P_34	BB26	LX110, LX155, LX220
34	IO_L14N_VREF_34	BA26	LX110, LX155, LX220
34	IO_L15P_34	BB24	LX110, LX155, LX220
34	IO_L15N_34	BA25	LX110, LX155, LX220

Table 2-10: **FF1760 Package—LX110, LX155, LX220, and LX330 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
34	IO_L16P_34	BA27	LX110, LX155, LX220
34	IO_L16N_34	BB27	LX110, LX155, LX220
34	IO_L17P_34	AY27	LX110, LX155, LX220
34	IO_L17N_34	AY28	LX110, LX155, LX220
34	IO_L18P_34	BB29	LX110, LX155, LX220
34	IO_L18N_34	BB28	LX110, LX155, LX220
34	IO_L19P_34	BA29	LX110, LX155, LX220
34	IO_L19N_34	AY29	LX110, LX155, LX220
NA	GND	E1	
NA	GND	K1	
NA	GND	R1	
NA	GND	Y1	
NA	GND	AE1	
NA	GND	AK1	
NA	GND	AR1	
NA	GND	AY1	
NA	GND	C2	
NA	GND	H2	
NA	GND	N2	
NA	GND	V2	
NA	GND	AC2	
NA	GND	AH2	
NA	GND	AN2	
NA	GND	AV2	
NA	GND	A3	
NA	GND	L3	
NA	GND	AA3	
NA	GND	AL3	
NA	GND	BA3	
NA	GND	D4	
NA	GND	P4	
NA	GND	AD4	
NA	GND	AP4	

Table 2-10: **FF1760 Package—LX110, LX155, LX220, and LX330 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	B5	
NA	GND	G5	
NA	GND	U5	
NA	GND	AG5	
NA	GND	AU5	
NA	GND	BB5	
NA	GND	K6	
NA	GND	Y6	
NA	GND	AK6	
NA	GND	AY6	
NA	GND	C7	
NA	GND	N7	
NA	GND	AC7	
NA	GND	AN7	
NA	GND	A8	
NA	GND	F8	
NA	GND	T8	
NA	GND	AF8	
NA	GND	AT8	
NA	GND	J9	
NA	GND	W9	
NA	GND	AJ9	
NA	GND	AW9	
NA	GND	B10	
NA	GND	M10	
NA	GND	U10	
NA	GND	AB10	
NA	GND	AM10	
NA	GND	BB10	
NA	GND	E11	
NA	GND	K11	
NA	GND	R11	
NA	GND	Y11	

Table 2-10: **FF1760 Package—LX110, LX155, LX220, and LX330 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	AE11	
NA	GND	AK11	
NA	GND	AR11	
NA	GND	H12	
NA	GND	N12	
NA	GND	T12	
NA	GND	V12	
NA	GND	Y12	
NA	GND	AB12	
NA	GND	AD12	
NA	GND	AH12	
NA	GND	AN12	
NA	GND	AV12	
NA	GND	A13	
NA	GND	L13	
NA	GND	R13	
NA	GND	U13	
NA	GND	W13	
NA	GND	AA13	
NA	GND	AC13	
NA	GND	AE13	
NA	GND	AG13	
NA	GND	AL13	
NA	GND	BA13	
NA	GND	D14	
NA	GND	P14	
NA	GND	V14	
NA	GND	Y14	
NA	GND	AB14	
NA	GND	AD14	
NA	GND	AJ14	
NA	GND	AP14	
NA	GND	G15	

Table 2-10: **FF1760 Package—LX110, LX155, LX220, and LX330 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	M15	
NA	GND	U15	
NA	GND	W15	
NA	GND	AA15	
NA	GND	AC15	
NA	GND	AE15	
NA	GND	AG15	
NA	GND	AM15	
NA	GND	AU15	
NA	GND	BB15	
NA	GND	K16	
NA	GND	R16	
NA	GND	T16	
NA	GND	V16	
NA	GND	Y16	
NA	GND	AB16	
NA	GND	AD16	
NA	GND	AF16	
NA	GND	AK16	
NA	GND	AY16	
NA	GND	C17	
NA	GND	N17	
NA	GND	U17	
NA	GND	W17	
NA	GND	AA17	
NA	GND	AC17	
NA	GND	AE17	
NA	GND	AG17	
NA	GND	AN17	
NA	GND	A18	
NA	GND	F18	
NA	GND	L18	
NA	GND	T18	

Table 2-10: **FF1760 Package—LX110, LX155, LX220, and LX330 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	V18	
NA	GND	Y18	
NA	GND	AB18	
NA	GND	AD18	
NA	GND	AF18	
NA	GND	AH18	
NA	GND	AL18	
NA	GND	AT18	
NA	GND	J19	
NA	GND	P19	
NA	GND	R19	
NA	GND	U19	
NA	GND	W19	
NA	GND	AA19	
NA	GND	AC19	
NA	GND	AE19	
NA	GND	AG19	
NA	GND	AJ19	
NA	GND	AW19	
NA	GND	B20	
NA	GND	M20	
NA	GND	T20	
NA	GND	V20	
NA	GND	Y20	
NA	GND	AB20	
NA	GND	AD20	
NA	GND	AF20	
NA	GND	AH20	
NA	GND	AM20	
NA	GND	BB20	
NA	GND	E21	
NA	GND	K21	
NA	GND	R21	

Table 2-10: **FF1760 Package—LX110, LX155, LX220, and LX330 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	U21	
NA	GND	W21	
NA	GND	AE21	
NA	GND	AG21	
NA	GND	AK21	
NA	GND	AR21	
NA	GND	H22	
NA	GND	T22	
NA	GND	V22	
NA	GND	AD22	
NA	GND	AF22	
NA	GND	AH22	
NA	GND	AN22	
NA	GND	AV22	
NA	GND	A23	
NA	GND	L23	
NA	GND	R23	
NA	GND	U23	
NA	GND	W23	
NA	GND	AA23	
NA	GND	AC23	
NA	GND	AE23	
NA	GND	AG23	
NA	GND	AL23	
NA	GND	BA23	
NA	GND	D24	
NA	GND	P24	
NA	GND	T24	
NA	GND	V24	
NA	GND	Y24	
NA	GND	AB24	
NA	GND	AD24	
NA	GND	AF24	

Table 2-10: **FF1760 Package—LX110, LX155, LX220, and LX330 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	AH24	
NA	GND	AP24	
NA	GND	G25	
NA	GND	M25	
NA	GND	R25	
NA	GND	U25	
NA	GND	W25	
NA	GND	AA25	
NA	GND	AC25	
NA	GND	AE25	
NA	GND	AG25	
NA	GND	AM25	
NA	GND	AU25	
NA	GND	BB25	
NA	GND	K26	
NA	GND	T26	
NA	GND	V26	
NA	GND	Y26	
NA	GND	AB26	
NA	GND	AD26	
NA	GND	AF26	
NA	GND	AH26	
NA	GND	AK26	
NA	GND	AY26	
NA	GND	C27	
NA	GND	N27	
NA	GND	U27	
NA	GND	W27	
NA	GND	AA27	
NA	GND	AC27	
NA	GND	AE27	
NA	GND	AG27	
NA	GND	AN27	

Table 2-10: **FF1760 Package—LX110, LX155, LX220, and LX330 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	A28	
NA	GND	F28	
NA	GND	L28	
NA	GND	T28	
NA	GND	V28	
NA	GND	Y28	
NA	GND	AB28	
NA	GND	AD28	
NA	GND	AF28	
NA	GND	AT28	
NA	GND	J29	
NA	GND	P29	
NA	GND	U29	
NA	GND	W29	
NA	GND	AA29	
NA	GND	AC29	
NA	GND	AE29	
NA	GND	AJ29	
NA	GND	AP29	
NA	GND	AW29	
NA	GND	B30	
NA	GND	M30	
NA	GND	V30	
NA	GND	Y30	
NA	GND	AB30	
NA	GND	AD30	
NA	GND	AM30	
NA	GND	BB30	
NA	GND	E31	
NA	GND	K31	
NA	GND	R31	
NA	GND	W31	
NA	GND	AA31	

Table 2-10: **FF1760 Package—LX110, LX155, LX220, and LX330 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	AC31	
NA	GND	AE31	
NA	GND	AK31	
NA	GND	AR31	
NA	GND	H32	
NA	GND	N32	
NA	GND	V32	
NA	GND	AC32	
NA	GND	AH32	
NA	GND	AN32	
NA	GND	AV32	
NA	GND	A33	
NA	GND	L33	
NA	GND	T33	
NA	GND	AA33	
NA	GND	AF33	
NA	GND	AL33	
NA	GND	BA33	
NA	GND	D34	
NA	GND	J34	
NA	GND	P34	
NA	GND	W34	
NA	GND	AD34	
NA	GND	AP34	
NA	GND	G35	
NA	GND	U35	
NA	GND	AG35	
NA	GND	AU35	
NA	GND	BB35	
NA	GND	K36	
NA	GND	Y36	
NA	GND	AK36	
NA	GND	AY36	

Table 2-10: **FF1760 Package—LX110, LX155, LX220, and LX330 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	C37	
NA	GND	N37	
NA	GND	AC37	
NA	GND	AN37	
NA	GND	A38	
NA	GND	F38	
NA	GND	T38	
NA	GND	AF38	
NA	GND	AT38	
NA	GND	BA38	
NA	GND	J39	
NA	GND	W39	
NA	GND	AJ39	
NA	GND	AW39	
NA	GND	B40	
NA	GND	M40	
NA	GND	AB40	
NA	GND	AM40	
NA	GND	BB40	
NA	GND	E41	
NA	GND	R41	
NA	GND	AE41	
NA	GND	AK41	
NA	GND	AR41	
NA	GND	AY41	
NA	GND	C42	
NA	GND	H42	
NA	GND	N42	
NA	GND	V42	
NA	GND	AC42	
NA	GND	AH42	
NA	GND	AN42	
NA	GND	AV42	

Table 2-10: **FF1760 Package—LX110, LX155, LX220, and LX330 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	VCCAUX	R12	
NA	VCCAUX	AF29	
NA	VCCAUX	U12	
NA	VCCAUX	U30	
NA	VCCAUX	W12	
NA	VCCAUX	W30	
NA	VCCAUX	AA12	
NA	VCCAUX	AA30	
NA	VCCAUX	AC12	
NA	VCCAUX	AC30	
NA	VCCAUX	AE12	
NA	VCCAUX	Y31	
NA	VCCAUX	T13	
NA	VCCAUX	AB31	
NA	VCCAUX	AD13	
NA	VCCAUX	AF13	
NA	VCCAUX	AH13	
NA	VCCAUX	V29	
NA	VCCAUX	AB29	
NA	VCCAUX	AD29	
NA	VCCINT	V13	
NA	VCCINT	Y13	
NA	VCCINT	AB13	
NA	VCCINT	W14	
NA	VCCINT	AA14	
NA	VCCINT	AC14	
NA	VCCINT	AE14	
NA	VCCINT	V15	
NA	VCCINT	Y15	
NA	VCCINT	AB15	
NA	VCCINT	AD15	
NA	VCCINT	U16	
NA	VCCINT	W16	

Table 2-10: **FF1760 Package—LX110, LX155, LX220, and LX330 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	VCCINT	AA16	
NA	VCCINT	AC16	
NA	VCCINT	AE16	
NA	VCCINT	AG16	
NA	VCCINT	T17	
NA	VCCINT	V17	
NA	VCCINT	Y17	
NA	VCCINT	AB17	
NA	VCCINT	AD17	
NA	VCCINT	AF17	
NA	VCCINT	AH17	
NA	VCCINT	U18	
NA	VCCINT	W18	
NA	VCCINT	AA18	
NA	VCCINT	AC18	
NA	VCCINT	AE18	
NA	VCCINT	AG18	
NA	VCCINT	T19	
NA	VCCINT	V19	
NA	VCCINT	Y19	
NA	VCCINT	AB19	
NA	VCCINT	AD19	
NA	VCCINT	AF19	
NA	VCCINT	AH19	
NA	VCCINT	R20	
NA	VCCINT	U20	
NA	VCCINT	W20	
NA	VCCINT	AA20	
NA	VCCINT	AC20	
NA	VCCINT	AE20	
NA	VCCINT	AG20	
NA	VCCINT	T21	
NA	VCCINT	V21	

Table 2-10: **FF1760 Package—LX110, LX155, LX220, and LX330 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	VCCINT	AD21	
NA	VCCINT	AF21	
NA	VCCINT	AH21	
NA	VCCINT	R22	
NA	VCCINT	U22	
NA	VCCINT	W22	
NA	VCCINT	AE22	
NA	VCCINT	AG22	
NA	VCCINT	T23	
NA	VCCINT	V23	
NA	VCCINT	Y23	
NA	VCCINT	AB23	
NA	VCCINT	AD23	
NA	VCCINT	AF23	
NA	VCCINT	AH23	
NA	VCCINT	R24	
NA	VCCINT	U24	
NA	VCCINT	W24	
NA	VCCINT	AA24	
NA	VCCINT	AC24	
NA	VCCINT	AE24	
NA	VCCINT	AG24	
NA	VCCINT	AJ24	
NA	VCCINT	T25	
NA	VCCINT	V25	
NA	VCCINT	Y25	
NA	VCCINT	AB25	
NA	VCCINT	AD25	
NA	VCCINT	AF25	
NA	VCCINT	AH25	
NA	VCCINT	R26	
NA	VCCINT	U26	
NA	VCCINT	W26	

Table 2-10: **FF1760 Package—LX110, LX155, LX220, and LX330 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	VCCINT	AA26	
NA	VCCINT	AC26	
NA	VCCINT	AE26	
NA	VCCINT	AG26	
NA	VCCINT	T27	
NA	VCCINT	V27	
NA	VCCINT	Y27	
NA	VCCINT	AB27	
NA	VCCINT	AD27	
NA	VCCINT	AF27	
NA	VCCINT	AH27	
NA	VCCINT	U28	
NA	VCCINT	W28	
NA	VCCINT	AA28	
NA	VCCINT	AC28	
NA	VCCINT	AE28	
NA	VCCINT	AG28	
NA	VCCINT	Y29	
0	VCCO_0	AL28	
0	VCCO_0	AG30	
1	VCCO_1	J14	
1	VCCO_1	E16	
2	VCCO_2	AR26	
2	VCCO_2	AV27	
3	VCCO_3	J24	
3	VCCO_3	E26	
4	VCCO_4	AV17	
4	VCCO_4	BA18	
5	VCCO_5	C22	
5	VCCO_5	F23	
5	VCCO_5	B25	
6	VCCO_6	AY21	
6	VCCO_6	AT23	

Table 2-10: **FF1760 Package—LX110, LX155, LX220, and LX330 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
6	VCCO_6	AW24	
7	VCCO_7	H17	
7	VCCO_7	D19	
7	VCCO_7	G20	
8	VCCO_8	AR16	
8	VCCO_8	AP19	
8	VCCO_8	AU20	
11	VCCO_11	V37	
11	VCCO_11	U40	
11	VCCO_11	Y41	
12	VCCO_12	W4	
12	VCCO_12	AB5	
12	VCCO_12	AA8	
13	VCCO_13	AB35	
13	VCCO_13	AA38	
13	VCCO_13	AD39	
14	VCCO_14	AE6	
14	VCCO_14	AD9	
14	VCCO_14	AG10	
15	VCCO_15	M35	
15	VCCO_15	R36	
15	VCCO_15	P39	
16	VCCO_16	T3	
16	VCCO_16	R6	
16	VCCO_16	V7	
17	VCCO_17	AE36	
17	VCCO_17	AH37	
17	VCCO_17	AG40	
18	VCCO_18	AF3	
18	VCCO_18	AJ4	
18	VCCO_18	AH7	
19	VCCO_19	H37	
19	VCCO_19	L38	

Table 2-10: **FF1760 Package—LX110, LX155, LX220, and LX330 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
19	VCCO_19	K41	
20	VCCO_20	M5	
20	VCCO_20	L8	
20	VCCO_20	P9	
21	VCCO_21	AJ34	
21	VCCO_21	AM35	
21	VCCO_21	AL38	
22	VCCO_22	AM5	
22	VCCO_22	AL8	
22	VCCO_22	AP9	
23	VCCO_23	E36	
23	VCCO_23	D39	
23	VCCO_23	G40	
24	VCCO_24	F3	
24	VCCO_24	J4	
24	VCCO_24	H7	
25	VCCO_25	AR36	
25	VCCO_25	AP39	
25	VCCO_25	AU40	
26	VCCO_26	AT3	
26	VCCO_26	AW4	
26	VCCO_26	AR6	
27	VCCO_27	C32	
27	VCCO_27	F33	
27	VCCO_27	B35	
28	VCCO_28	E6	
28	VCCO_28	D9	
28	VCCO_28	G10	
29	VCCO_29	AT33	
29	VCCO_29	AW34	
29	VCCO_29	AV37	
30	VCCO_30	AV7	
30	VCCO_30	BA8	

Table 2-10: **FF1760 Package—LX110, LX155, LX220, and LX330 *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
30	VCCO_30	AU10	
31	VCCO_31	H27	
31	VCCO_31	D29	
31	VCCO_31	G30	
32	VCCO_32	C12	
32	VCCO_32	F13	
32	VCCO_32	B15	
33	VCCO_33	BA28	
33	VCCO_33	AU30	
33	VCCO_33	AY31	
34	VCCO_34	AY11	
34	VCCO_34	AT13	
34	VCCO_34	AW14	

Notes:

1. Do not connect a single-ended clock to the N-side of the differential clock pair of pins, for example, IO_L3N_GC_3.
2. Do not connect a single-ended clock to the N-side of clock capable pins, for example, IO_L8N_CC_11.
3. RSVD pins must be tied to GND (logic 0).

XILINX®

Chapter 3

Pinout and SelectIO Bank Diagrams

Summary

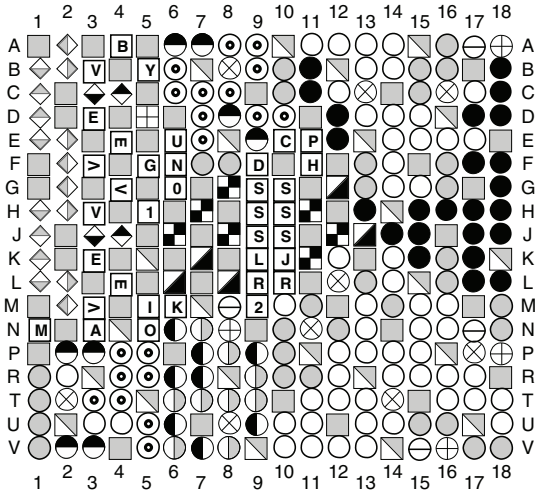
This chapter provides pinout diagrams for each Virtex®-5 package/device combination.

Multi-function I/O pins are represented in these diagrams by symbols for only one of the pins available functions, with precedence given to functionality in the following order:

- VREF, VRP, or VRN
- GC
- CC
- D0 – D31
- A0 – A25

For example, a pin description such as IO_L8P_CC_A3_D19_1 is represented with a CC symbol, a pin description such as IO_L14N_VREF_12 is represented with a VREF symbol, and a pin description such as IO_L2P_A15_D31_1 is represented with a D0–D31 symbol.

FF323 Package—LX20T and LX30T



User I/O Pins	Multi-Function Pins	Dedicated Pins		Other Pins		
IO_LXXY_#	VREF	C CCLK	P PROGRAM_B	GND	E MGTAVCC	MGTRXP
	VRN	B CS_B	U RDWR_B	R RSVD	m MGTAVCCPLL	MGTRXN
	VRP	N D_IN	K TCK	VBATT	V MGTAVTTRX	MGTTXN
	P_GC	D DONE	I TDI	VCCAUX	< MGTAVTTRXC	MGTTXP
	N_GC	A D_OUT_BUSY	O TDO	VCCINT	> MGTAVTTTX	
	CC	H HSWAPEN	M TMS	VCCO	MGTREFCLKP	
	D0 - D31	Y INIT	J DXP	n NC	MGTREFCLKN	
	A0 - A25	2 1 0 M2, M1, M0	L DXN	F FLOAT	G MGTRREF	
	SM	S AVDD_0, AVSS_0, VP_0, VN_0, VREFP_0, VREFN_0				

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Figure 3-1: **FF323—Package LX20T and LX30T Pinout Diagram**

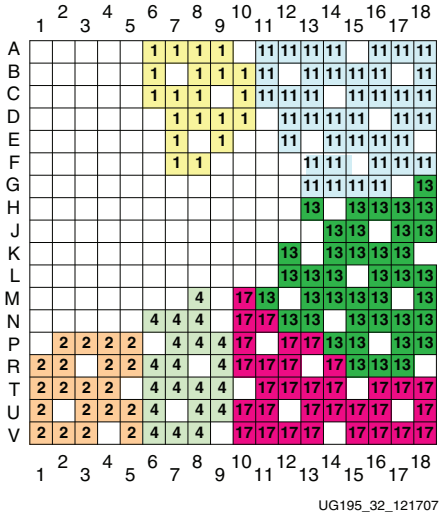

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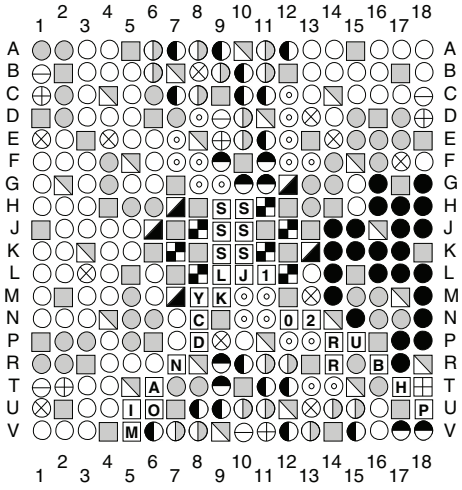
Figure 3-2: **FF323—Package LX20T and LX30T SelectIO Bank Diagram**

FF324 Package—LX30 and LX50



User I/O Pins	Multi-Function Pins	Dedicated Pins		Other Pins
IO_LXXY_#	VREF	C CCLK	P PROGRAM_B	GND
	VRN	B CS_B	U RDWR_B	R RSVD
	VRP	N D_IN	K TCK	VBATT
	P_GC	D DONE	I TDI	VCCAUX
	N_GC	A D_OUT_BUSY	O TDO	VCCINT
	CC	H HSWAPEN	M TMS	VCCO
	D0 - D31	Y INIT	J DXP	n NO CONNECT
	A0 - A25	2 1 0 M2, M1, M0	L DXN	
	SM	S AVDD_0, AVSS_0, VP_0, VN_0, VREFP_0, VREFN_0		

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Figure 3-3: **FF324 Package—LX30 and LX50 Pinout Diagram**

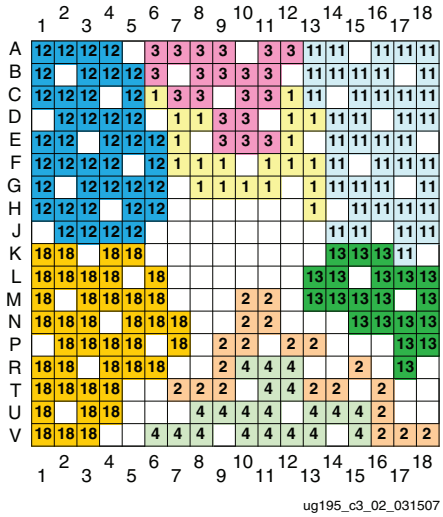

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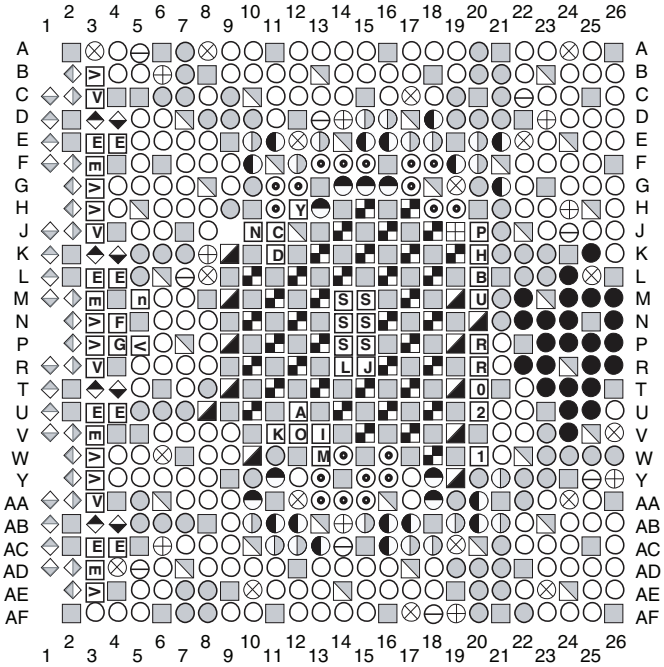
Figure 3-4: **FF324 Package—LX30 and LX50 SelectIO Bank Diagram**

FF665 Package—LX30T, FX30T, SX35T, LX50T, SX50T, and FX70T



User I/O Pins	Multi-Function Pins	Dedicated Pins		Other Pins		
IO_LXXY_#	VREF	CCLK	PROGRAM_B	GND	MGTAVCC	MGTRXP
	VRN	CS_B	RDWR_B	RSVD	MGTAVCCPLL	MGTRXN
	VRP	D_IN	TCK	VBATT	MGTAVTTRX	MGTTXN
	P_GC	DONE	TDI	VCCAUX	MGTAVTTRXC	MGTTXP
	N_GC	D_OUT_BUSY	TDO	VCCINT	MGTAVTTTX	
	CC	HSWAPEN	TMS	VCCO	MGTREFCLKP	
	D0 - D31	INIT	DXP	NC	MGTREFCLKN	
	A0 - A25	M2, M1, M0	DXN	FLOAT	MGTRREF	
	SM	AVDD_0, AVSS_0, VP_0, VN_0, VREFP_0, VREFN_0				

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Figure 3-5: **FF665 Package—LX30T, FX30T, SX35T, LX50T, SX50T, and FX70T Pinout Diagram**

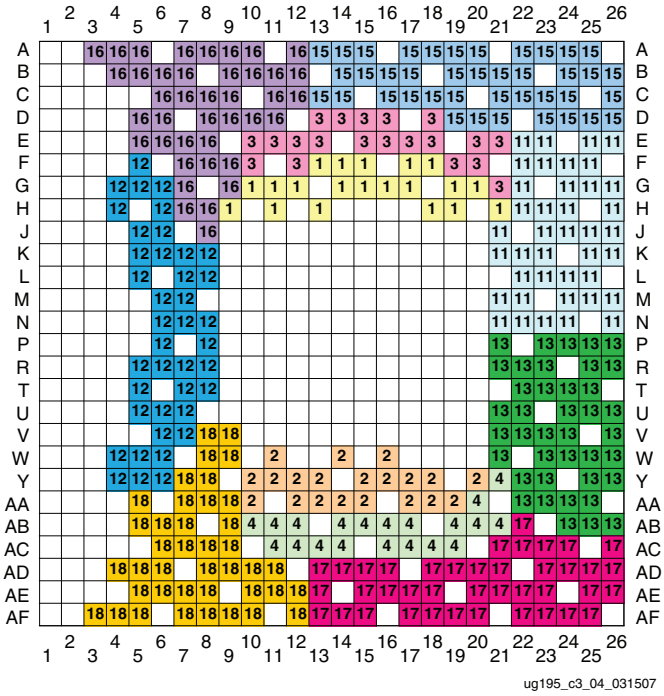
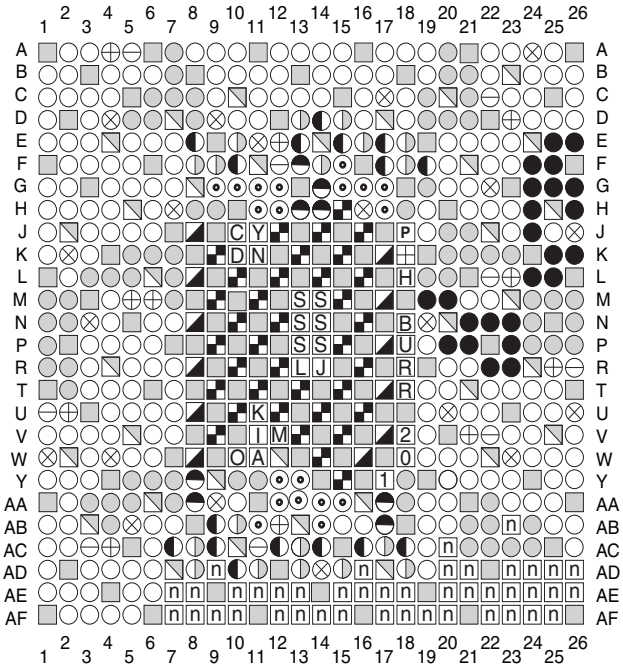


Figure 3-6: **FF665 Package—LX30T, FX30T, SX35T, LX50T, SX50T, and FX70T SelectIO Bank Diagram**

FF676 Package—LX30



User I/O Pins	Multi-Function Pins	Dedicated Pins		Other Pins
○ IO_LXXY_#	⊗ VREF	C CCLK	P PROGRAM_B	GND
	⊕ VRN	B CS_B	U RDWR_B	R RSVD
	⊖ VRP	N D_IN	K TCK	⊞ VBATT
	◍ P_GC	D DONE	I TDI	◪ VCCAUX
	◐ N_GC	A D_OUT_BUSY	O TDO	▪ VCCINT
	◌ CC	H HSWAPEN	M TMS	▧ VCCO
	⊙ D0 - D31	Y INIT	J DXP	n NO CONNECT
	◓ A0 - A25	2 1 0 M2, M1, M0	L DXN	
	● SM	S AVDD_0, AVSS_0, VP_0, VN_0, VREFP_0, VREFN_0		

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Figure 3-7: **FF676 Package—LX30 Pinout Diagram**

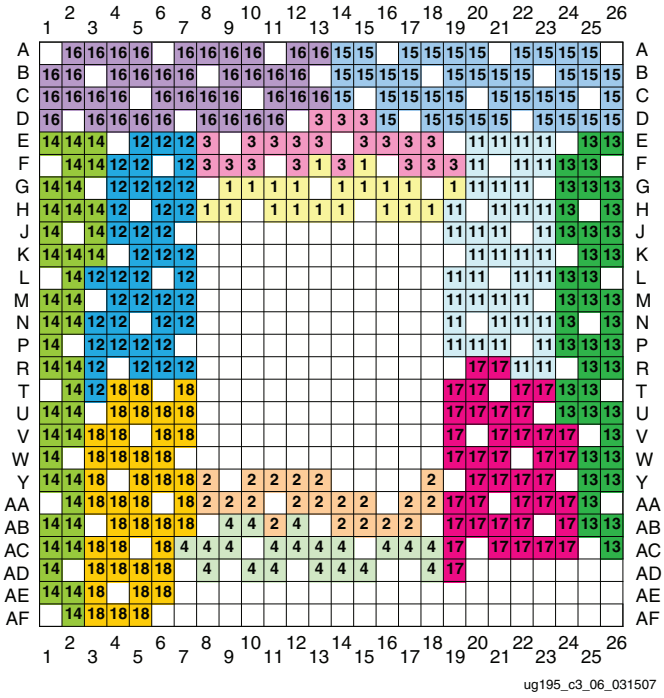
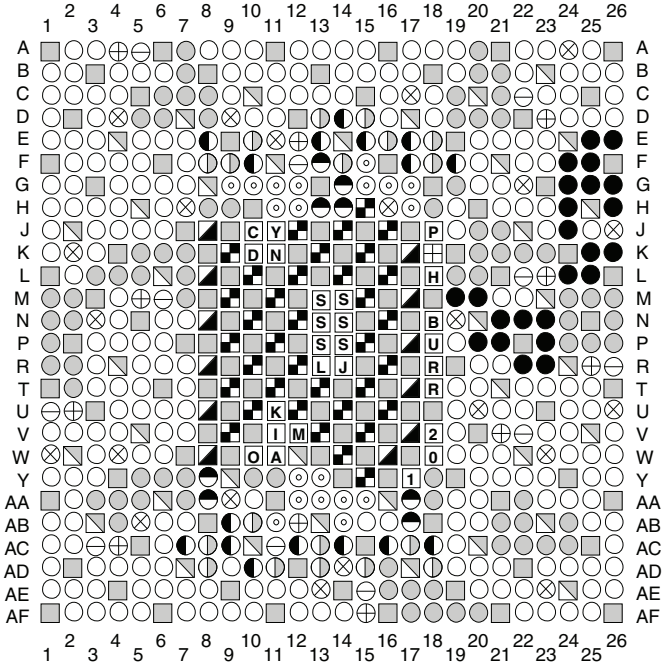


Figure 3-8: **FF676 Package—LX30 SelectIO Bank Diagram**

FF676 Package—LX50, LX85, and LX110



User I/O Pins	Multi-Function Pins	Dedicated Pins		Other Pins
○ IO_LXXY_#	⊗ VREF	C CCLK	P PROGRAM_B	GND
	⊕ VRN	B CS_B	U RDWR_B	R RSVD
	⊖ VRP	N D_IN	K TCK	VBATT
	◑ P_GC	D DONE	I TDI	VCCAUX
	◐ N_GC	A D_OUT_BUSY	O TDO	VCCINT
	○ CC	H HSWAPEN	M TMS	VCCO
	⊙ D0 - D31	Y INIT	J DXP	n NO CONNECT
	◓ A0 - A25	2 1 0 M2, M1, M0	L DXN	
	● SM	S AVDD_0, AVSS_0, VP_0, VN_0, VREFP_0, VREFN_0		

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Figure 3-9: **FF676 Package—LX50, LX85, and LX110 Pinout Diagram**

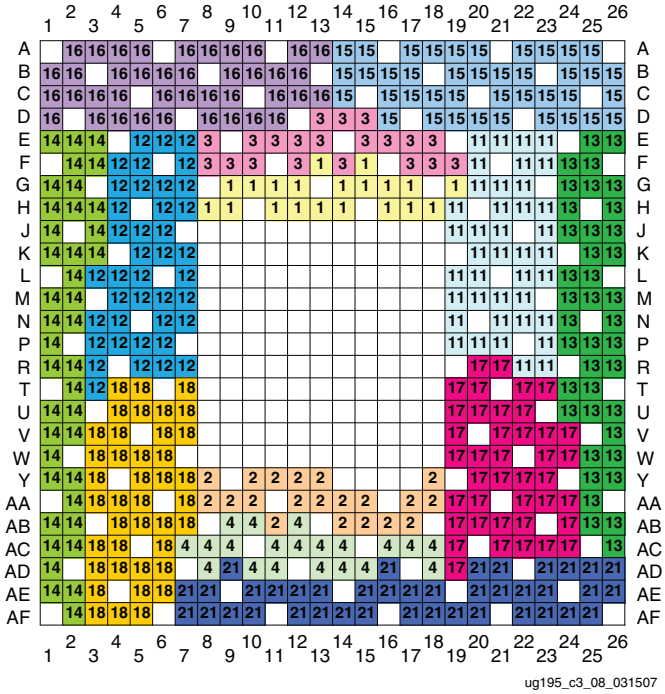
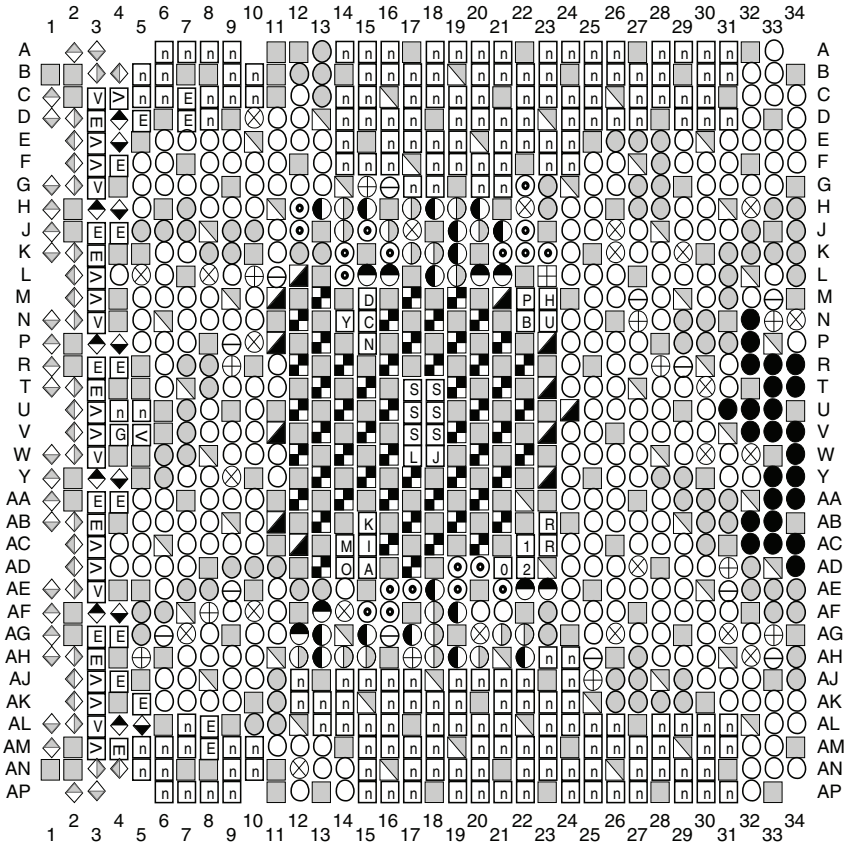


Figure 3-10: **FF676 Package—LX50, LX85, and LX110 SelectIO Bank Diagram**

FF1136 Package—LX50T, SX50T, and LX85T



User I/O Pins	Multi-Function Pins	Dedicated Pins		Other Pins		
IO_LXXY_#	VREF	CCLK	PROGRAM_B	GND	MGTAVCC	MGTRXP
	VRN	CS_B	RDWR_B	RSVD	MGTAVCCPLL	MGTRXN
	VRP	D_IN	TCK	VBATT	MGTAVTTRX	MGTTXN
	P_GC	DONE	TDI	VCCAUX	MGTAVTTRXC	MGTTXP
	N_GC	D_OUT_BUSY	TDO	VCCINT	MGTAVTTTX	
	CC	HSWAPEN	TMS	VCCO	MGTREFCLKP	
	D0 - D31	INIT	DXP	NC	MGTREFCLKN	
	A0 - A25	M2, M1, M0	DXN	FLOAT	MGTRREF	
	SM	AVDD_0, AVSS_0, VP_0, VN_0, VREFP_0, VREFN_0				

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Figure 3-11: **FF1136 Package—LX50T, SX50T, and LX85T Pinout Diagram**

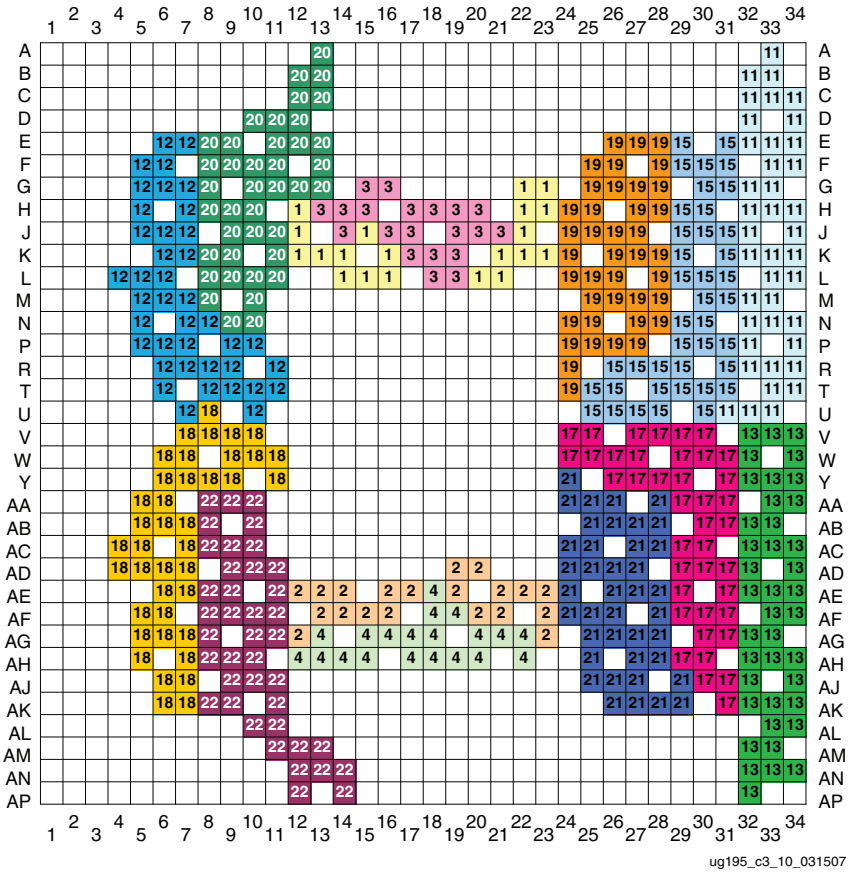
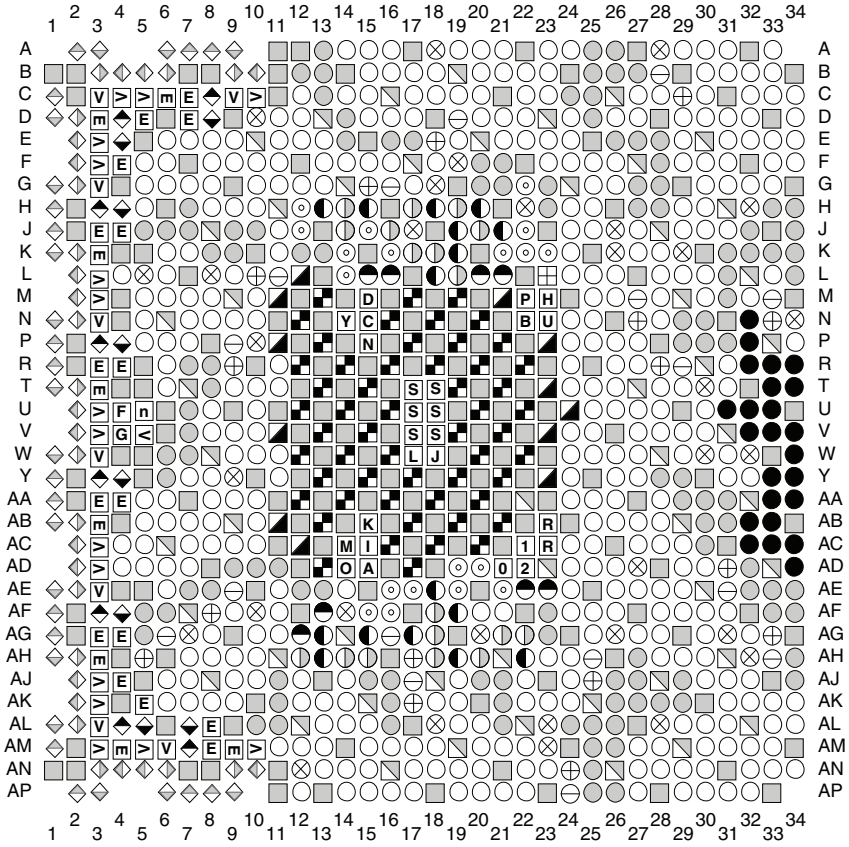


Figure 3-12: **FF1136 Package—LX50T, SX50T, and LX85T SelectIO Bank Diagram**

FF1136 Package—FX70T, SX95T, FX100T, LX110T, and LX155T



User I/O Pins	Multi-Function Pins	Dedicated Pins		Other Pins		
IO_LXXY_#	VREF	CCLK	PROGRAM_B	GND	MGTAVCC	MGTRXP
	VRN	CS_B	RDWR_B	RSVD	MGTAVCCPLL	MGTRXN
	VRP	D_IN	TCK	VBATT	MGTAVTTRX	MGTTXN
	P_GC	DONE	TDI	VCCAUX	MGTAVTTRXC	MGTTXP
	N_GC	D_OUT_BUSY	TDO	VCCINT	MGTAVTTTX	
	CC	HSWAPEN	TMS	VCCO	MGTREFCLKP	
	D0 - D31	INIT	DXP	NC	MGTREFCLKN	
	A0 - A25	M2, M1, M0	DXN	FLOAT	MGTRREF	
	SM	AVDD_0, AVSS_0, VP_0, VN_0, VREFP_0, VREFN_0				

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Figure 3-13: **FF1136 Package—FX70T, SX95T, FX100T, LX110T, and LX155T Pinout Diagram**

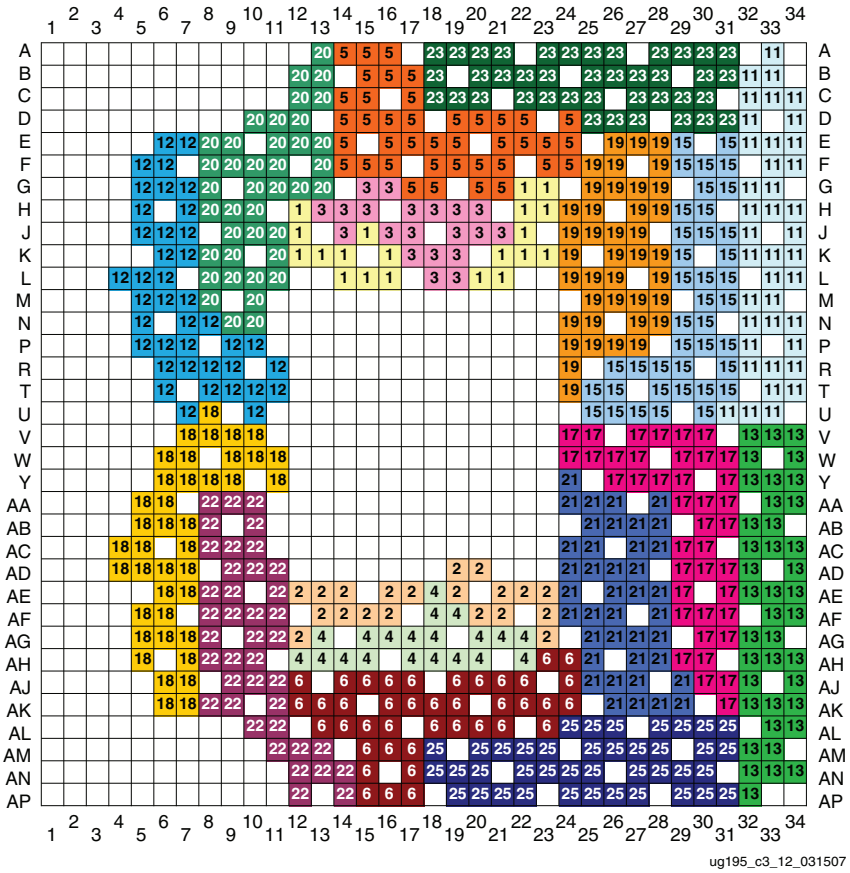
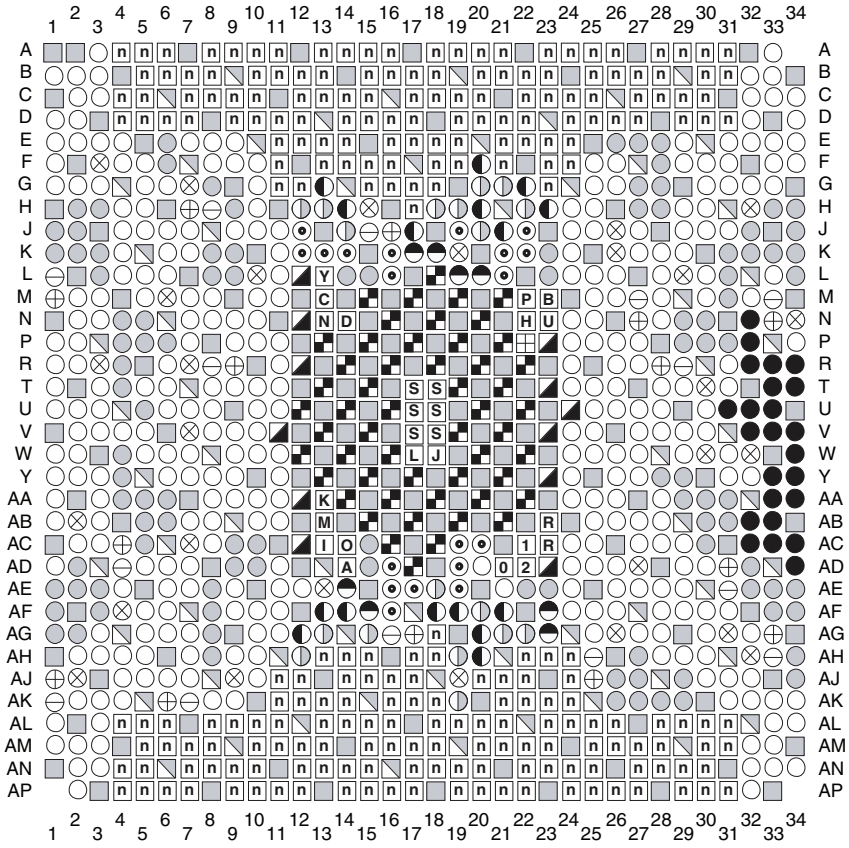


Figure 3-14: **FF1136 Package—FX70T, SX95T, FX100T, LX110T, and LX155T SelectIO Bank Diagram**

FF1153 Package—LX50 and LX85



User I/O Pins	Multi-Function Pins	Dedicated Pins		Other Pins
IO_LXXY_#	VREF	C CCLK	P PROGRAM_B	GND
	VRN	B CS_B	U RDWR_B	R RSVD
	VRP	N D_IN	K TCK	VBATT
	P_GC	D DONE	I TDI	VCCAUX
	N_GC	A D_OUT_BUSY	O TDO	VCCINT
	CC	H HSWAPEN	M TMS	VCCO
	D0 - D31	Y INIT	J DXP	n NO CONNECT
	A0 - A25	2 1 0 M2, M1, M0	L DXN	
	SM	S AVDD_0, AVSS_0, VP_0, VN_0, VREFP_0, VREFN_0		

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Figure 3-15: **FF1153 Package—LX50 and LX85 Pinout Diagram**

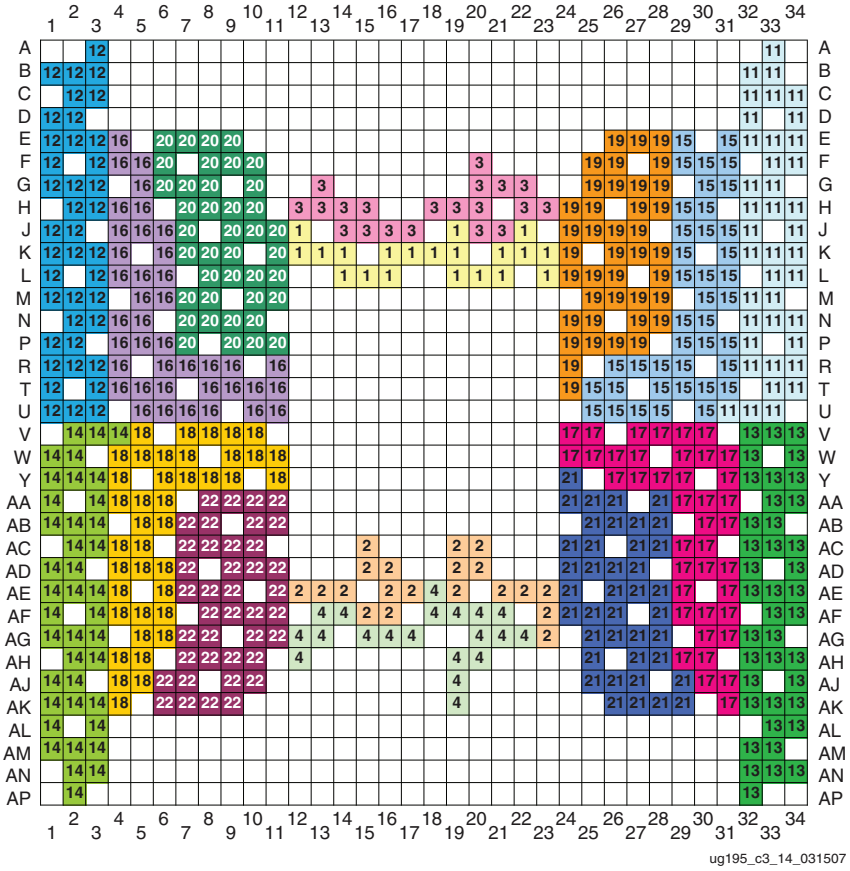
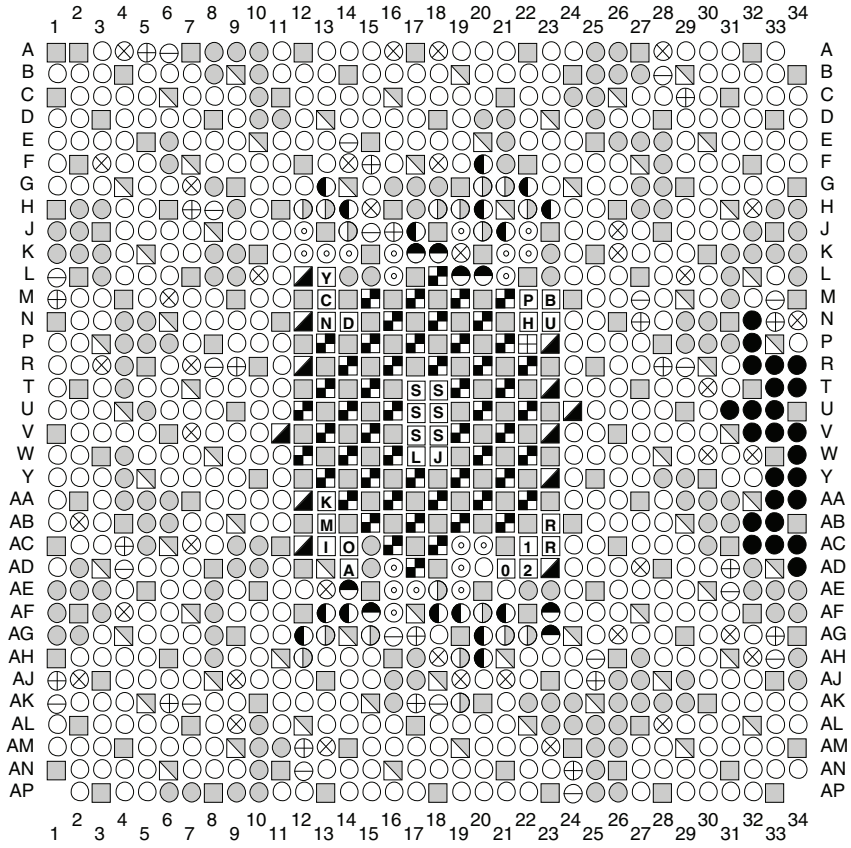


Figure 3-16: **FF1153 Package—LX50 and LX85 SelectIO Bank Diagram**

FF1153 Package—LX110 and LX155



User I/O Pins	Multi-Function Pins	Dedicated Pins		Other Pins
IO_LXXY_#	VREF	C CCLK	P PROGRAM_B	GND
	VRN	B CS_B	U RDWR_B	R RSVD
	VRP	N D_IN	K TCK	VBATT
	P_GC	D DONE	I TDI	VCCAUX
	N_GC	A D_OUT_BUSY	O TDO	VCCINT
	CC	H HSWAPEN	M TMS	VCCO
	D0 - D31	Y INIT	J DXP	n NO CONNECT
	A0 - A25	2 1 0 M2, M1, M0	L DXN	
	SM	S AVDD_0, AVSS_0, VP_0, VN_0, VREFP_0, VREFN_0		

ug195_c3_15_080607

Figure 3-17: **FF1153 Package—LX110 and LX155 Pinout Diagram**

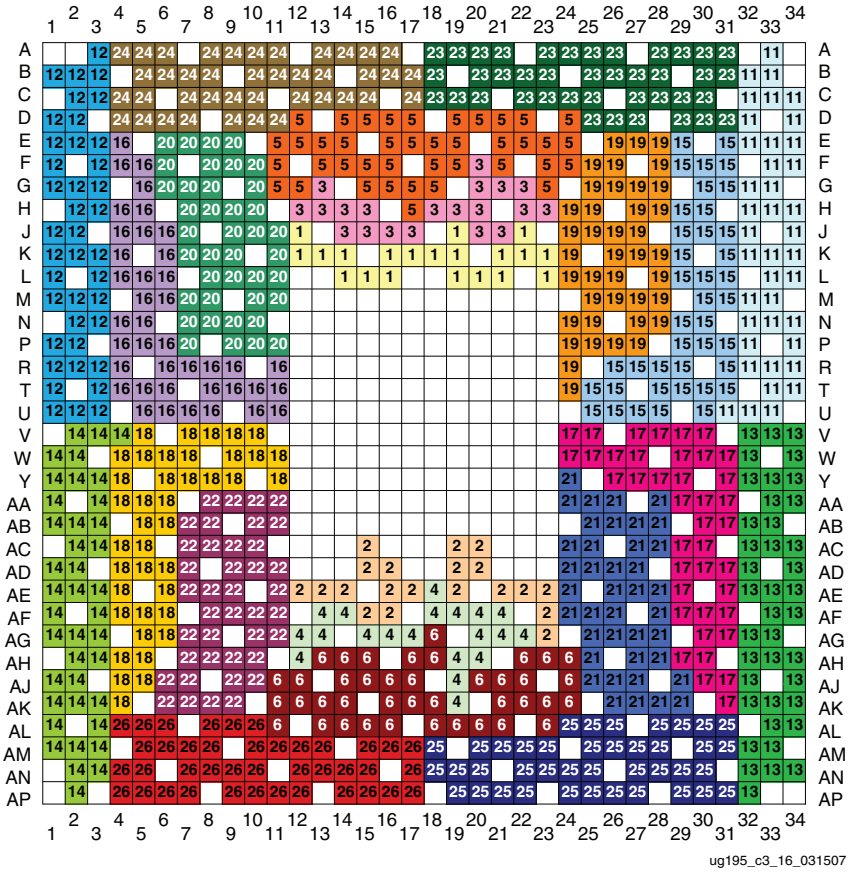
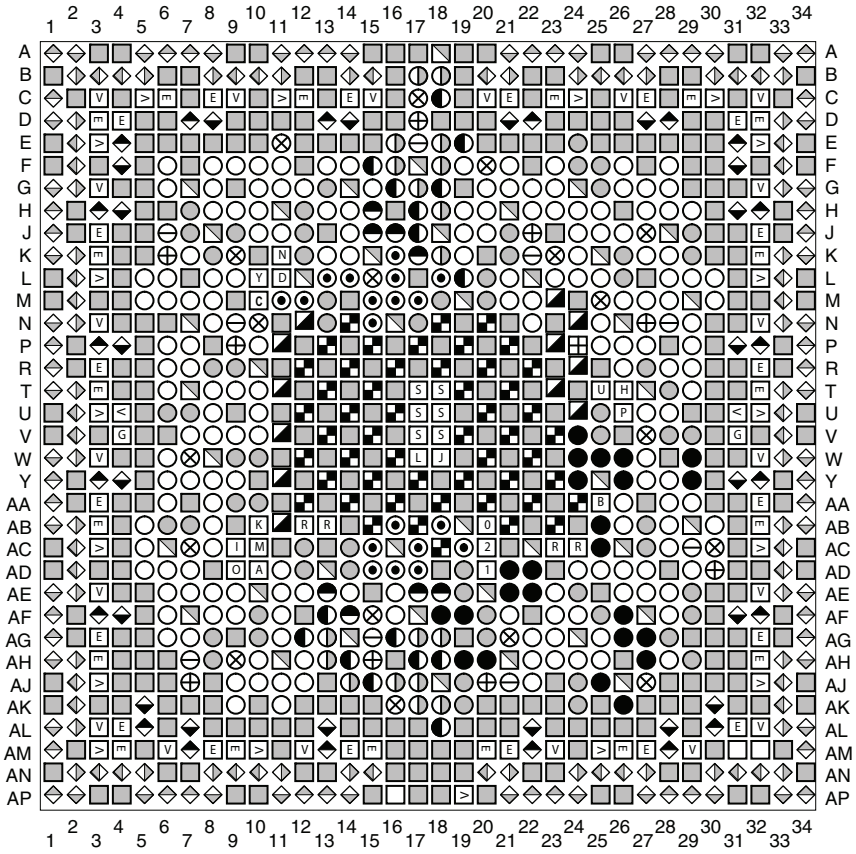


Figure 3-18: **FF1153 Package—LX110 and LX155 SelectIO Bank Diagram**

FF1156 Package—TX150T



User I/O Pins	Multi-Function Pins	Dedicated Pins		Other Pins		
IO_LXXY_#	VREF	CCLK	PROGRAM_B	GND	MGTAVCC	MGTRXP
	VRN	CS_B	RDWR_B	RSVD	MGTAVCCPLL	MGTRXN
	VRP	D_IN	TCK	VBATT	MGTAVTTRX	MGTTXN
	P_GC	DONE	TDI	VCCAUX	MGTAVTTRXC	MGTTXP
	N_GC	D_OUT_BUSY	TDO	VCCINT	MGTAVTTTX	
	CC	HSWAPEN	TMS	VCCO	MGTREFCLKP	
	D0 - D31	INIT	DXP	NC	MGTREFCLKN	
	A0 - A25	M2, M1, M0	DXN	FLOAT	MGTRREF	
	SM	AVDD_0, AVSS_0, VP_0, VN_0, VREFP_0, VREFN_0				

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Figure 3-19: **FF1156 Package—TX150T Pinout Diagram**

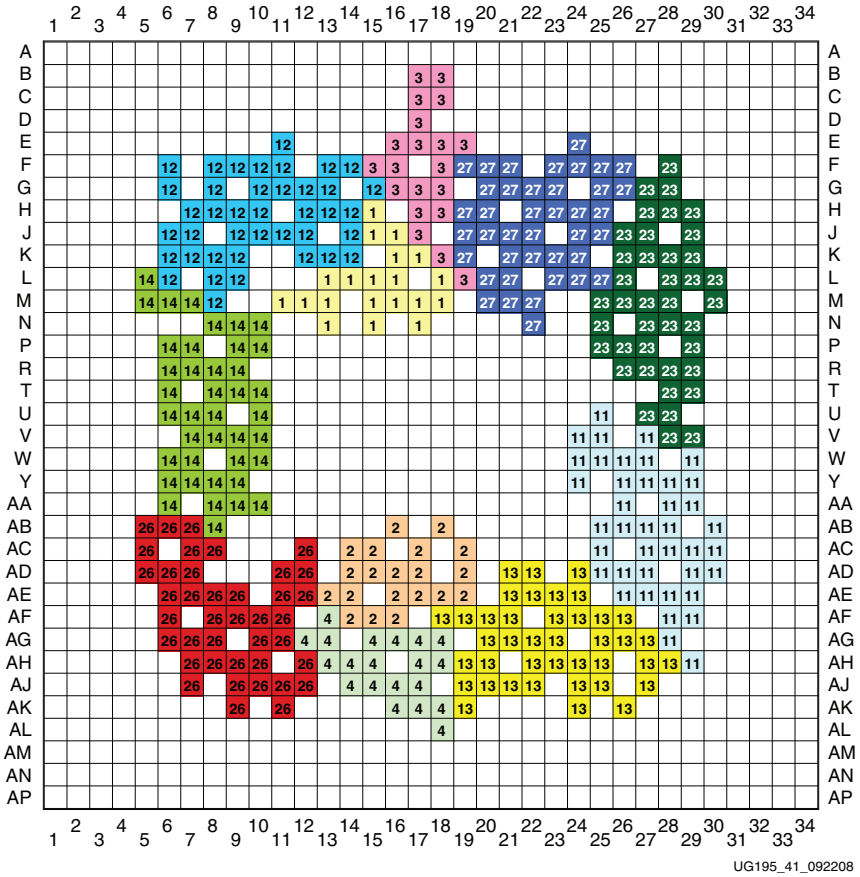
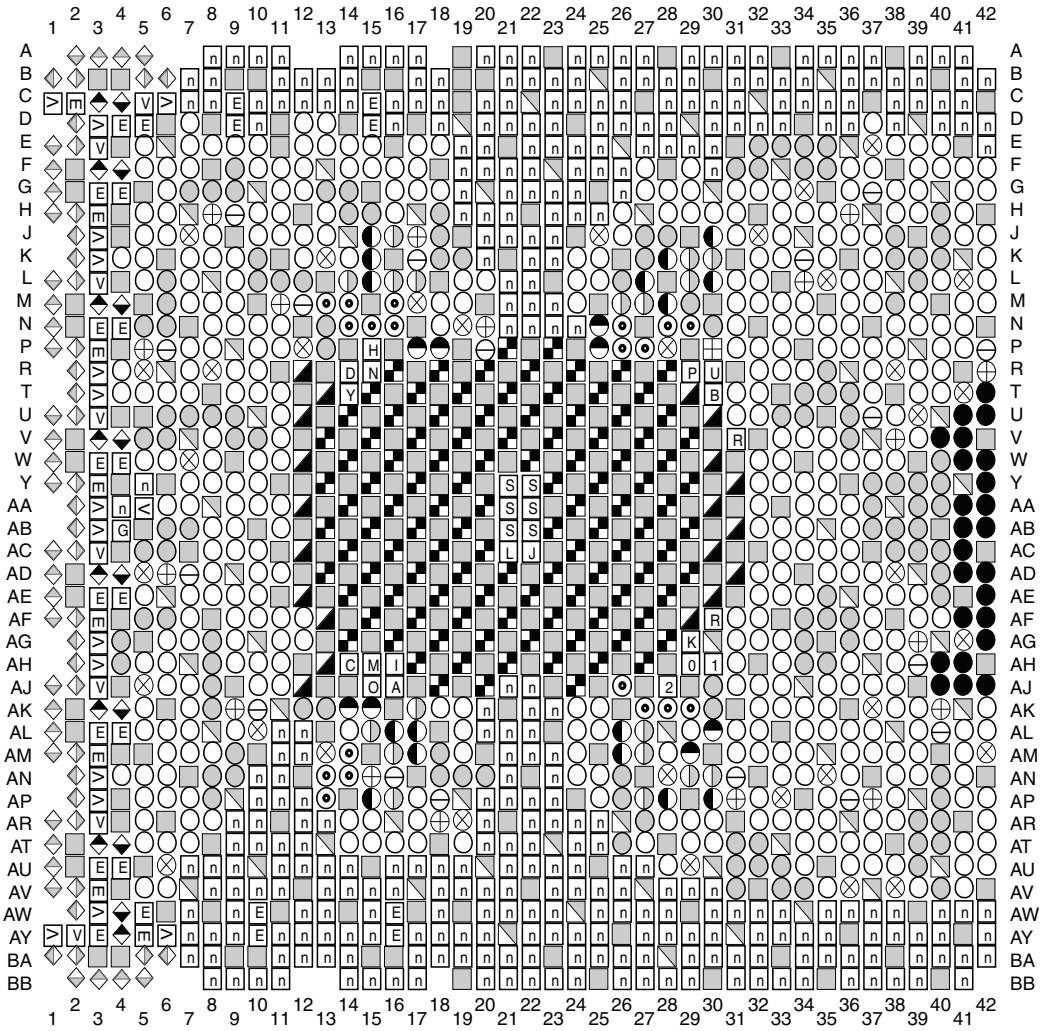


Figure 3-20: **FF1156 Package—TX150T SelectIO Bank Diagram**

FF1738 Package—FX100T, LX110T, LX155T, and LX220T



User I/O Pins	Multi-Function Pins	Dedicated Pins		Other Pins		
IO_LXXY_#	VREF	CCLK	PROGRAM_B	GND	MGTAVCC	MGTRXP
	VRN	CS_B	RDWR_B	RSVD	MGTAVCCPLL	MGTRXN
	VRP	D_IN	TCK	VBATT	MGTAVTTRX	MGTTXN
	P_GC	DONE	TDI	VCCAUX	MGTAVTTRXC	MGTTXP
	N_GC	D_OUT_BUSY	TDO	VCCINT	MGTAVTTTX	
	CC	HSWAPEN	TMS	VCCO	MGTREFCLKP	
	D0 - D31	INIT	DXP	NC	MGTREFCLKN	
	A0 - A25	M2, M1, M0	DXN	FLOAT	MGTRREF	
	SM	AVDD_0, AVSS_0, VP_0, VN_0, VREFP_0, VREFN_0				

ug195_c3_17_120707

Figure 3-21: **FF1738 Package—FX100T, LX110T, LX155T, and LX220T Pinout Diagram**

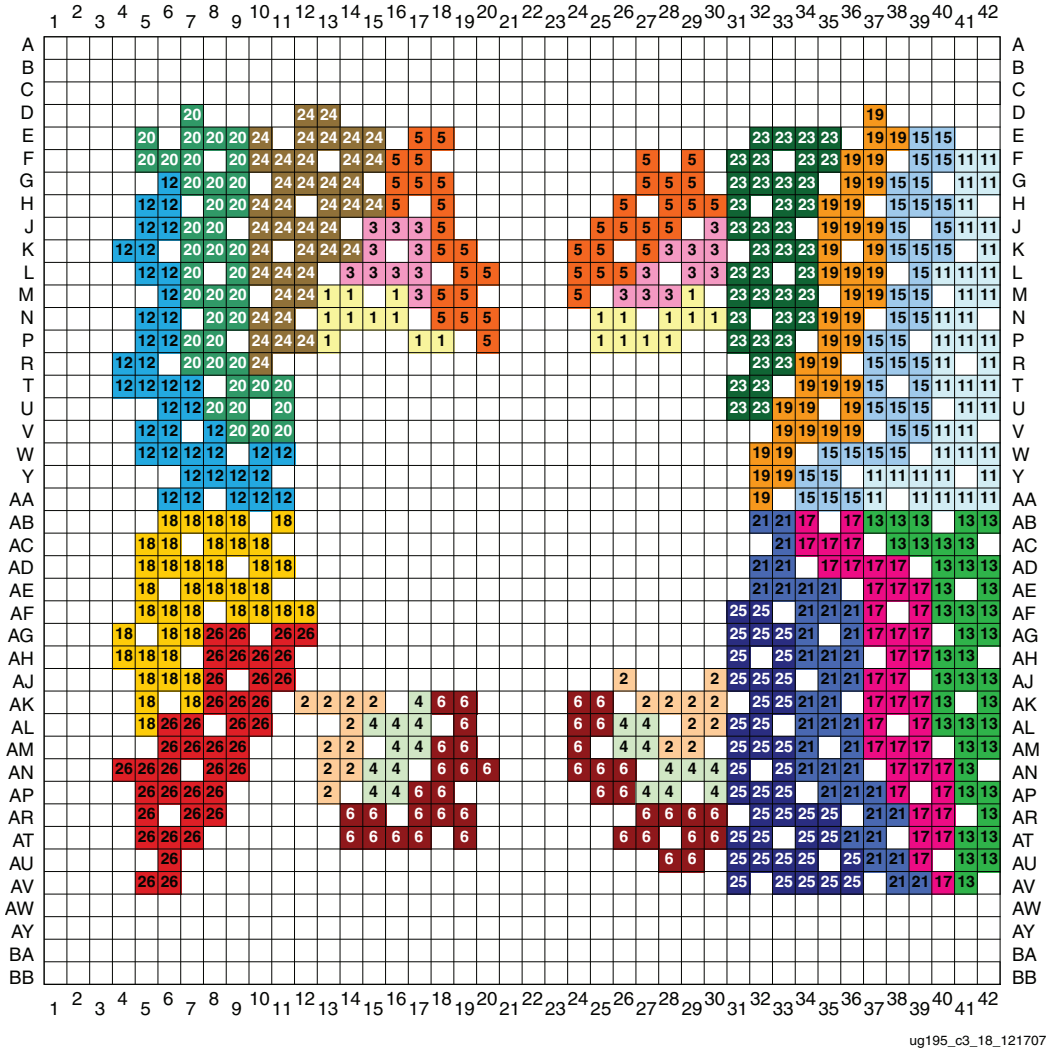
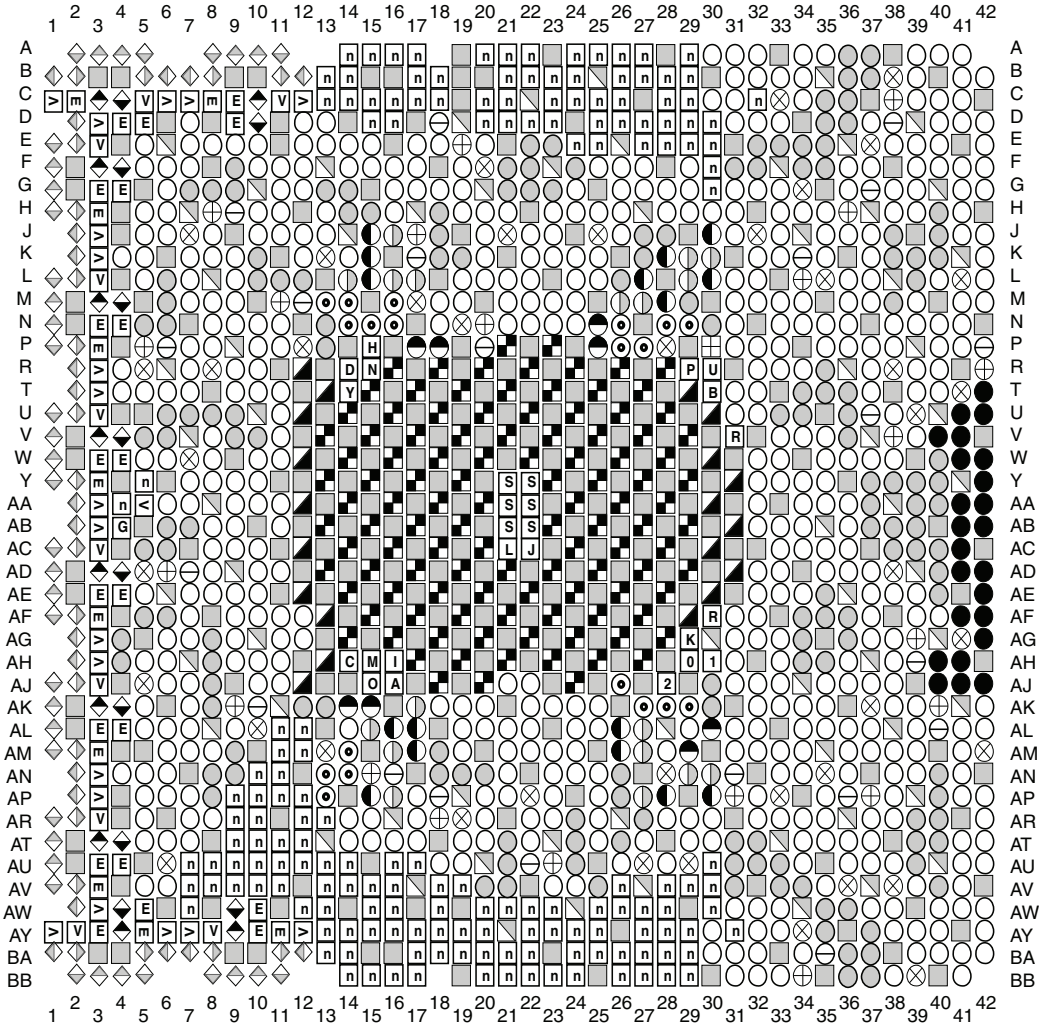


Figure 3-22: **FF1738 Package—FX100T, LX110T, LX155T, and LX220T SelectIO Bank Diagram**

FF1738 Package—FX130T



User I/O Pins	Multi-Function Pins	Dedicated Pins		Other Pins		
IO_LXXY_#	VREF	CCLK	PROGRAM_B	GND	MGTAVCC	MGTRXP
	VRN	CS_B	RDWR_B	RSVD	MGTAVCCPLL	MGTRXN
	VRP	D_IN	TCK	VBATT	MGTAVTTRX	MGTTXN
	P_GC	DONE	TDI	VCCAUX	MGTAVTTRXC	MGTTXP
	N_GC	D_OUT_BUSY	TDO	VCCINT	MGTAVTTTX	
	CC	HSWAPEN	TMS	VCCO	MGTREFCLKP	
	D0 - D31	INIT	DXP	NC	MGTREFCLKN	
	A0 - A25	M2, M1, M0	DXN	FLOAT	MGTRREF	
	SM	AVDD_0, AVSS_0, VP_0, VN_0, VREFP_0, VREFN_0				

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Figure 3-23: **FF1738 Package—FX130T Pinout Diagram**

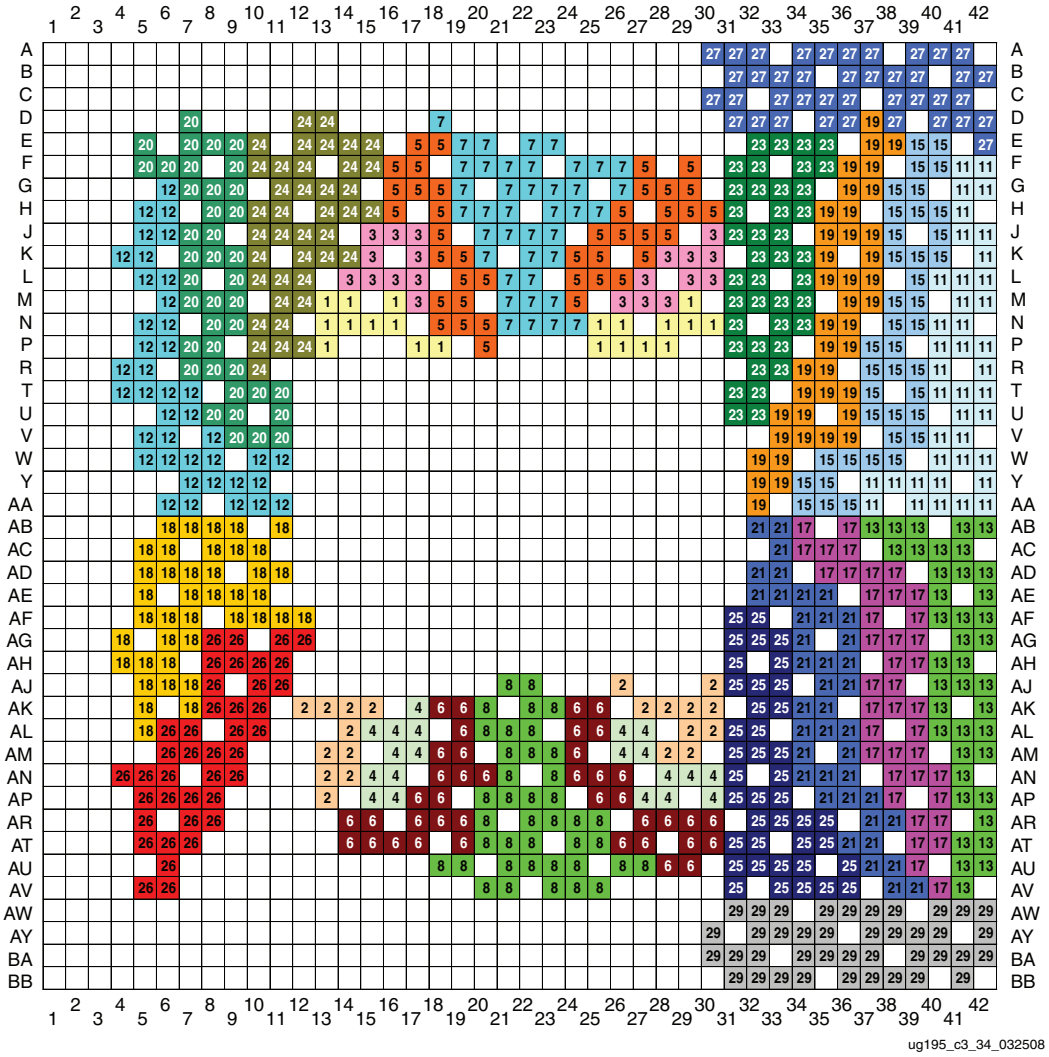
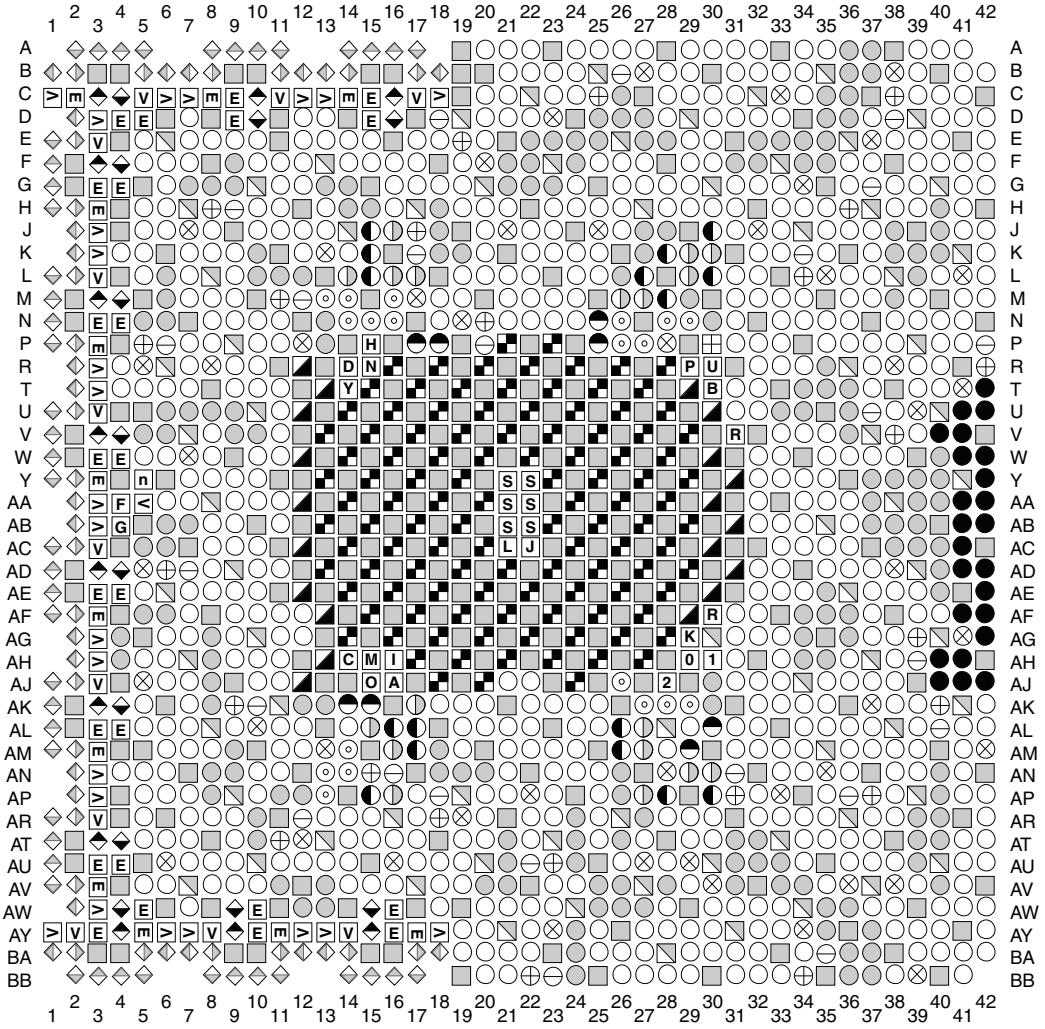


Figure 3-24: **FF1738 Package—FX130T SelectIO Bank Diagram**

FF1738 Package—FX200T, SX240T, and LX330T



User I/O Pins	Multi-Function Pins	Dedicated Pins		Other Pins		
○ IO_LXXY_#	⊗ VREF	C CCLK	P PROGRAM_B	GND	E MGTAVCC	MGTRXP
	⊕ VRN	B CS_B	U RDWR_B	R RSVD	m MGTAVCCPLL	MGTRXN
	⊖ VRP	N D_IN	K TCK	VBATT	V MGTAVTTRX	MGTTXN
	P_GC	D DONE	I TDI	VCCAUX	< MGTAVTTRXC	MGTTXP
	N_GC	A D_OUT_BUSY	O TDO	VCCINT	> MGTAVTTTX	
	CC	H HSWAPEN	M TMS	VCCO	MGTREFCLKP	
	D0 - D31	Y INIT	J DXP	n NC	MGTREFCLKN	
	A0 - A25	2 1 0 M2, M1, M0	L DXN	F FLOAT	G MGTRREF	
	SM	S AVDD_0, AVSS_0, VP_0, VN_0, VREFP_0, VREFN_0				

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Figure 3-25: **FF1738 Package—FX200T, SX240T, and LX330T Pinout Diagram**

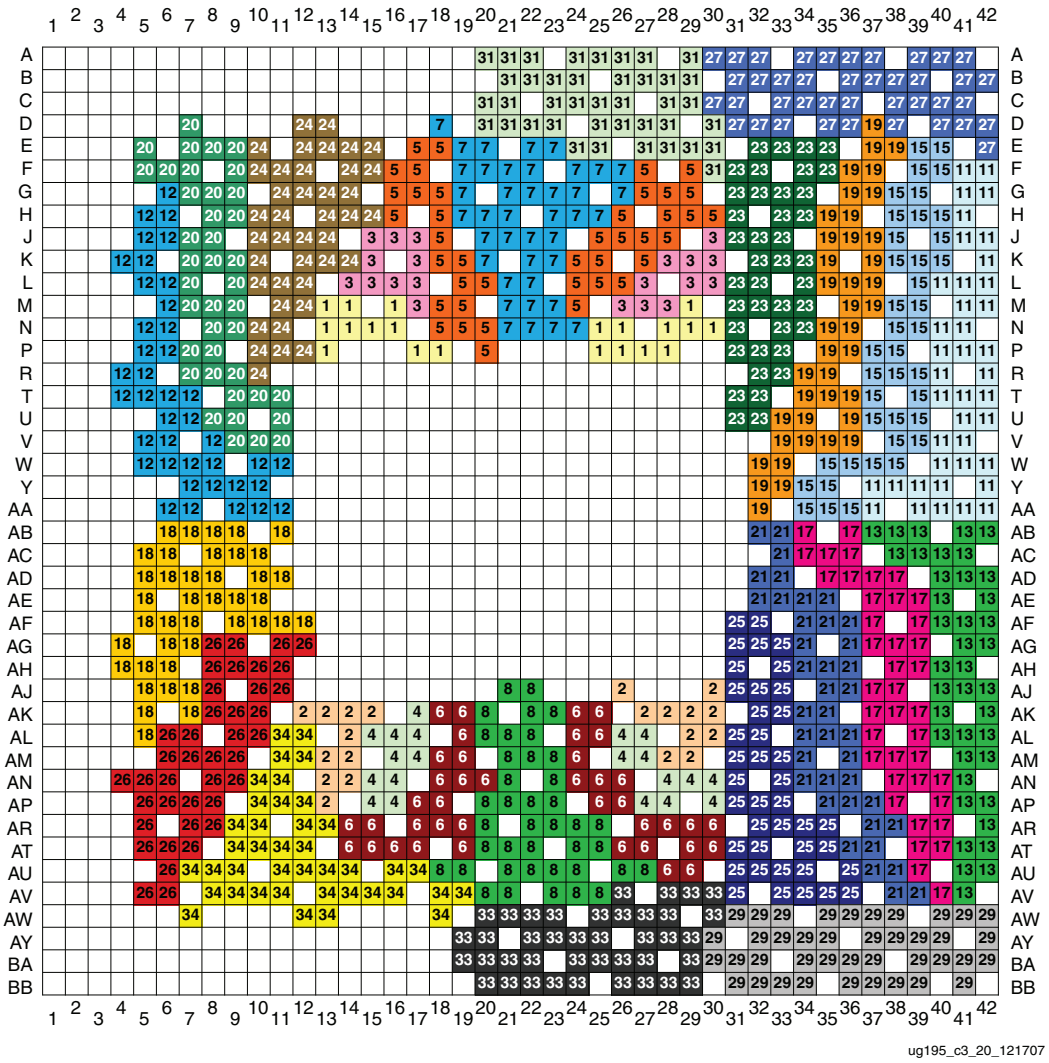
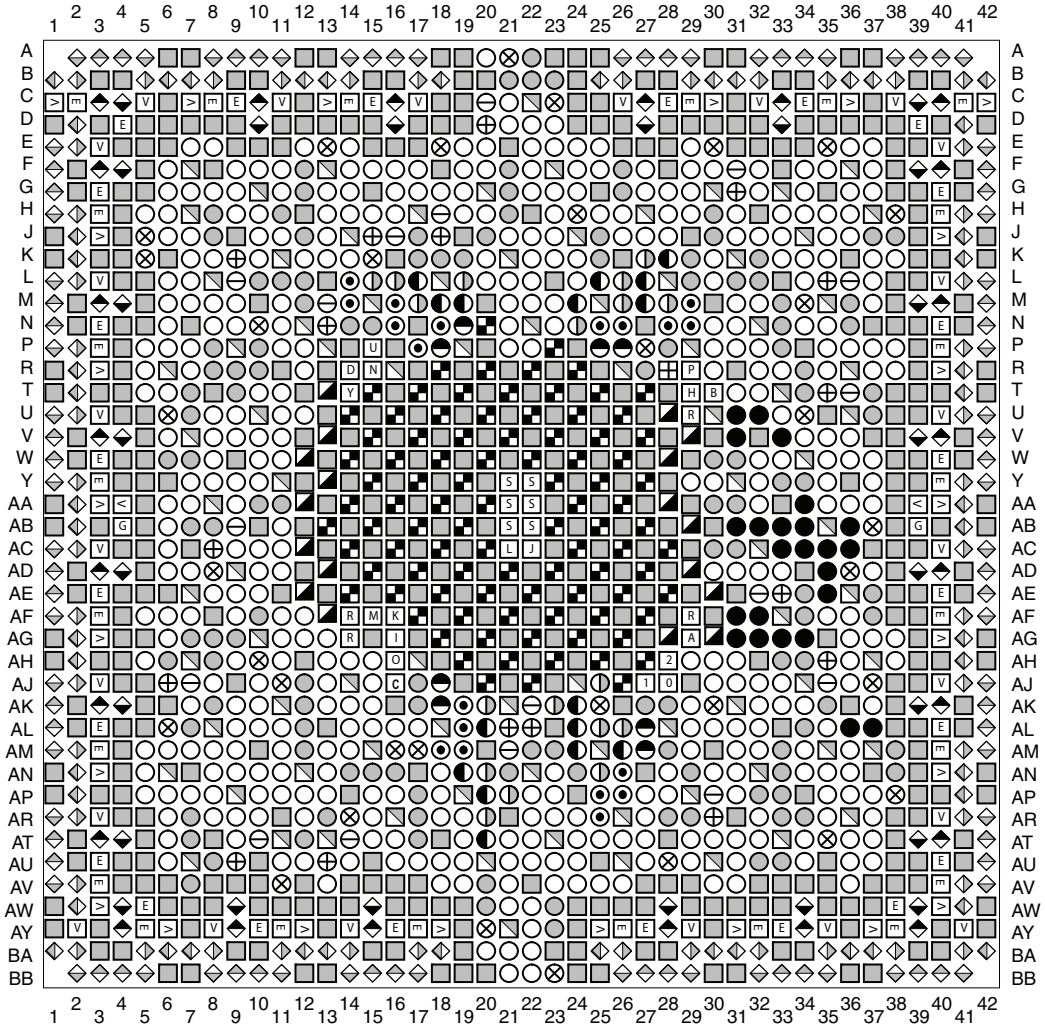


Figure 3-26: **FF1738 Package—FX200T, SX240T, and LX330T SelectIO Bank Diagram**

FF1759 Package—TX150T and TX240T



User I/O Pins	Multi-Function Pins	Dedicated Pins		Other Pins		
IO_LXXY_#	VREF	CCLK	PROGRAM_B	GND	MGTAVCC	MGTRXP
	VRN	CS_B	RDWR_B	RSVD	MGTAVCCPLL	MGTRXN
	VRP	D_IN	TCK	VBATT	MGTAVTTRX	MGTTXN
	P_GC	DONE	TDI	VCCAUX	MGTAVTTRXC	MGTTXP
	N_GC	D_OUT_BUSY	TDO	VCCINT	MGTAVTTTX	
	CC	HSWAPEN	TMS	VCCO	MGTREFCLKP	
	D0 - D31	INIT	DXP	NC	MGTREFCLKN	
	A0 - A25	M2, M1, M0	DXN	FLOAT	MGTRREF	
	SM	AVDD_0, AVSS_0, VP_0, VN_0, VREFP_0, VREFN_0				

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Figure 3-27: **FF1759 Package—TX150T and TX240T Pinout Diagram**

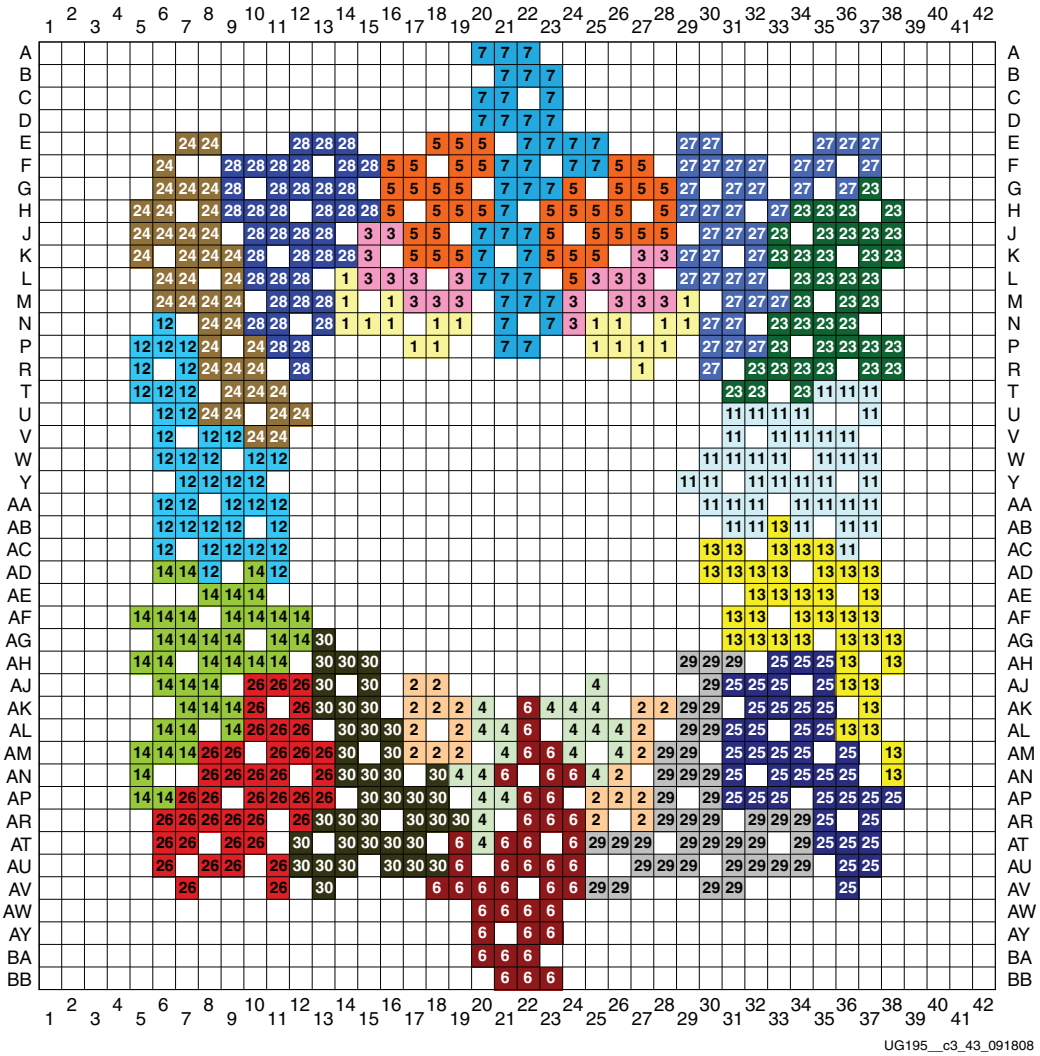
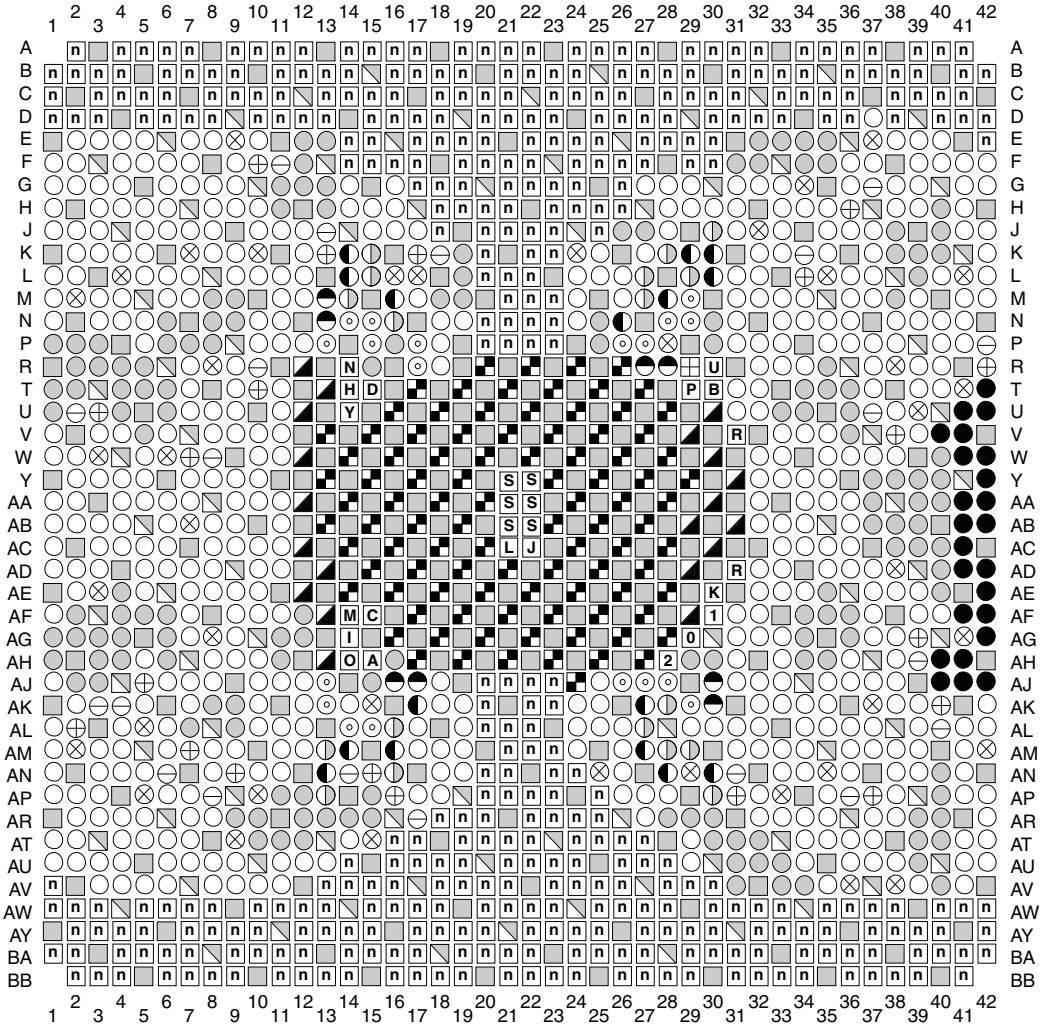


Figure 3-28: **FF1759 Package—TX150T and TX240T SelectIO Bank Diagram**

FF1760 Package—LX110, LX155, and LX220



User I/O Pins	Multi-Function Pins	Dedicated Pins		Other Pins
○ IO_LXXY_#	⊗ VREF	C CCLK	P PROGRAM_B	GND
	⊕ VRN	B CS_B	U RDWR_B	R RSVD
	⊖ VRP	N D_IN	K TCK	⊞ VBATT
	◑ P_GC	D DONE	I TDI	◪ VCCAUX
	◐ N_GC	A D_OUT_BUSY	O TDO	◩ VCCINT
	● CC	H HSWAPEN	M TMS	◪ VCCO
	⊙ D0 - D31	Y INIT	J DXP	n NO CONNECT
	◓ A0 - A25	2 1 0 M2, M1, M0	L DXN	
	● SM	S AVDD_0, AVSS_0, VP_0, VN_0, VREFP_0, VREFN_0		

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Figure 3-29: **FF1760 Package—LX110, LX155, and LX220 Pinout Diagram**

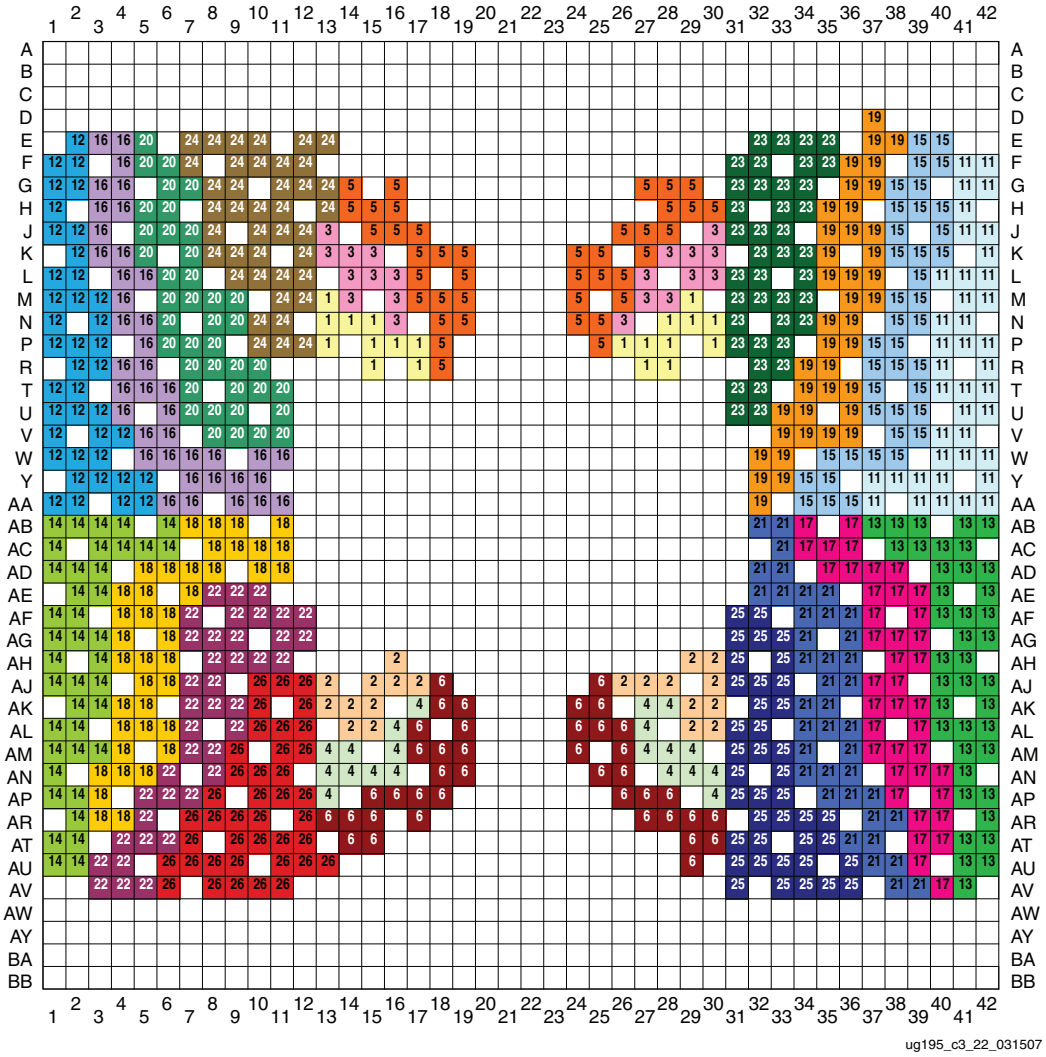
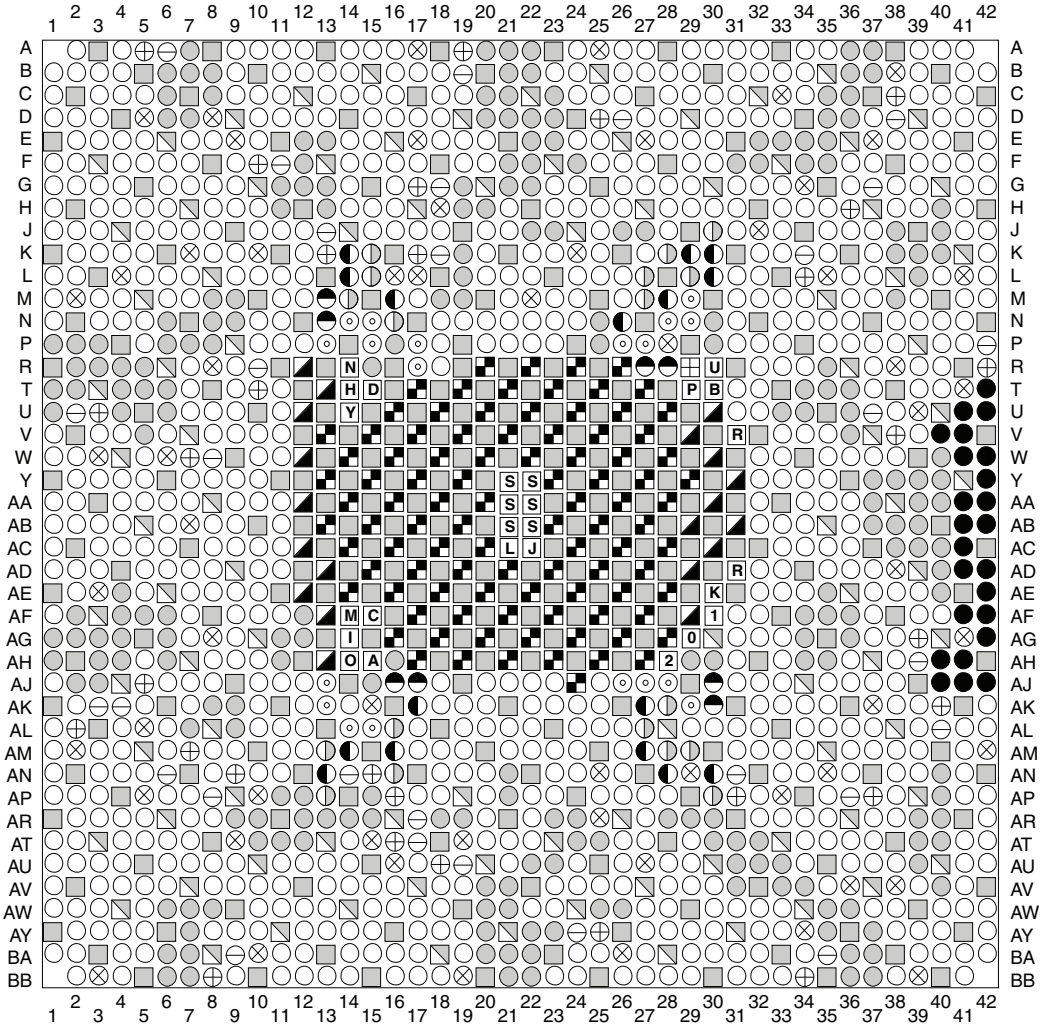


Figure 3-30: **FF1760 Package—LX110, LX155, and LX220 SelectIO Bank Diagram**

FF1760 Package—LX330



User I/O Pins	Multi-Function Pins	Dedicated Pins		Other Pins
○ IO_LXXY_#	⊗ VREF	C CCLK	P PROGRAM_B	GND
	⊕ VRN	B CS_B	U RDWR_B	R RSVD
	⊖ VRP	N D_IN	K TCK	VBATT
	◑ P_GC	D DONE	I TDI	VCCAUX
	◐ N_GC	A D_OUT_BUSY	O TDO	VCCINT
	○ CC	H HSWAPEN	M TMS	VCCO
	⊙ D0 - D31	Y INIT	J DXP	n NO CONNECT
	◓ A0 - A25	2 1 0 M2, M1, M0	L DXN	
	● SM	S AVDD_0, AVSS_0, VP_0, VN_0, VREFP_0, VREFN_0		

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Figure 3-31: **FF1760 Package—LX330 Pinout Diagram**

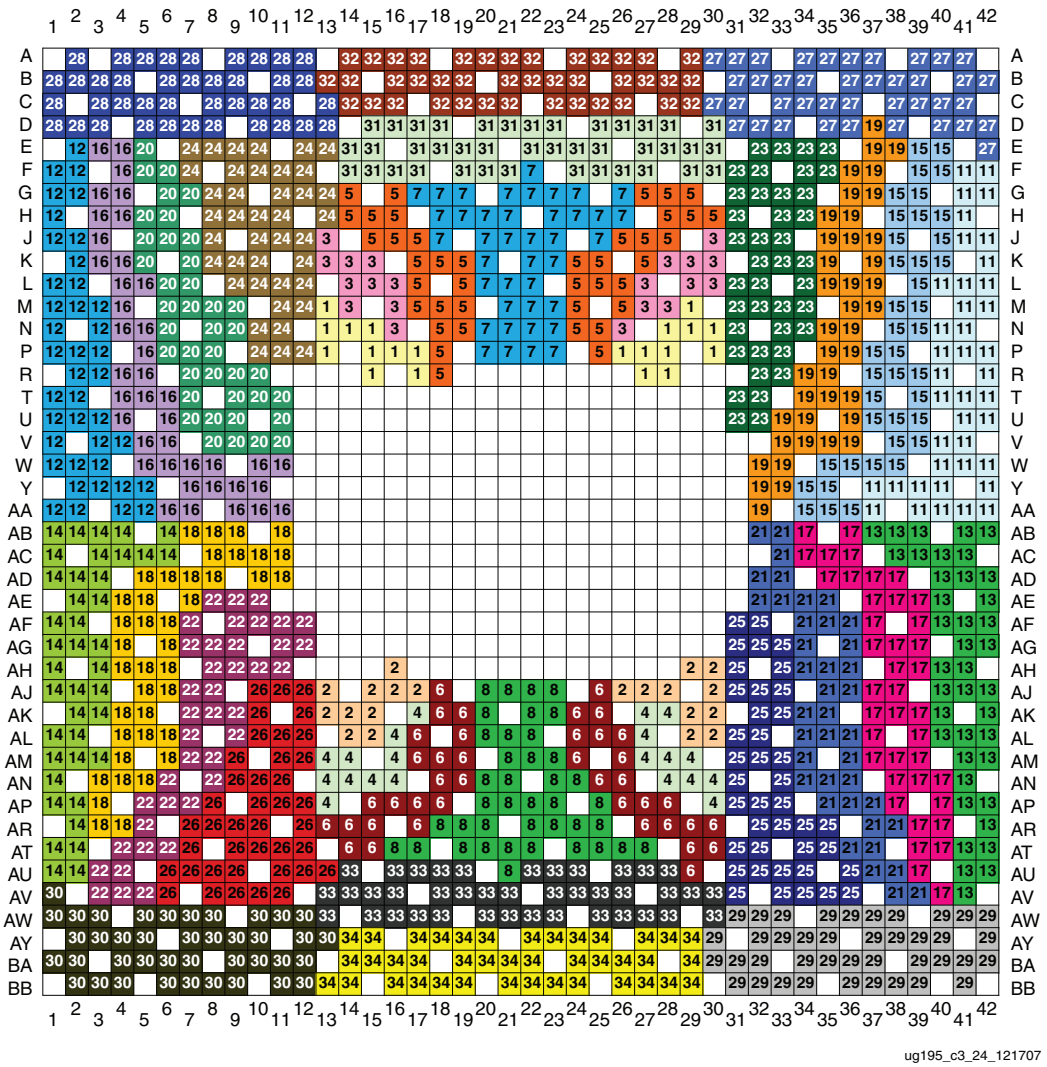


Figure 3-32: **FF1760 Package—LX330 SelectIO Bank Diagram**

XILINX®

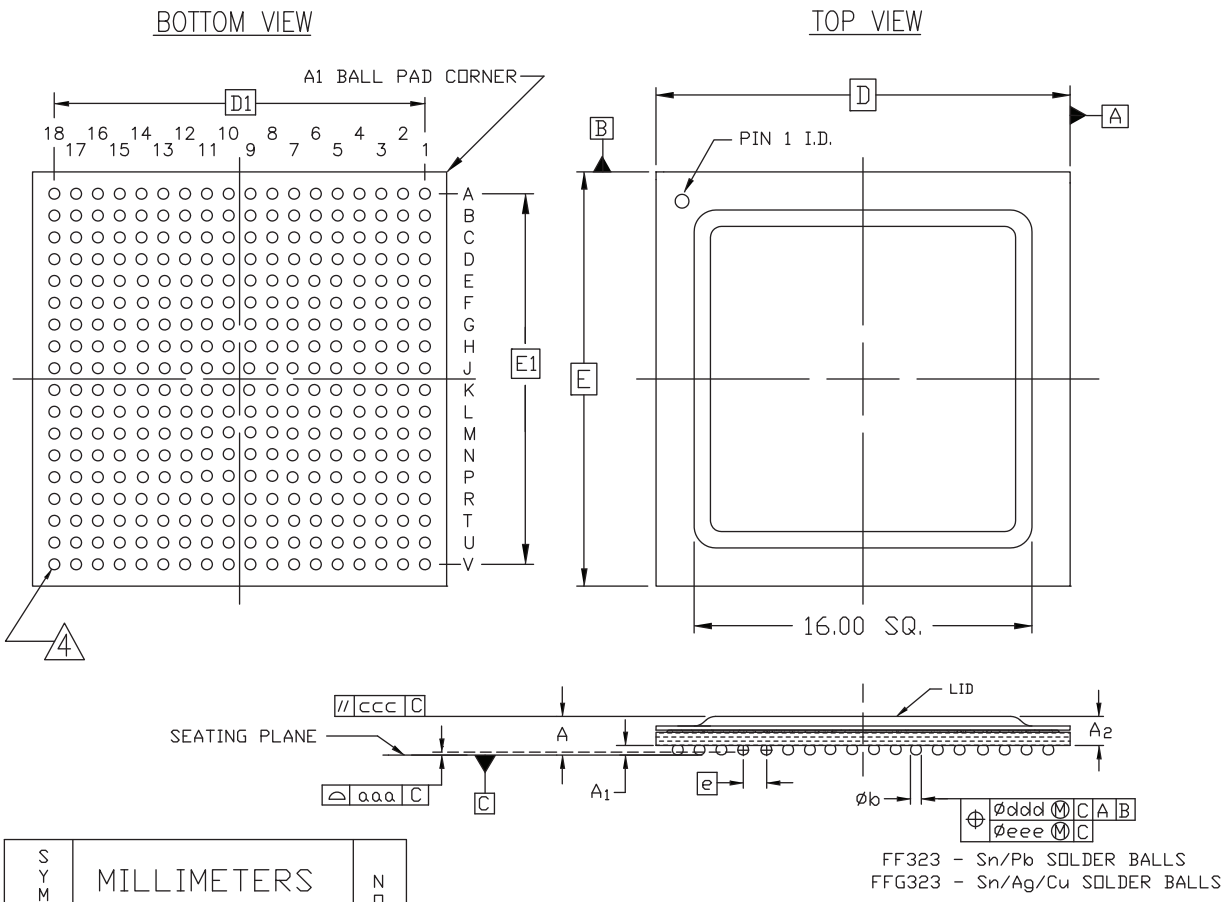
Chapter 4

Mechanical Drawings

Summary

This chapter provides mechanical drawings of the following Virtex®-5 packages:

FF323 Flip-Chip Fine-Pitch BGA Package Specifications (1.00 mm Pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	2.00	~	2.85	
A_1	0.40	~	0.60	
A_2	1.60	~	2.25	
D/E	19.00 BASIC			
D_1/E_1	17.00 REF			
e	1.00 BASIC			
øb	0.50	0.60	0.70	
aaa	~	~	0.20	
ccc	~	~	0.25	
ddd	~	~	0.25	
eee	~	~	0.10	
M	18			2

NOTES:

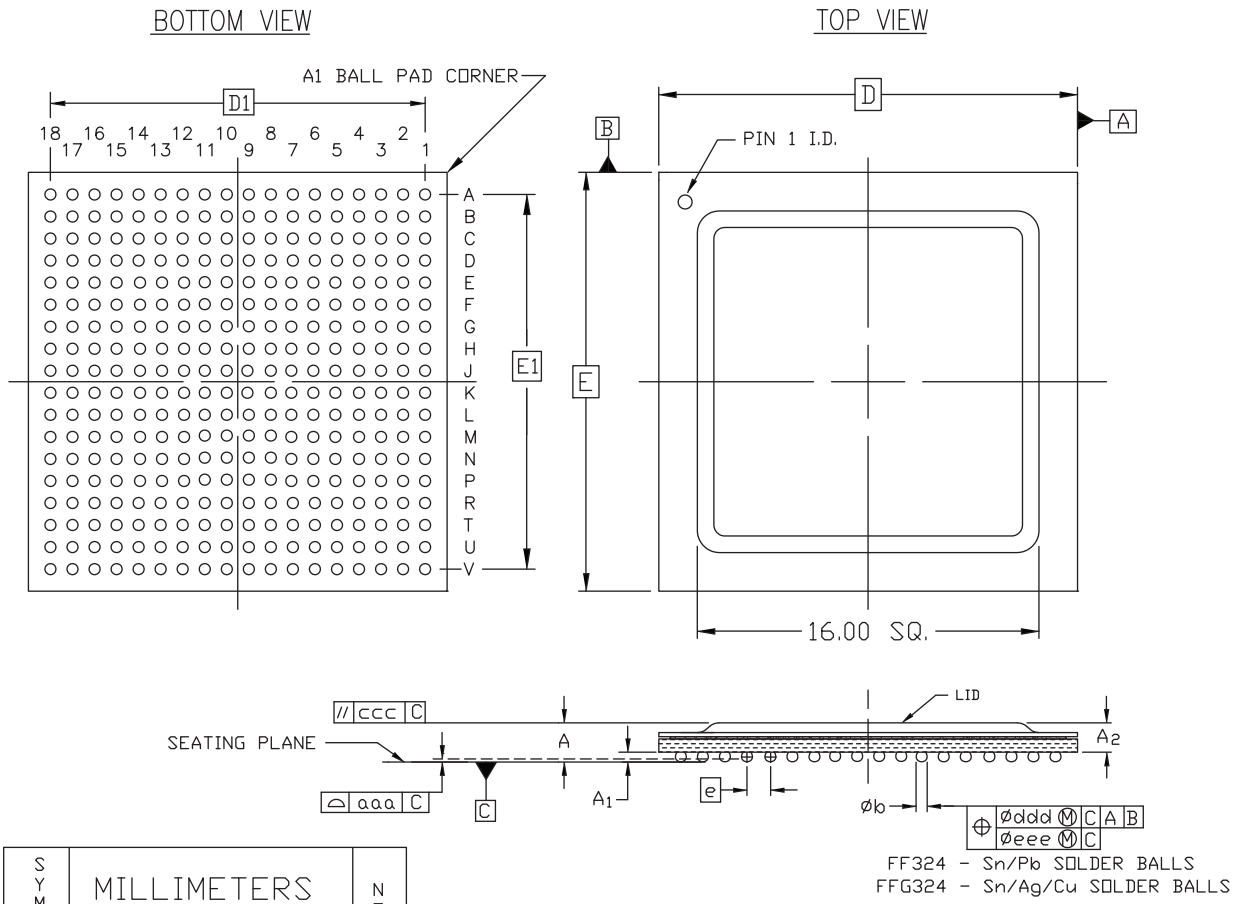
1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
3. CONFORMS TO JEDEC MS–034–AAG–1

4 SOLDER BALL COUNT = 324

ug195_c4_10_032508

Figure 4-1: **FF323 Flip-Chip Fine-Pitch BGA Package Specifications**

FF324 Flip-Chip Fine-Pitch BGA Package Specifications (1.00 mm Pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	2.00	---	2.85	
A_1	0.40	---	0.60	
A_2	1.60	---	2.25	
D/E	19.00 BASIC			
D_1/E_1	17.00 REF			
e	1.00 BASIC			
øb	0.50	0.60	0.70	
aaa	---	---	0.20	
ccc	---	---	0.25	
ddd	---	---	0.25	
eee	---	---	0.10	
M	18			2

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
3. CONFORMS TO JEDEC MS-034-AAG-1

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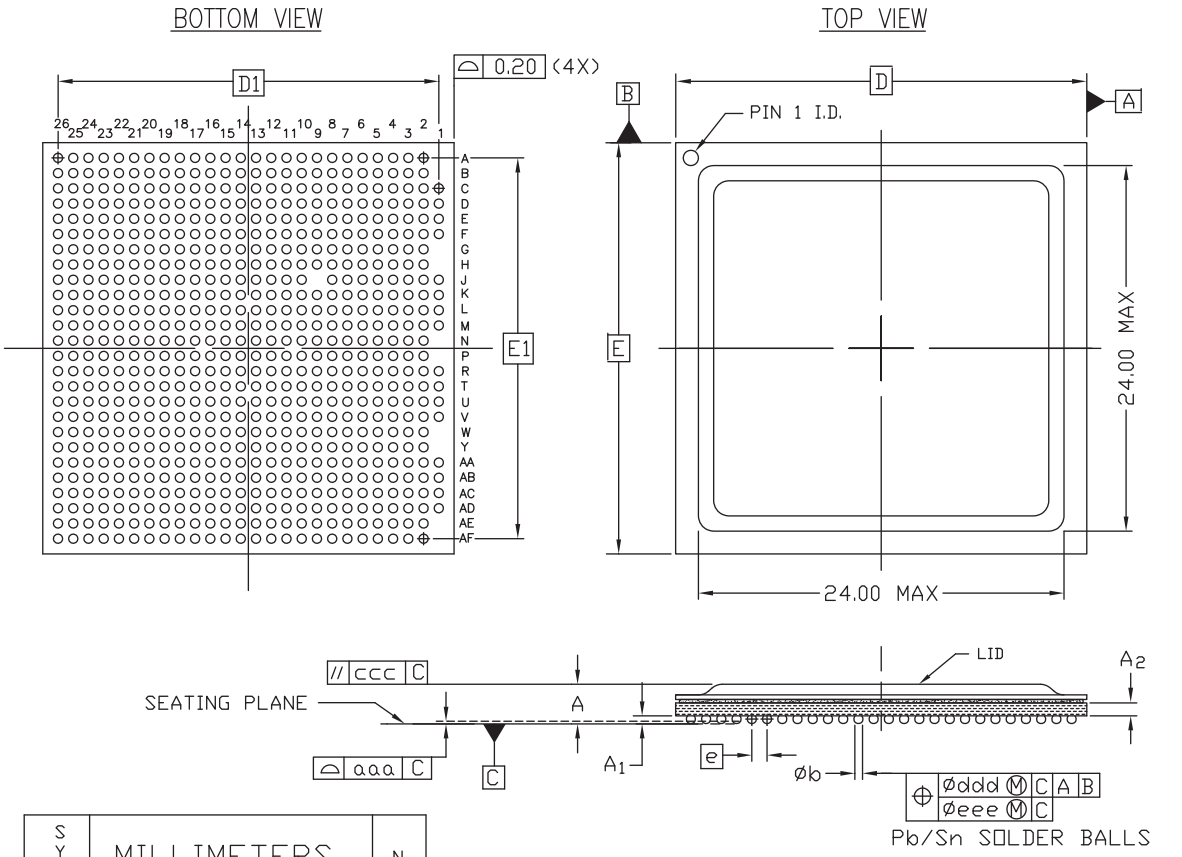
Figure 4-2: **FF324 Flip-Chip Fine-Pitch BGA Package Specifications**

EF665 Flip-Chip Fine-Pitch BGA Package Specifications (1.00 mm Pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	2.50	~~	2.90	
A_1	0.40	~~	0.60	
A_2	0.65	~~	1.10	
D/E	27.00 BASIC			
D_1/E_1	25.00 REF			
e	1.00 BASIC			
øb	0.50	0.60	0.70	
aaa	~~	~~	0.20	
ccc	~~	~~	0.25	
ddd	~~	~~	0.25	
eee	~~	~~	0.10	
M	26			2

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
3. CONFORMS TO JEDEC MS–034–AAL–1 (DEPOPULATED)

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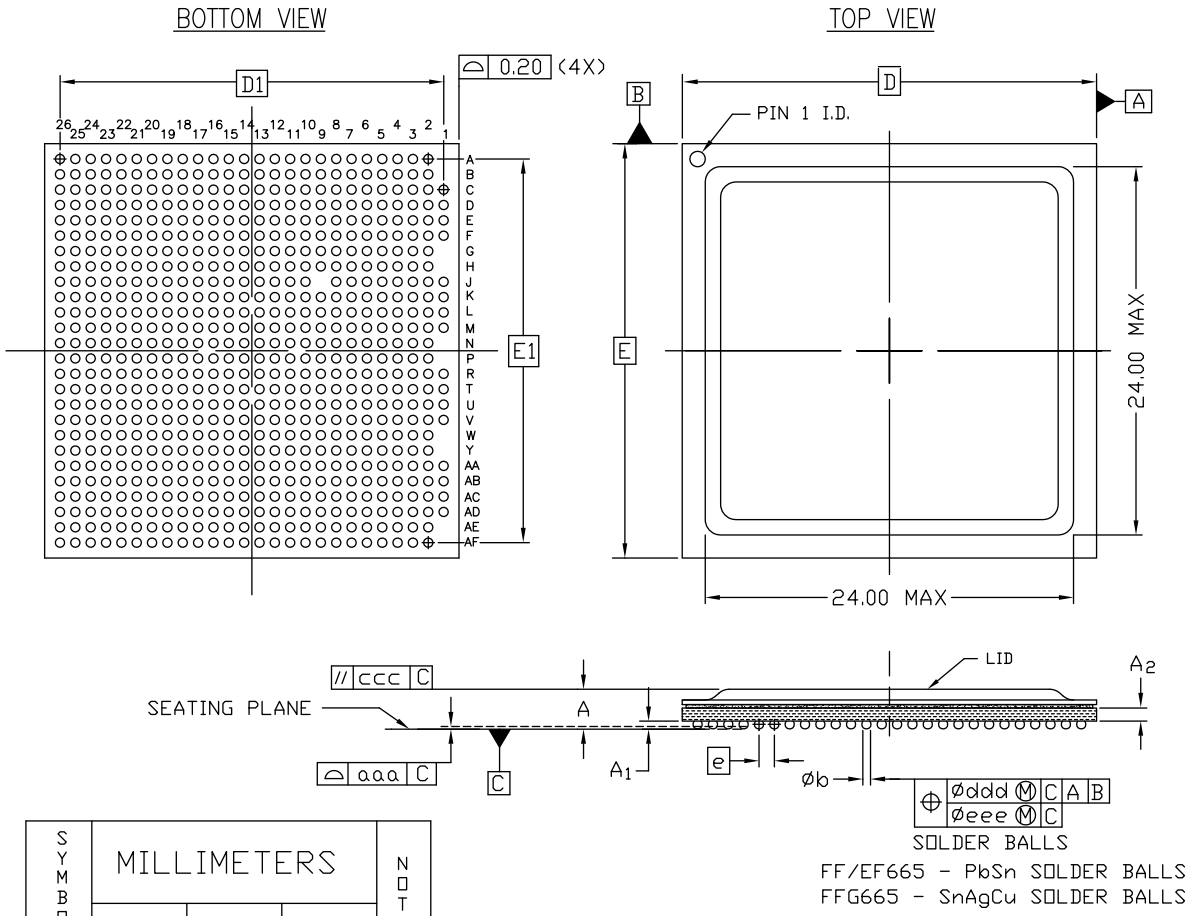
Figure 4-3: **EF665 Flip-Chip Fine-Pitch BGA Package Specifications**

FF665 Flip-Chip Fine-Pitch BGA Package Specifications (1.00 mm Pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	2.50		2.90	
A_1	0.40		0.60	
A_2	0.65		1.10	
D/E	27.00 BASIC			
D_1/E_1	25.00 REF			
e	1.00 BASIC			
øb	0.50	0.60	0.70	
aaa			0.20	
ccc			0.25	
ddd			0.25	
eee			0.10	
M	26			2

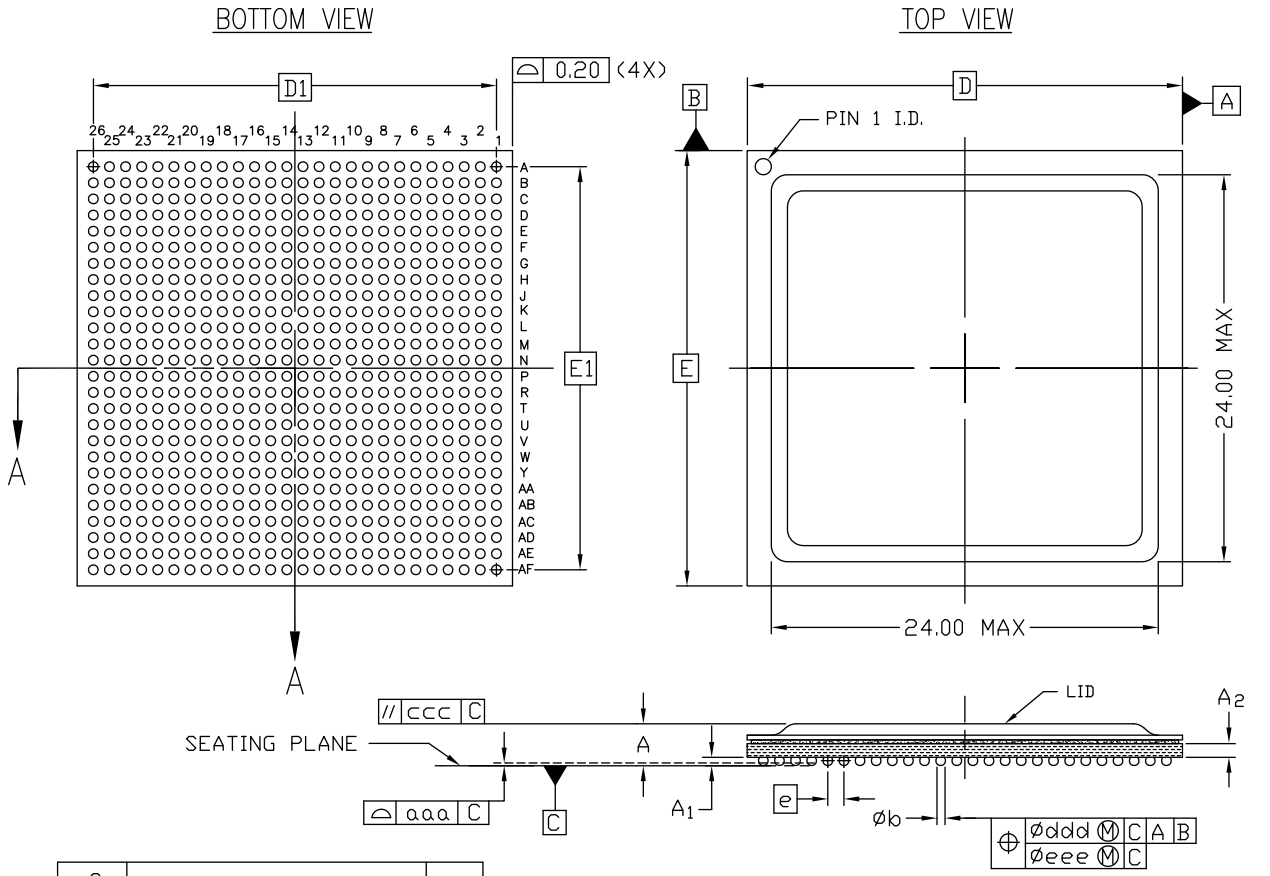
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
3. CONFORMS TO JEDEC MS-034-AAL-1 (DEPOPULATED)

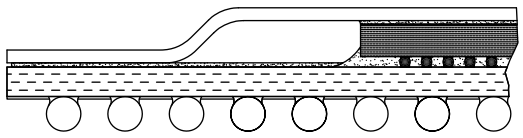
ug195_c4_02_100909

Figure 4-4: **FF665 Flip-Chip Fine-Pitch BGA Package Specifications**

FF676 Flip-Chip Fine-Pitch BGA Package Specifications (1.00 mm Pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	2.35		3.00	
A_1	0.40		0.60	
A_2	0.65		1.10	
D/E	27.00 BASIC			
D_1/E_1	25.00 REF			
e	1.00 BASIC			
øb	0.50	0.60	0.70	
aaa			0.20	
ccc			0.25	
ddd			0.25	
eee			0.10	
M	26			2



SECTION A–A
(NOT TO SCALE)

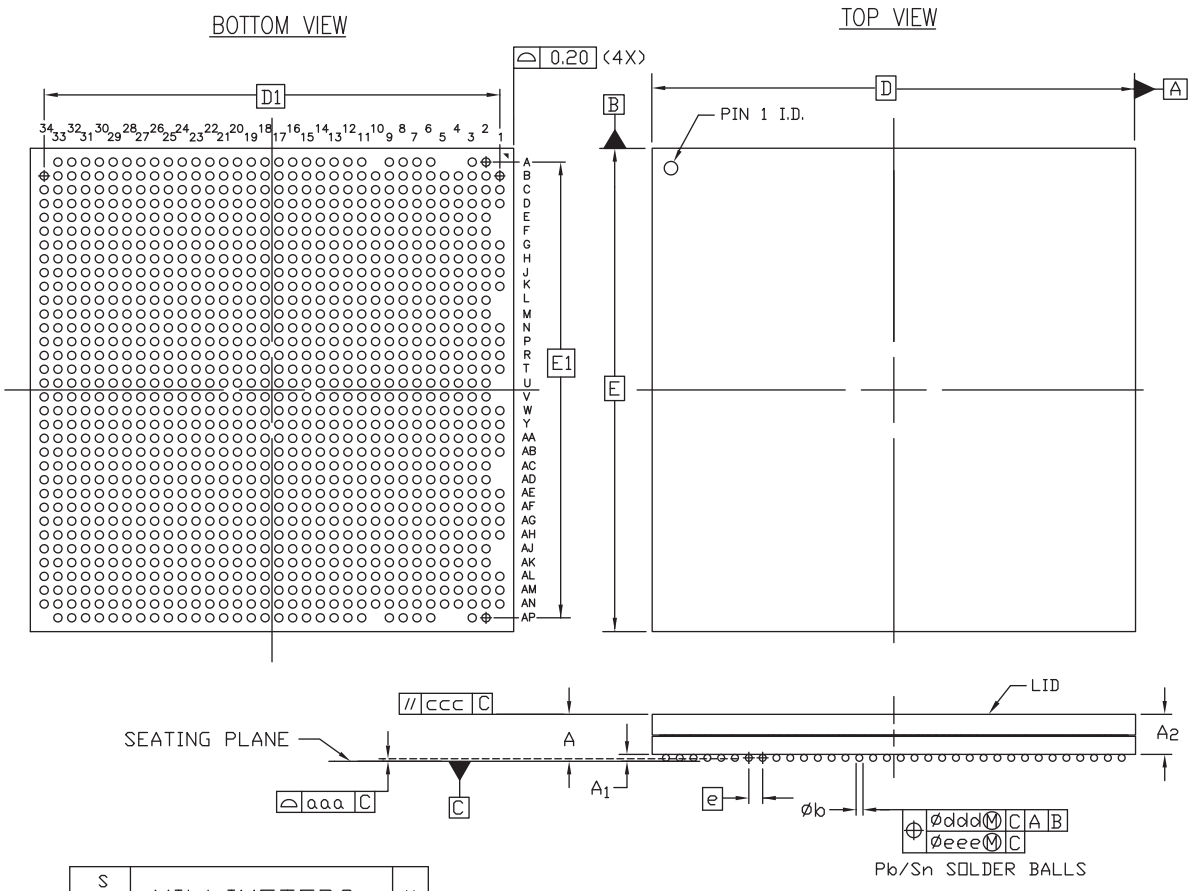
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
3. CONFORMS TO JEDEC MS–034–AAL–1

ug195_c4_03_100909

Figure 4-5: **FF676 Flip-Chip Fine-Pitch BGA Package Specifications**

EF1136 Flip-Chip Fine-Pitch BGA Package Specifications (1.00 mm Pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	2.70		3.40	
A_1	0.40	0.50	0.60	
A_2	2.30		2.80	
D/E	35.00 BASIC			
D_1/E_1	33.00 REF			
e	1.00 BASIC			
øb	0.50	0.60	0.70	
aaa			0.20	
ccc			0.35	
ddd			0.30	
eee			0.10	
M	34			2

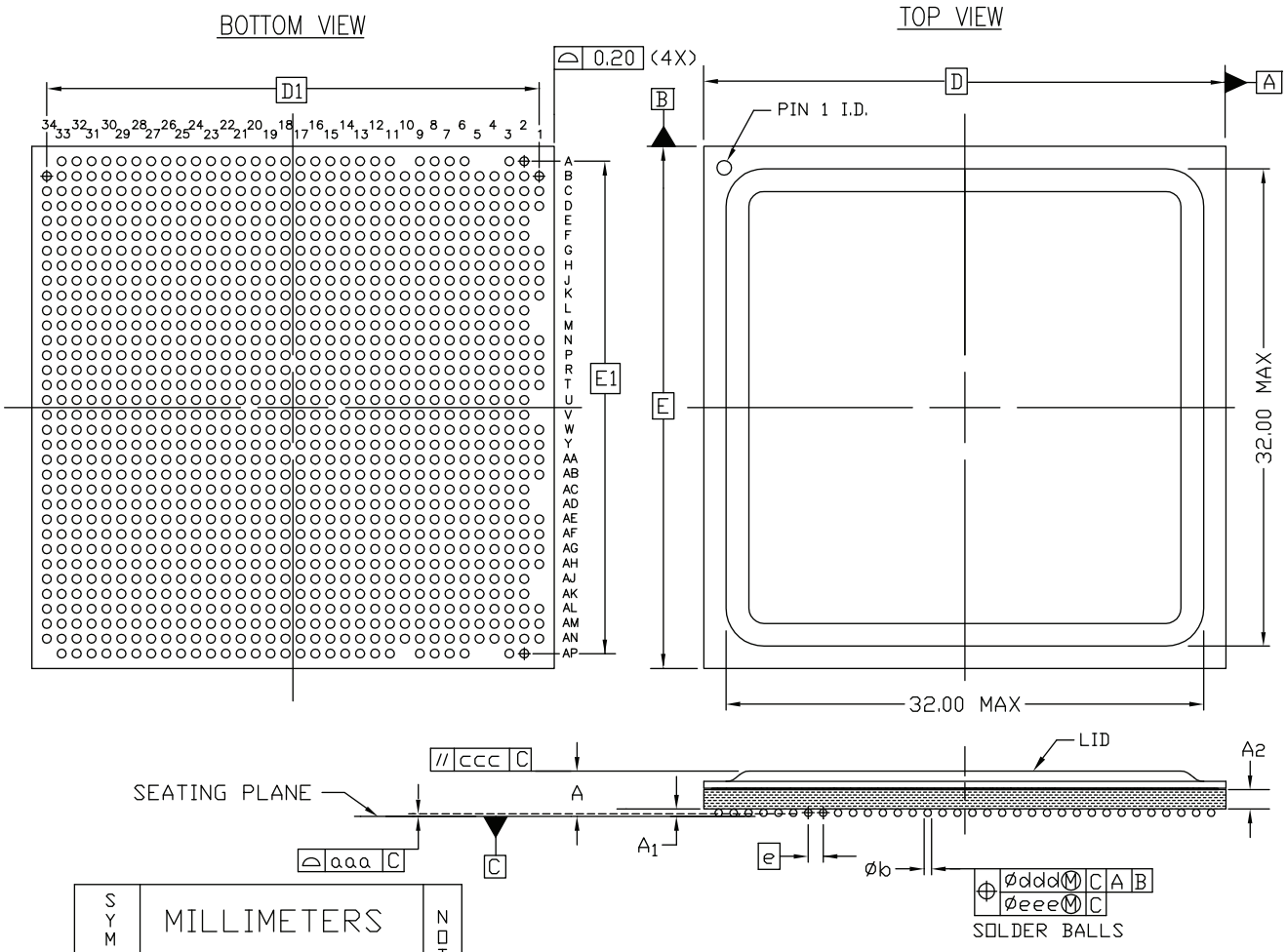
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
3. CONFORMS TO JEDEC MS–034–AAR–1 (DEPOPULATED)

ug195_c4_20_100909

Figure 4-6: **EF1136 Flip-Chip Fine-Pitch BGA Package Specifications**

FF1136 Flip-Chip Fine-Pitch BGA Package Specifications (1.00 mm Pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	2.70		3.40	
A_1	0.40	0.50	0.60	
A_2	0.90		1.40	
D/E	35.00 BASIC			
D_1/E_1	33.00 REF			
e	1.00 BASIC			
øb	0.50	0.60	0.70	
aaa			0.20	
ccc			0.35	
ddd			0.30	
eee			0.10	
M	34			2

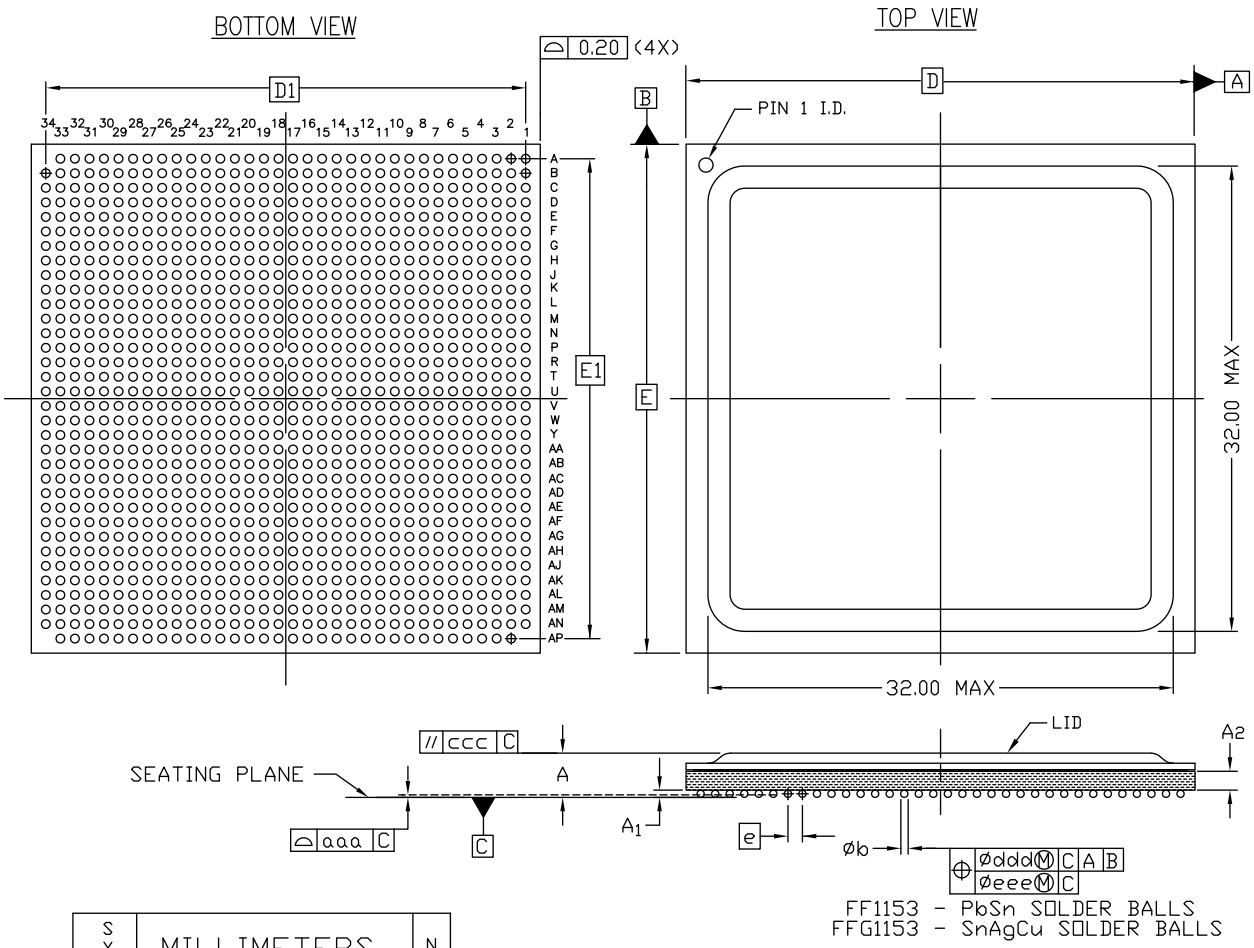
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
3. CONFORMS TO JEDEC MS–034–AAR–1 (DEPOPULATED)

ug195_c4_04_081406

Figure 4-7: **FF1136 Flip-Chip Fine-Pitch BGA Package Specifications**

FF1153 Flip-Chip Fine-Pitch BGA Package Specifications (1.00 mm Pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	2.70		3.40	
A_1	0.40	0.50	0.60	
A_2	0.90		1.40	
D/E	35.00 BASIC			
D_1/E_1	33.00 REF			
e	1.00 BASIC			
øb	0.50	0.60	0.70	
aaa			0.20	
ccc			0.35	
ddd			0.30	
eee			0.10	
M	34			2

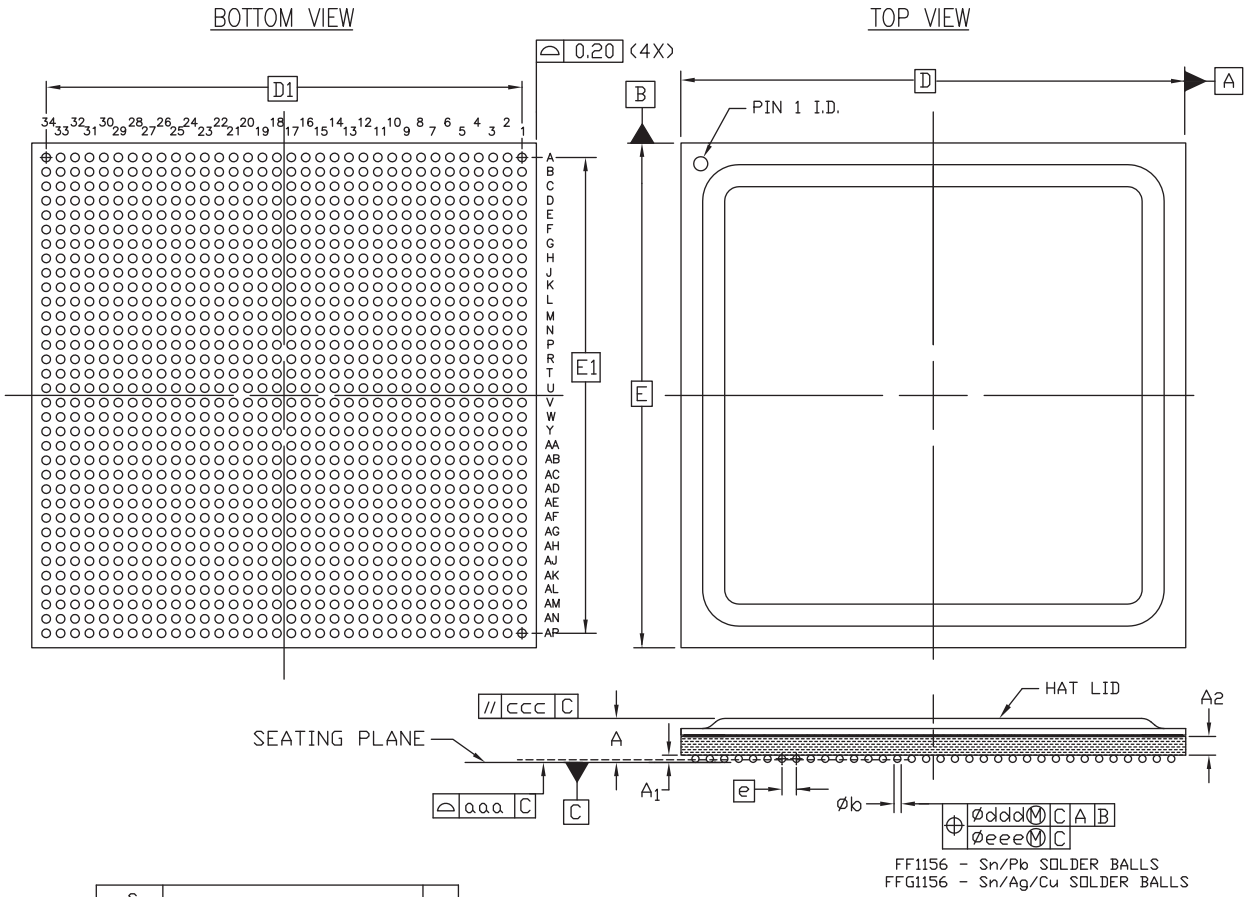
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
3. CONFORMS TO JEDEC MS–034–AAR–1 (DEPOPULATED)

ug195_c4_05_100909

Figure 4-8: **FF1153 Flip-Chip Fine-Pitch BGA Package Specifications**

FF1156 Flip-Chip Fine-Pitch BGA Package Specifications (1.00 mm Pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	2.70		3.50	
A_1	0.40	0.50	0.60	
A_2	0.90		1.50	
D/E	35.00 BASIC			
D_1/E_1	33.00 REF			
e	1.00 BASIC			
øb	0.50	0.60	0.70	4
aaa			0.20	
ccc			0.35	
ddd			0.25	
eee			0.10	
M	34			2

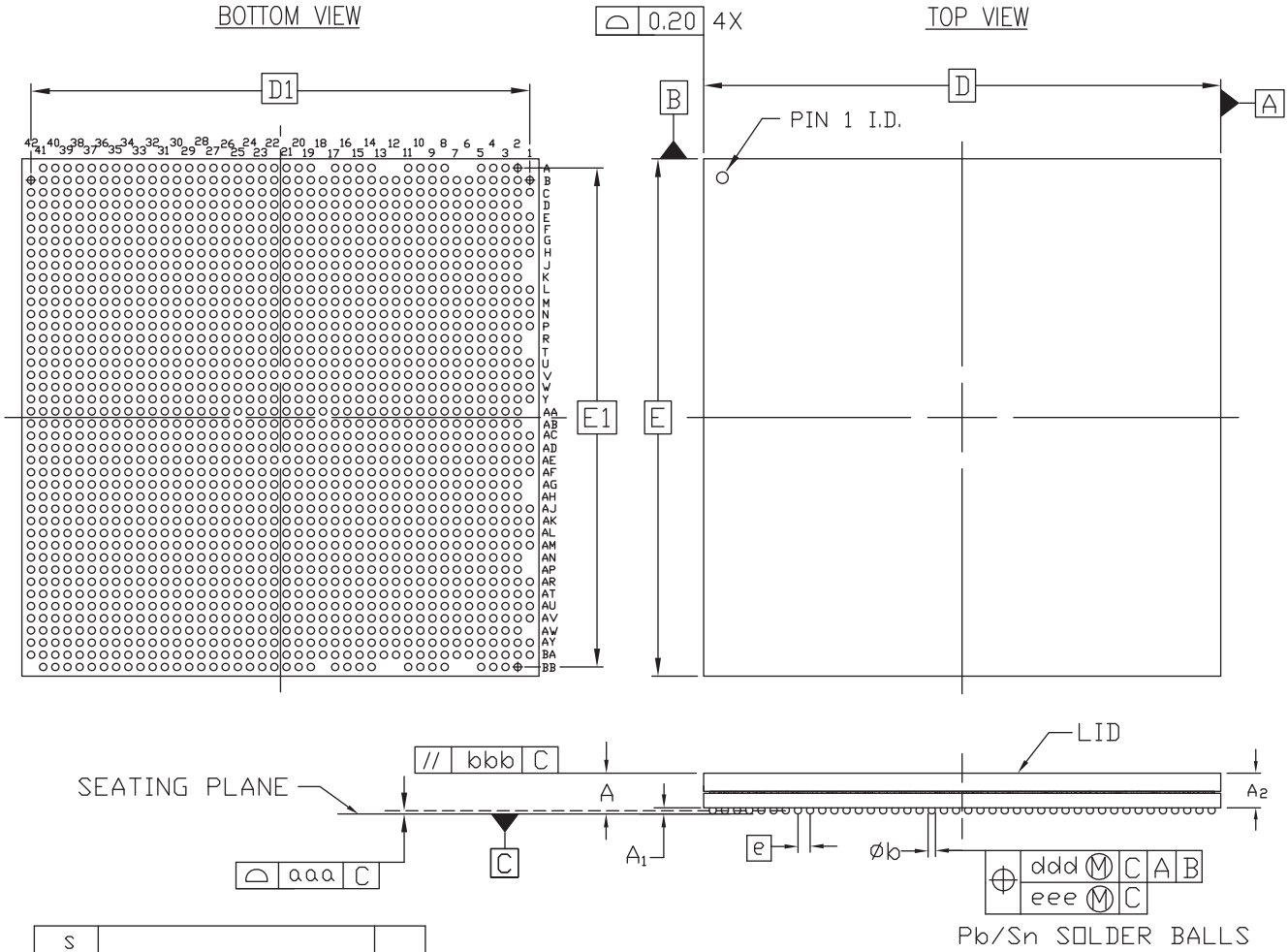
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
3. CONFORMS TO JEDEC MS–034–AAR–1
4. ACTUAL SOLDER BALL COUNT = 1156

ug195_c4_11_100909

Figure 4-9: **FF1156 Flip-Chip Fine-Pitch BGA Package Specifications**

EF1738 Flip-Chip Fine-Pitch BGA Package Specifications (1.00 mm Pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	2.70		3.50	
A_1	0.40	0.50	0.60	
A_2	2.30		2.90	
D/E	42.50 BASIC			
D_1/E_1	41.00 REF			
e	1.00 BASIC			
øb	0.50	0.60	0.70	
aaa			0.20	
bbb			0.25	
ddd			0.25	
eee			0.10	
M	42			2

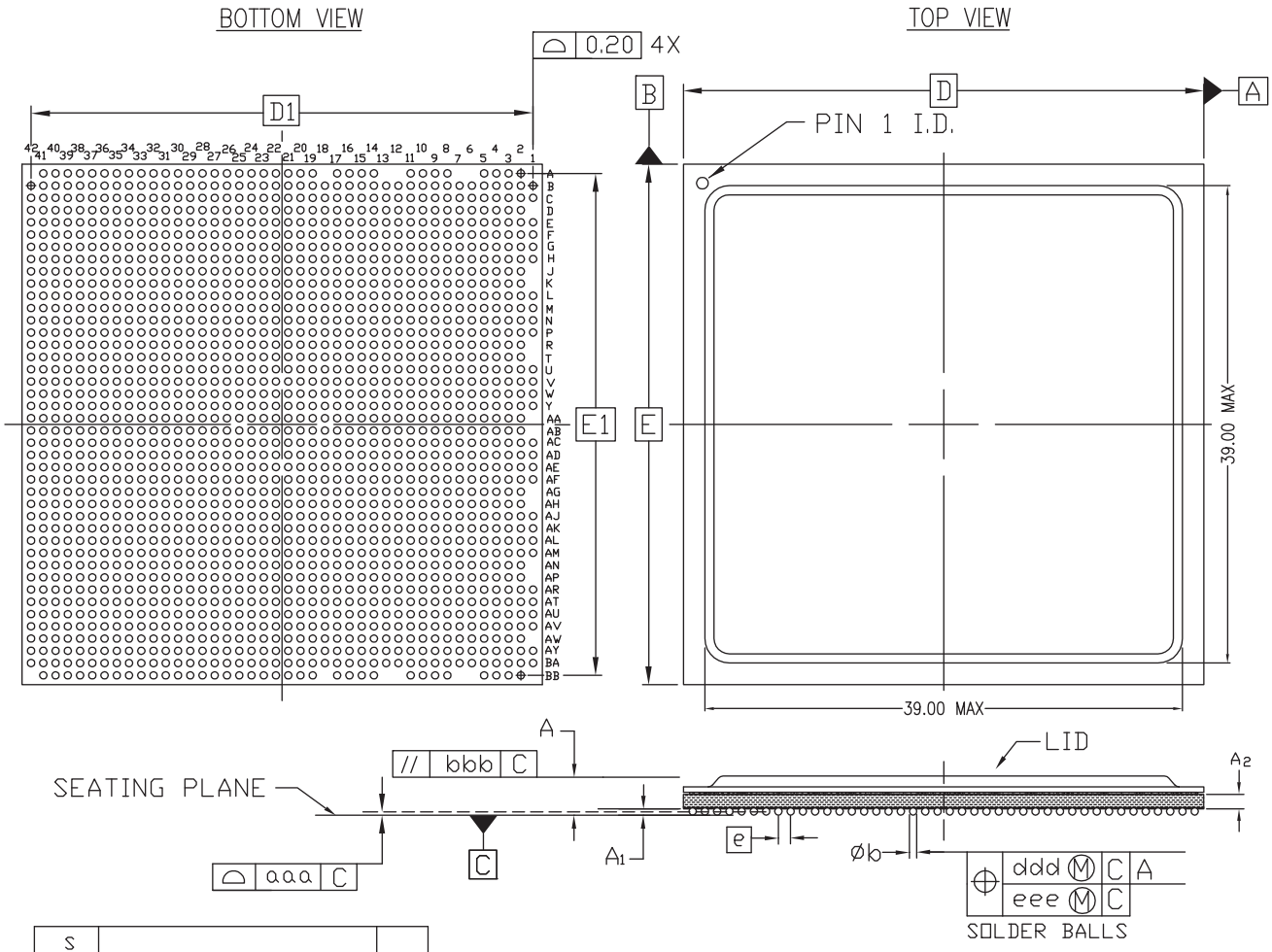
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MS–034–AAV–1 (DEPOPULATED)

ug195_c4_21_041609

Figure 4-10: **EF1738 Flip-Chip Fine-Pitch BGA Package Specifications**

FF1738 Flip-Chip Fine-Pitch BGA Package Specifications (1.00 mm Pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	2.70		3.50	
A_1	0.40	0.50	0.60	
A_2	1.00		1.40	
D/E	42.50 BASIC			
D_1/E_1	41.00 REF			
e	1.00 BASIC			
øb	0.50	0.60	0.70	
aaa			0.20	
bbb			0.25	
ddd			0.25	
eee			0.10	
M	42			2

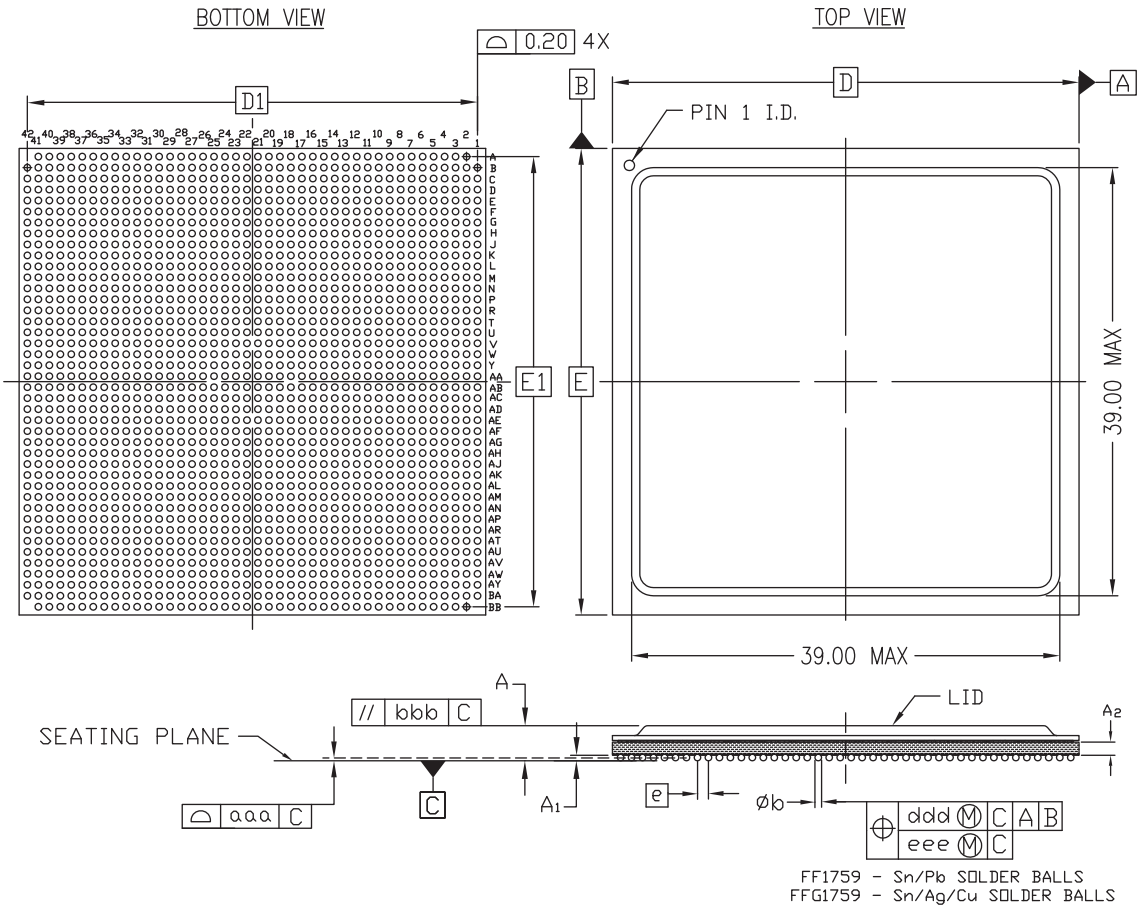
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MS–034–AAV–1 (DEPOPULATED)

ug195_c4_06_081406

Figure 4-11: **FF1738 Flip-Chip Fine-Pitch BGA Package Specifications**

FF1759 Flip-Chip Fine-Pitch BGA Package Specifications (1.00 mm Pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	2.80		3.50	
A_1	0.40	0.50	0.60	
A_2	1.10		1.50	
D/E	42.50 BASIC			
D_1/E_1	41.00 REF			
e	1.00 BASIC			
øb	0.50	0.60	0.70	4
aaa			0.20	
bbb			0.25	
ddd			0.25	
eee			0.10	
M	42			2

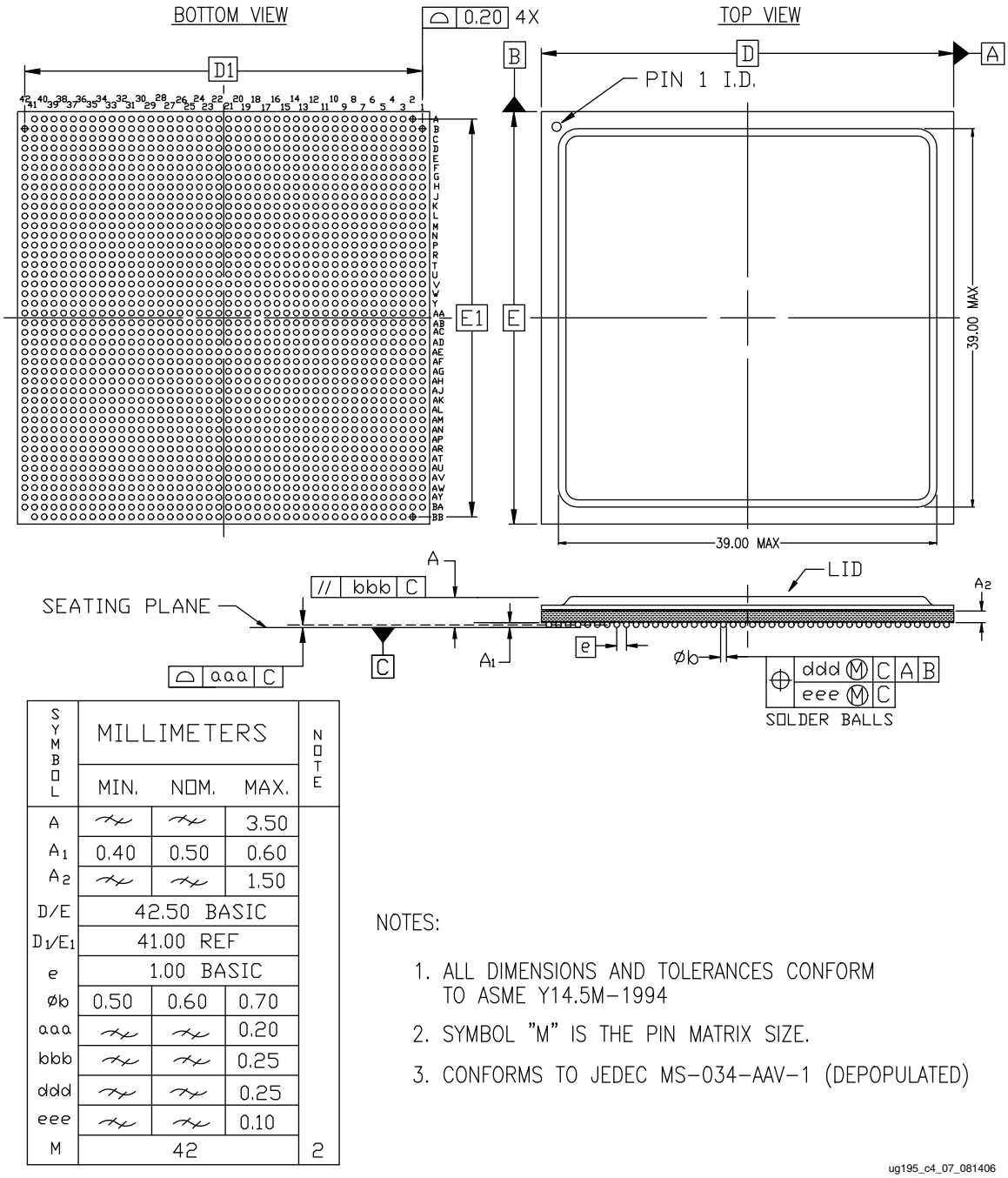
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MS–034–AAV–1 (DEPOPULATED)
4. ACTUAL SOLDER BALL COUNT = 1760

ug195_c4_11_090908

Figure 4-12: **FF1759 Flip-Chip Fine-Pitch BGA Package Specification**

FF1760 Flip-Chip Fine-Pitch BGA Package Specifications (1.00 mm Pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A			3.50	
A_1	0.40	0.50	0.60	
A_2			1.50	
D/E	42.50 BASIC			
D_1/E_1	41.00 REF			
e	1.00 BASIC			
Øb	0.50	0.60	0.70	
aaa			0.20	
bbb			0.25	
ddd			0.25	
eee			0.10	
M	42			2

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MS–034–AAV–1 (DEPOPULATED)

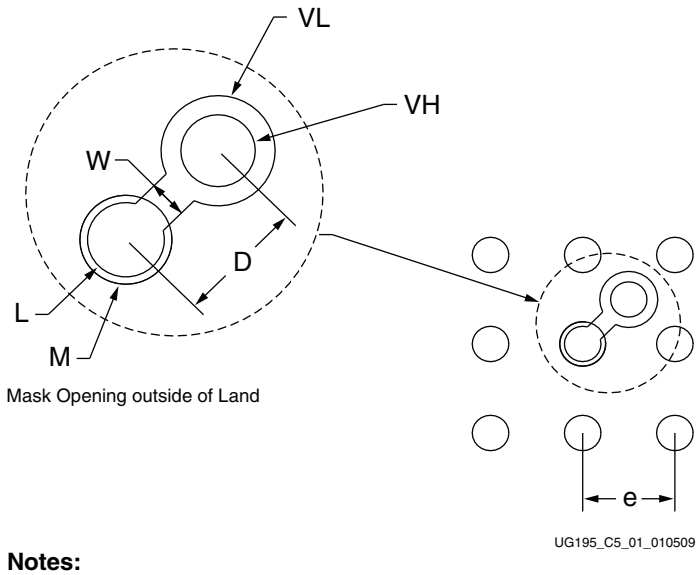
ug195_c4_07_081406

Figure 4-13: **FF1760 Flip-Chip Fine-Pitch BGA Package Specification**

Chapter 5

Recommended PCB Design Rules for BGA Packages

Xilinx provides the diameter of a land pad on the component side. This information is required prior to the start of the board layout so the board pads can be designed to match the component-side land geometry. The typical values of these land pads are described in Figure 5-1 and summarized in Table 5-1. For Xilinx® BGA packages, Non-Solder Mask Defined (NSMD) pads on the board are suggested to allow a clearance between the land metal (diameter L) and the solder mask opening (diameter M) as shown in Figure 5-1. The space between the NSMD pad and the solder mask as well as the actual signal trace widths depend on the capability of the PCB vendor. The cost of the PCB is higher when the line width and spaces are smaller.



Notes:

1. 3 x 3 matrix is shown for illustration purposes only. One land pad is shown with via connection.

Figure 5-1: **Suggested Board Layout of Soldered Pads for BGA Packages**

Table 5-1: **Recommended PCB Design Rules (Dimensions in mm)**

	EF665, EF676, FF323, FFG323, FF324, FFG324, FF665, FFG665, FF668, FFG668, FF672, FFG672, FF676, FFG676, FF896, FFG896	**EF1136, EF1153, FF1136, FFG1136, FF1148, FFG1148, FF1152, FFG1152, FF1153, FFG1153, FF1156, FFG1156, FF1696, FFG1696**	**EF1738, FF1513, FFG1513, FF1517, FFG1517, FF1704, FFG1704, FF1738, FFG1738, FF1759, FFG1759, FF1760, FFG1760**	**SF363**
Component Land Pad Diameter (SMD)(1)	0.53	0.53	0.53	0.40
Solder Land (L) Diameter	0.45	0.45	0.45	0.33
Opening in Solder Mask (M) Diameter	0.55	0.55	0.55	0.50
Solder (Ball) Land Pitch (e)	1.00	1.00	1.00	0.80
Line Width Between Via and Land (w)	0.13	0.13	0.13	0.13
Distance Between Via and Land (D)	0.70	0.70	0.70	0.56
Via Land (VL) Diameter	0.61	0.61	0.61	0.50
Through Hole (VH) Diameter	0.300	0.300	0.300	0.300

Notes:

1. Component land pad diameter refers to the pad opening on the component side (solder mask defined).

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Chapter 6

Thermal Specifications

Summary

This chapter provides thermal data associated with Virtex®-5 FPGA packages. The following topics are discussed:

- Introduction
- Power Management Strategy
- Some Thermal Management Options
- Support for Compact Thermal Models (CTM)
- References

Introduction

Virtex-5 devices are offered exclusively in thermally efficient flip-chip BGA packages. These 1.0 mm flip-chip packages range in pin-count from the smaller 19 x 19 mm FF324 to the 42.5 x 42.5 mm FF1760. The suite of packages is used to address the various power requirements of the Virtex-5 devices. All Virtex-5 devices are implemented in the 65 nm process technology

Similar to Virtex-4 FPGAs, all Virtex-5 devices feature versatile SelectIO™ resources that support a variety of I/O standards. They also include Digital Clock Managers (DCMs), DSPs, and other traditional features and blocks (such as block RAM) contained in earlier Virtex products.

In line with Moore's law, the transistor count in this family of devices has been increased substantially. Though several innovative features at the silicon level have been deployed to minimize power dissipation, including leakage at the 65 nm node, these products have more densely packed transistors and embedded blocks with the capability to run faster than before. Thus, a fully configured Virtex-5 design that exploits the fabric speed and incorporates several embedded circuits and systems can present power consumption challenges that must be managed.

Unlike features in an ASIC or a microprocessor, the combination of FPGA features used in an user application are not known to the component supplier. Therefore, it remains a challenge for Xilinx to predict the power requirements of a given FPGA when it leaves the factory. Accurate estimates are obtained when the board design takes shape. For this purpose, Xilinx offers and supports a suite of integrated device power analysis tools to help users quickly and accurately estimate their design power requirements. Virtex-5 devices are supported similarly to previous FPGA products. The uncertainty of design power requirements makes it difficult to apply canned thermal solutions to fit all users. Therefore, Xilinx devices do not come with preset thermal solutions. The user's operating conditions dictate the appropriate solution.

Table 6-1 and Table 6-2 show the thermal resistance data for Virtex-5 devices (grouped in the packages offered). The data includes junction-to-ambient in still air, junction-to-case, and junction-to-board data based on standard JEDEC four-layer measurements.

- Thermal data is available on the Xilinx website at:
  http://www.xilinx.com/cgi-bin/thermal/thermal.pl.
- Compact package thermal models for these products are available on the Xilinx support download center at:
  http://www.xilinx.com/xlnx/xil_sw_updates_home.jsp.

Table 6-1: **Thermal Resistance Data—LX Devices**

Package	Package Body Size	Devices	θ_{JA} (°C/W)	θ_{JB} (°C/W)	θ_{JC} (°C/W)	θ_{JA} (°C/W) @ 250 LFM	θ_{JA} (°C/W) @ 500 LFM	θ_{JA} (°C/W) @ 750 LFM
FF324 FFG324	19x19	XC5VLX30	18.5	4.5	0.18	12.9	11.4	10.5
		XC5VLX50	18.5	4.5	0.18	12.9	11.4	10.5
FF676 FFG676	27x27	XC5VLX30	12.1	3.2	0.19	7.8	6.6	6.1
		XC5VLX50	12.1	3.2	0.19	7.8	6.6	6.1
		XC5VLX85	12.0	3.1	0.17	7.7	6.5	6.0
		XC5VLX110	11.7	2.8	0.12	7.4	6.3	5.7
FF1153 FFG1153	35x35	XC5VLX50	10.2	2.7	0.19	6.3	5.3	4.8
		XC5VLX85	10.0	2.6	0.17	6.1	5.1	4.7
		XC5VLX110	9.8	2.5	0.13	6.0	5.0	4.5
		XC5VLX155	9.7	2.5	0.10	5.9	4.9	4.4
FF1760 FFG1760	42.5x42.5	XC5VLX110	8.0	2.0	0.12	4.9	4.0	3.6
		XC5VLX155	8.0	2.2	0.10	4.9	4.0	3.6
		XC5VLX220	7.6	1.6	0.10	4.5	3.6	3.3
		XC5VLX330	7.6	1.6	0.10	4.5	3.6	3.3

Table 6-2: **Thermal Resistance Data—LXT, SXT, TXT, and FXT Devices**

Package	Package Body Size	Devices	θ_{JA} (°C/W)	θ_{JB} (°C/W)	θ_{JC} (°C/W)	θ_{JA} (°C/W) @ 250 LFM	θ_{JA} (°C/W) @ 500 LFM	θ_{JA} (°C/W) @ 750 LFM
FF323 FFG323	19x19	XC5VLX20T	18.9	5.3	0.44	13.7	11.9	11.1
		XC5VLX30T	18.6	4.6	0.27	13.4	11.6	10.8
FF665 FFG665	27x27	XC5VLX30T	12.1	3.2	0.19	7.8	6.6	6.1
		XC5VFX30T	11.9	3.2	0.13	7.6	6.4	5.9
		XC5VSX35T	11.8	2.9	0.15	7.5	6.3	5.8
		XC5VLX50T	12.1	3.2	0.19	7.8	6.6	6.1
		XC5VSX50T	11.8	2.9	0.15	7.5	6.3	5.8
		XC5VFX70T	11.9	3.2	0.13	7.6	6.4	5.9
FF1136 FFG1136	35x35	XC5VLX50T	10.2	2.7	0.19	6.3	5.3	4.8
		XC5VSX50T	9.9	2.5	0.12	6.0	5.0	4.6
		XC5VFX70T	9.9	2.7	0.14	6.1	5.1	4.6
		XC5VLX85T	10.0	2.6	0.17	6.1	5.1	4.7
		XC5VSX95T	9.7	2.3	0.12	5.8	4.8	4.4
		XC5VFX100T	9.6	2.0	0.10	5.7	4.7	4.3
		XC5VLX110T	9.8	2.4	0.13	6.0	5.0	4.5
		XC5VLX155T	9.7	2.5	0.10	5.9	4.9	4.4
FF1156 FFG1156	35x35	XC5VTX150T	9.7	2.4	0.10	5.8	4.8	4.3
FF1759 FFG1759	42.5x42.5	XC5VTX150T	8.0	2.0	0.10	4.8	3.9	3.5
		XC5VTX240T	7.8	1.8	0.10	4.7	3.8	3.3
FF1738 FFG1738	42.5x42.5	XC5VFX100T	7.8	2.0	0.10	4.8	3.9	3.5
		XC5VLX110T	8.0	2.0	0.12	4.9	4.0	3.6
		XC5VFX130T	7.8	2.0	0.10	4.8	3.9	3.5
		XC5VLX155T	8.0	2.2	0.10	4.9	4.0	3.6
		XC5VFX200T	7.7	1.8	0.10	4.6	3.7	3.3
		XC5VLX220T	7.8	1.8	0.10	4.6	3.8	3.4
		XC5VSX240T	7.7	1.8	0.10	4.6	3.7	3.3
		XC5VLX330T	7.6	1.6	0.10	4.4	3.6	3.2

Power Management Strategy

Xilinx relies on a multi-prong approach with regards to the heat-dissipating potential of Virtex-5 devices:

- Design and Silicon

  Significant power reduction in Virtex devices at the 90 nm and 65 nm nodes is achieved through innovative process and circuit design. For example, transistor static leakage current is minimized by more than 50 percent (comparable devices) by deploying multi-gate oxide transistors in the power-efficient Virtex-4 and Virtex-5 architectures. Despite these improvements and a lower operating voltage, the base transistor counts are higher for these Virtex-5 devices. They pack higher gate densities and the fabric is faster. Compared to previous generations, the power consumption is lower for the same design (same function and gate density) in a Virtex-5 FPGA implementation.

  However, the increased resources and functionality associated with these higher gate density devices and faster switching fabric implies that more computation is possible in shorter time. Associated with this improved functionality is potential higher power dissipation that would have been worse without the silicon and device-based innovations.

- Packaging

  At the package component level, Xilinx has selected the more efficient flip-chip BGA packages, which present a low thermal path to the outside. This package incorporates a heat spreader with a thermal interface material (TIM), as shown in Figure 6-1.

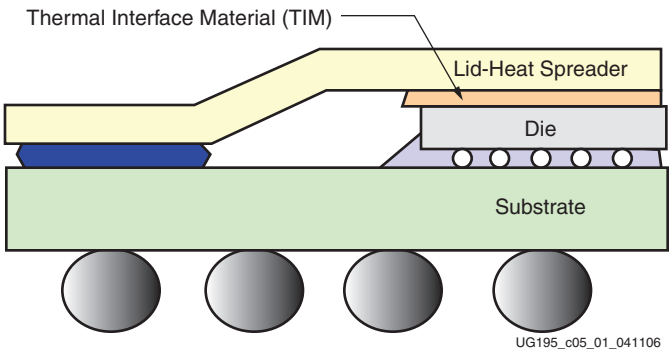

Figure 6-1: **Heat Spreader with Thermal Interface Material**

Materials with better thermal conductivity and consistent process applications deliver low thermal resistance up to the heat spreader. The junction-to-case thermal resistance (top of heat spreader) of all Virtex-5 FPGA packages is typically less than 0.20•C/W. These packages deliver a low resistance platform for heat sink applications.

The parallel effort to ensure optimized package electrical return paths has produced an added benefit of enhanced power and ground plane arrangement in the packages. The boost in copper density on the planes improves the overall thermal conductivity through the laminate. In addition, the extra dense and distributed via fields in the package increase the vertical thermal conductivity. These packages offer up to 20 percent lower θ_{JB} compared to previous flip-chips packages.

- Heat Sinking Solutions at the System Level

  Depending on the system's physical as well as mechanical constraints, the expectation is that the thermal budget is maintained with custom or OEM heat sink solutions, providing the third prong in the thermal management strategy. At this point, Xilinx has left the heat sink solution to the system-level designers who can tailor the design and solution to the constraints of their systems, being fully aware that the part has certain inherent capabilities for delivering the heat to the surface.

  Heat sink solutions do exist and can be effective on these low θ_{JB} flip-chip platforms. Table 6-3 below illustrates a finned heat sink solution matrix in Network environment (1U and 2U) arrangement for 35 mm packages and up for power ranging from 15W to 40W. The AAVID standard finned heat sink offerings are used to illustrate the coverage given thermal budgets of ΔT = 35°C and ΔT = 45°C scenarios. Other heat sink configurations can be explored similarly.

Table 6-3: **Finned Heat Sink Solution Matrix for Large Flip-chip BGA in Network**

Package Power (W)		35 x 35 mm FF1136/FF1153/FF1156		42.5 x 42.5 mm FF1738/FF1759/FF1760	
		ΔT=35°C	ΔT=45°C	ΔT=35°C	ΔT=45°C
15W	1U(5)	Note 1		Note 1	
	2U(6)	Note 1		Note 1	
25W	1U(5)	Note 4	Note 2	Note 4	Note 2
	2U(6)	Note 2	Note 1	Note 2	Note 1
35W	1U(5)	Note 4	Note 3	Note 4	Note 3
	2U(6)	Note 4	Note 2	Note 4	Note 2
40W	1U(5)	–		Note 4	Note 3
	2U(6)	–		Note 3	Note 2

Notes:

1. Solution available at 200 LFM, for example, AAVID finned part number 68520, 72390, 72415.
2. Solution available at 400 LFM, for example, AAVID finned part number 68520, 69920.
3. Solution available at 600 LFM, for example, AAVID finned part number 72390, 69920, 74590.
4. No standard. AAVID finned solution below 600 LFM—custom finned might be required.
5. For 1U Height—(max heat sink height = 26 mm)
6. For 2U Height—(max heat sink height = 64 mm

The Virtex-5 FPGA packages can be grouped into medium- and high-performance packages based on their power handling capabilities. All Virtex-5 FPGA packages can use thermal enhancements, ranging from simple airflow to schemes that can include passive as well as active heat sinks. This is particularly true for the bigger flip-chip BGA packages where system designers have the option to further enhance the packages with bigger and more elaborate heat sinks to handle excesses of 25W with arrangements that consider system –physical constraints as illustrated in Table 6-3.

Some Thermal Management Options

The flip-chip thermal management chart in Figure 6-2 illustrates simple but incremental power management schemes that can be applied on a flip-chip BGA package.

Low End 1–6W	Bare Package with Moderate Air 8–12°C/W	Bare Package Package can be used with moderate airflow within a system
Mid Range 4–10W	Passive H/S + Air 5–10°C/W	Packaged Used with Various Forms of Passive Heat Sinks Heat spreader techniques
High End 8–25W	Active Heat Sink 2–3°C/W or Better	Package Used with Active Heat Sinks TEC and board level heat spreader techniques

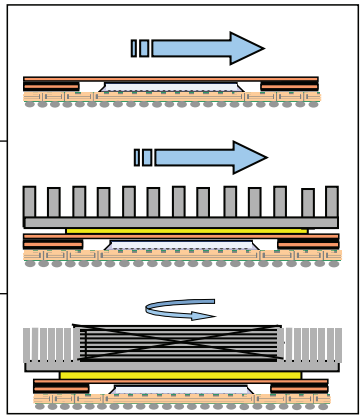

Figure 6-2: **Thermal Management Options for Flip-Chip BGA Packages**

- For moderate power dissipation (less than 6W), the use of passive heat sinks and heat spreaders attached with thermally conductive double-sided tapes or retainers (with TIM around 0.2•C/W) can offer quick thermal solutions in these packages.
- The use of lightweight, finned, external, passive heat sinks can be effective for dissipating up to 10–25W in the bigger packages. The more efficient external heat sinks tend to be tall and heavy. To help protect component joints from heat sink induced stress cracks, the use of spring-loaded pins or clips that transfer the mounting stress to a circuit board is advisable whenever a bulky heat sink is considered.
- As stated earlier, the flip-chip BGA packages offered for Virtex-5 devices are thermally enhanced BGAs with the die facing down. These packages have an exposed metal heat sink at the top. These high-end thermal packages lend themselves to the application of efficient external heat sinks (passive or active) for further heat removal efficiency. Again, precautions must be taken to prevent component damage when a bulky heat sink is attached. The thermal interface resistance needs to be controlled to take full advantage of these packages.
- An active heat sink might include a simple heat sink incorporating a mini fan or even a Peltier Thermoelectric Cooler (TEC) with a fan to carry away any dissipated heat. When considering the use of a TEC for heat management, consultation with experts in using the device is important because these devices can be reversed and cause damage to components. Also condensation can be an issue with these devices.
- The printed circuit board on which the package is mounted can have a significant impact on thermal performance. As much as 60 to 80 percent of the dissipated heat can go through the BGA balls and thus to the board. A typical systems board is larger than the standard 4 x 4 in JEDEC thermal board. Components mounted on these boards with multiple copper layers and several internal vias show low effective junction-to-ambient thermal resistances.

  Table 6-4 shows this impact as an FF1148 flip-chip package's effective junction to ambient resistance is changed depending on the mounting board.

Table 6-4: **Impact of Mounted Board Characteristics on θ_{JA}(FF1148)**

Xilinx 35 x 35mm FF1148		θ_{JA} (°C/W) for Different Board Sizes		
		4 x 4 in	10 x 10 in	20 x 20 in
Layer Count of Mounted Board	4	9.1 (1)	8.3	–
	8	8.0	5.5	4.9
	12	7.5	4.7	4.4
	16	7.2	4.5	4.2
	24	–	4.3	4.0

Notes:

1. Base JEDEC Mount Conditions

- Designs can be implemented to take advantage of the board's ability to spread heat. The effect of the board is dependent on its size and how it conducts heat. Board size, the level of copper traces, and the number of buried copper planes all lower the junction-to-ambient thermal resistance for a package mounted on the board. The cold ring junction-to-board thermal data for Virtex-5 FPGA packages are given in Table 6-1. Users need to be aware that a direct heat path to the board from a component also exposes the component to the effect of other heat sources on the board, particularly if the board is not cooled effectively. An otherwise cooler component can be heated by other heat contributing components on the board.

Support for Compact Thermal Models (CTM)

Table 6-1 provides the traditional thermal resistance data for Virtex-5 devices. These resistances are measured using a prescribed JEDEC standard that might not necessarily reflect the user's actual board conditions and environment. The quoted θ_{JA}, and θ_{JC} numbers are environmentally dependent, and JEDEC has traditionally recommended that these be used with that awareness. For more accurate junction temperature prediction, these might not be enough, and a system-level thermal simulation might be required. Though Xilinx continues to support these figure of merit data, for Virtex-5 FPGAs, boundary conditions independent compact thermal models (BCI-CTM) are also available to assist users in their thermal simulations.

Two-resistor as well as eight to ten-resistor network models are offered for all Virtex-5 devices. These compact models seek to capture the thermal behavior of the packages more accurately at predetermined critical points (junction, case, top, leads, and so on) with the reduced set of nodes as illustrated in Figure 6-3.

Unlike a full 3D model, these are computationally efficient and work well in an integrated system simulation environment. Delphi CTM models are available on the Xilinx support download center at: http://www.xilinx.com/xlnx/xil_sw_updates_home.jsp.

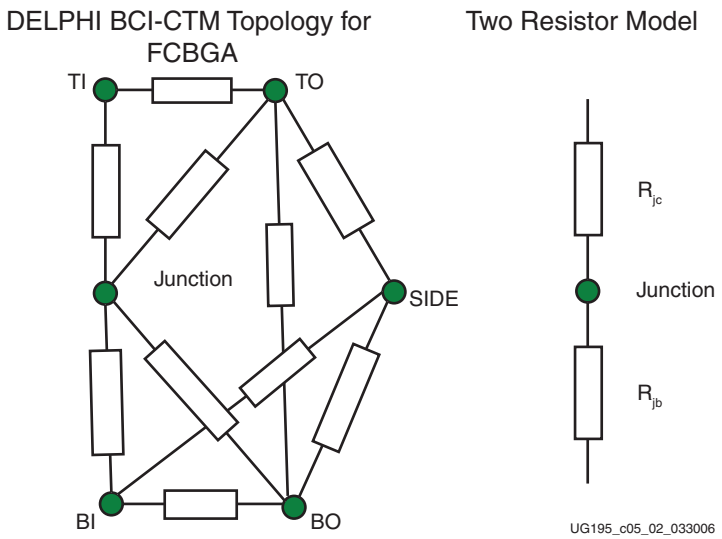

Figure 6-3: **Thermal Model Topologies**

The CTM models are based on the DELPHI approach that JEDEC has proposed. Since the JEDEC neutral (XML) format proposal has not been adopted yet, the DELPHI approach is used to generate these files and the data saved in the NATIVE and proprietary file formats of the targeted CFD tools - rather than follow a neutral file format. The CTM libraries are available in Flotherm (PDML) format – good for V5.1 and above and Icepack (version 4.2 and above) format.

References

The following websites contain additional information on heat management and contact information.

- http://www.wakefield.com
- http://www.aavidthermalloy.com
- http://www.qats.com

Refer to the following websites for interface material sources:

- Power Devices - http://www.powerdevices.com
- Bergquist Company - http://www.bergquistcompany.com
- AOS Thermal Compound - http://www.aosco.com
- Chometrics - http://www.chomerics.com
- Kester - http://www.kester.com

Refer to the following websites for CFD tools Xilinx supports with thermal models.

- Flomerics - Flotherm & FloPCB - http://www.flotherm.com
- Fluent - Icepak - http://www.icepak.com

Chapter 7

Package Marking

All Virtex-5 devices have package top-markings similar to the example shown in Figure 7-1 and explained in Table 7-1.

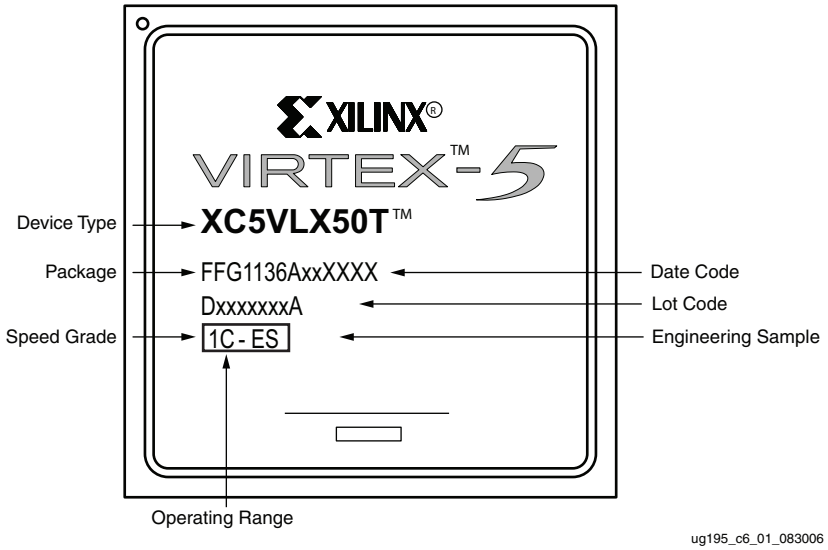

Figure 7-1: **Virtex-5 Device Package Marking**

Table 7-1: **Xilinx Device Marking Definition—Example**

Item	Definition
Xilinx Logo	Xilinx logo, Xilinx name with trademark, and trademark-registered status.
Family Brand Logo	Virtex-5 family name with trademark and trademark-registered status. This line is optional and could appear blank.
1st Line	Device type.
2nd Line	Package type and pin count, circuit design revision, the location code for the wafer fab, the geometry code, and date code. A *G* in the third letter of a package type indicates a Pb-free RoHS compliant package. For more details on Xilinx Pb-Free and RoHS Compliant Products, see: http://www.xilinx.com/pbfree.
3rd Line	Ten alphanumeric characters for Assembly, Lot, and Step information. The last digit is usually an *A* or an *M* if a stepping version does not exist. In this example, the last number on this line indicates the stepping version (2) of the device.

Table 7-1: **Xilinx Device Marking Definition—Example *(Continued)***

Item	Definition	
4th Line	Device speed grade and temperature range. If a grade is not marked on the package, the product is considered commercial grade. Other variations for the 4th line:	
	1C-xxxx	The *xxxx* indicates the SCD for the device. An SCD is a special ordering code that is not always marked in the device top mark.
	1C-ES	The *ES* indicates an Engineering Sample.