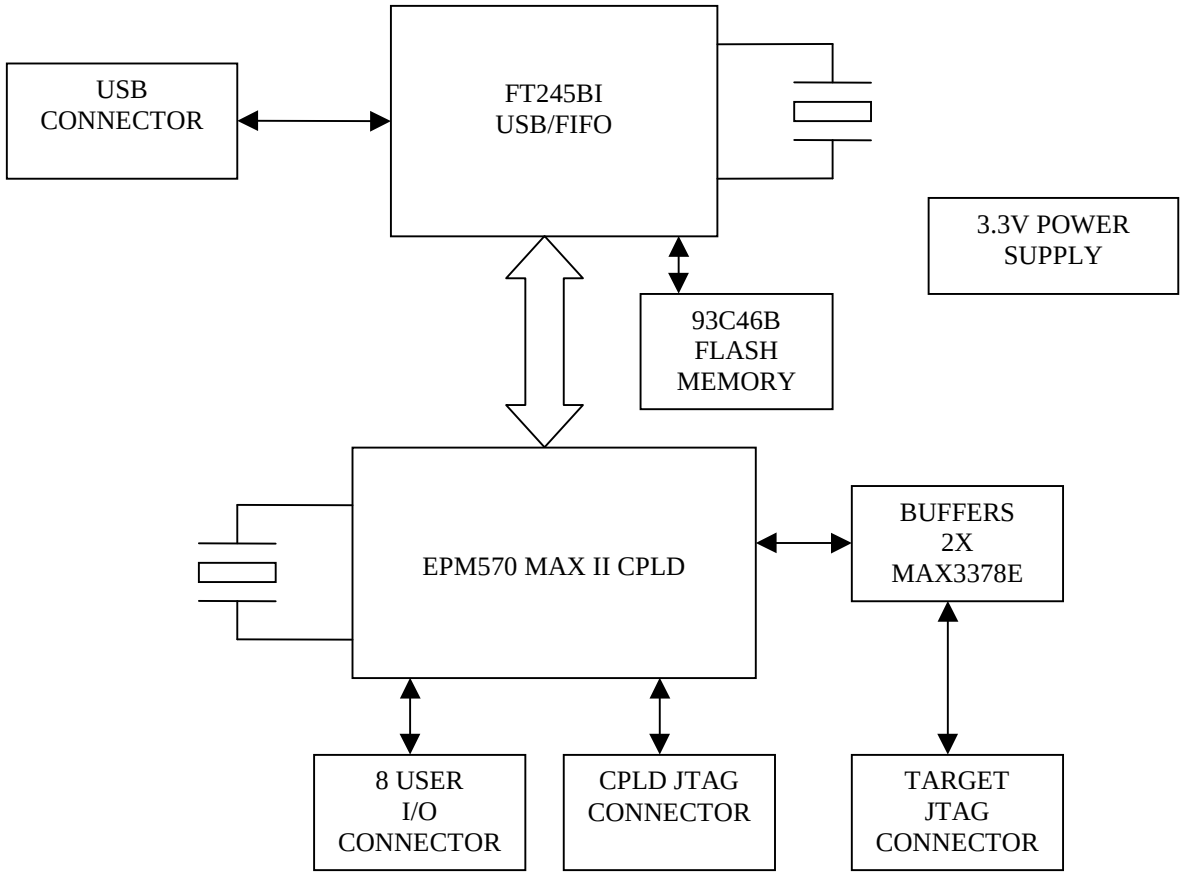
OPEN JTAG

www.openjtag.org

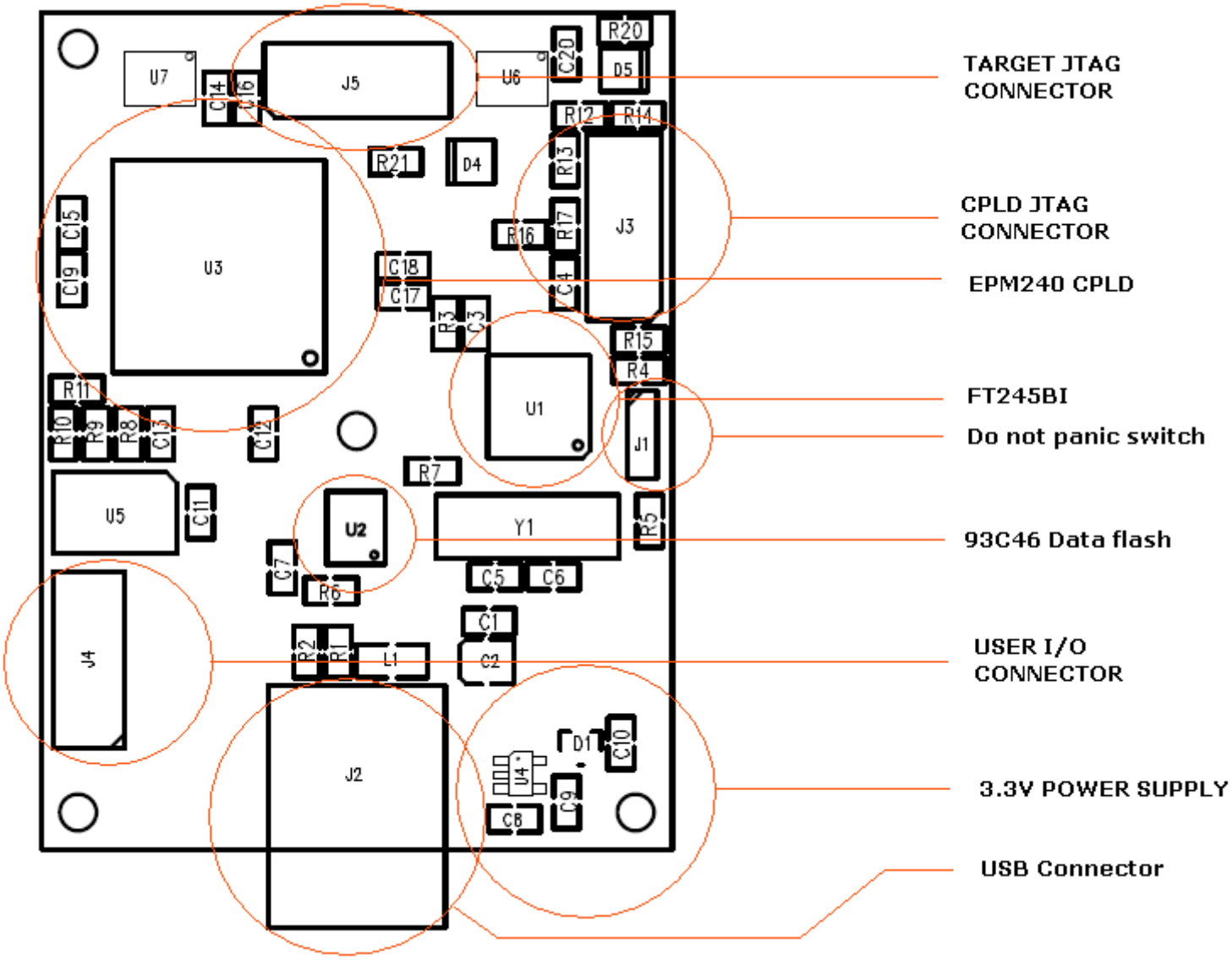
Hardware User Manual

The **OPENJTAG** hardware uses the MAX II EPM570 CPLD from Altera as serializer, and the FT245BM from FTDI Chips as USB FIFO. The circuit is simple an easy to understand. The FT245BM is the USB front end from the PC and the CPLD, bringing an easy and cheap solution to communicate with the target hardware. The EPM570 selection is because Altera has not another device with a minor pin count and enough capacity. You can see that the half device –a whole bank- is unused. The **OPENJTAG** hardware is powered from the USB power supply, using a LK112M33TR regulator to supply the internal 3.3V 140mA.
All the JTAG output pins are buffered by two MAX3378E from Maxim. This bi-directional level translators isolates the **OPENJTAG** hardware from the target device. The **OPENJTAG** hardware uses 3.3V as I/O power, but the target hardware could use a diverse power supply, as 1.2V, 1.8V, 2.5V, 3.3V or 5V. The half-part of the MAX3378E –the target side- is powered directly from the target I/O power supply.
The CPLD uses a 48MHZ crystal oscillator as the main clock supply. The shifter uses two clock pulses to output the TCK signal, then the maximum clock frequency to drive TCK will be 24MHZ.
Also, the **OPENJTAG** hardware has a 8 non protected user I/O pins to expand the board capabilities. The board have two JTAG connectors: J5 is the JTAG cable to communicate with the target device, and J3 is the JTAG cable to program the internal EPM570 CPLD.

HARDWARE BLOCK DIAGRAM



BOARD LAYOUT



CONNECTOR DESCRIPTION:

J1 – Do-not-panic switch

Sometimes, when the FT245BM is programmed, if a parameter is wrong, for example the VID (USB Vendor ID), the PC stops seeing the device as legacy device, and is not possible a further programming. Do not panic. These parameters are saved in the external 93C46B data flash. In the FT245BM the data flash is optional, used only for store custom parameters. If the data flash is unconnected, the FT245BM is seen by the PC as USB-FIFO. If this problem happens, you could:

- Remove the USB cable from the computer.
- Switch the J1 jumper to the side position.

- Wait a few seconds.
- Reconnect the USB cable to the computer
- The computer sees the device as USB FIFO. If not, sometimes is necessary to reboot the computer.
- When Windows start to see the FT245BM, move the J1 jumper back.
- Reprogram the FT245BM

J2 – USB connector

Used to connect the **OPENJTAG** hardware to the computer.

J3 – CPLD JTAG connector

This connector is only used to program the CPLD, usually using the USB Blaster, BYTE Blaster or another Altera JTAG. The pin out is:

- 1 – TCK/DCLK
- 2 – GND
- 3 - TDO/CONF_DONE
- 4 - +VCCIO
- 5 – TMS/nCONFIG
- 6 – NC
- 7 – NC
- 8 – NC
- 9 - TDI/ASDI
- 10 – GND

Note: NC = Not Connected

J4 – User I/O connector. The pin out is:

- 1 – I/O_0
- 2 – GND
- 3 – I/O_1
- 4 – +5V
- 5 – I/O_2
- 6 – I/O_7
- 7 – I/O_3
- 8 – I/O_6
- 9 – I/O_4
- 10 – I/O_5
- 11 – GND
- 12 - +VCCIO

Note: These input / output are driven directly from the EPM570 CPLD, and they are **NOT PROTECTED**. Be careful against ESD voltages, and do not exceed 3.3V level signals.

J5 – Target JTAG connector

This is the main connector, used to communicate with the hardware target. The pin out is:

- 1 – TCK/DCLK
- 2 – GND
- 3 – TDO/CONFIG
- 4 – +VCC from target hardware
- 5 – TMS/nConfig
- 6 – nCE
- 7 – DATAOUT
- 8 – nCS
- 9 – TDI/ASDI
- 10 – GND

The **OPENJTAG** board perfectly fits inside the Altera USB Blaster plastic box, and could be used as USB Blaster alternative, but the internal CPLD must be programmed differently.
You could download the Kolja Waschk project from http://www.ixo.de. The project is released with the GNU General Public License as published by the Free Software Foundation.
It will be necessary to use the Altera USB Vendor ID (VID) 09FBh and Product ID (PID) 6001h to make the Quartus II software to see the **OPENJTAG** hardware as an Altera USB Blaster.