

Spartan-6 LX9 MicroBoard	
Avnet Design Services	
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Spartan-6 LX9 MicroBoard Rev B

7/26/2011

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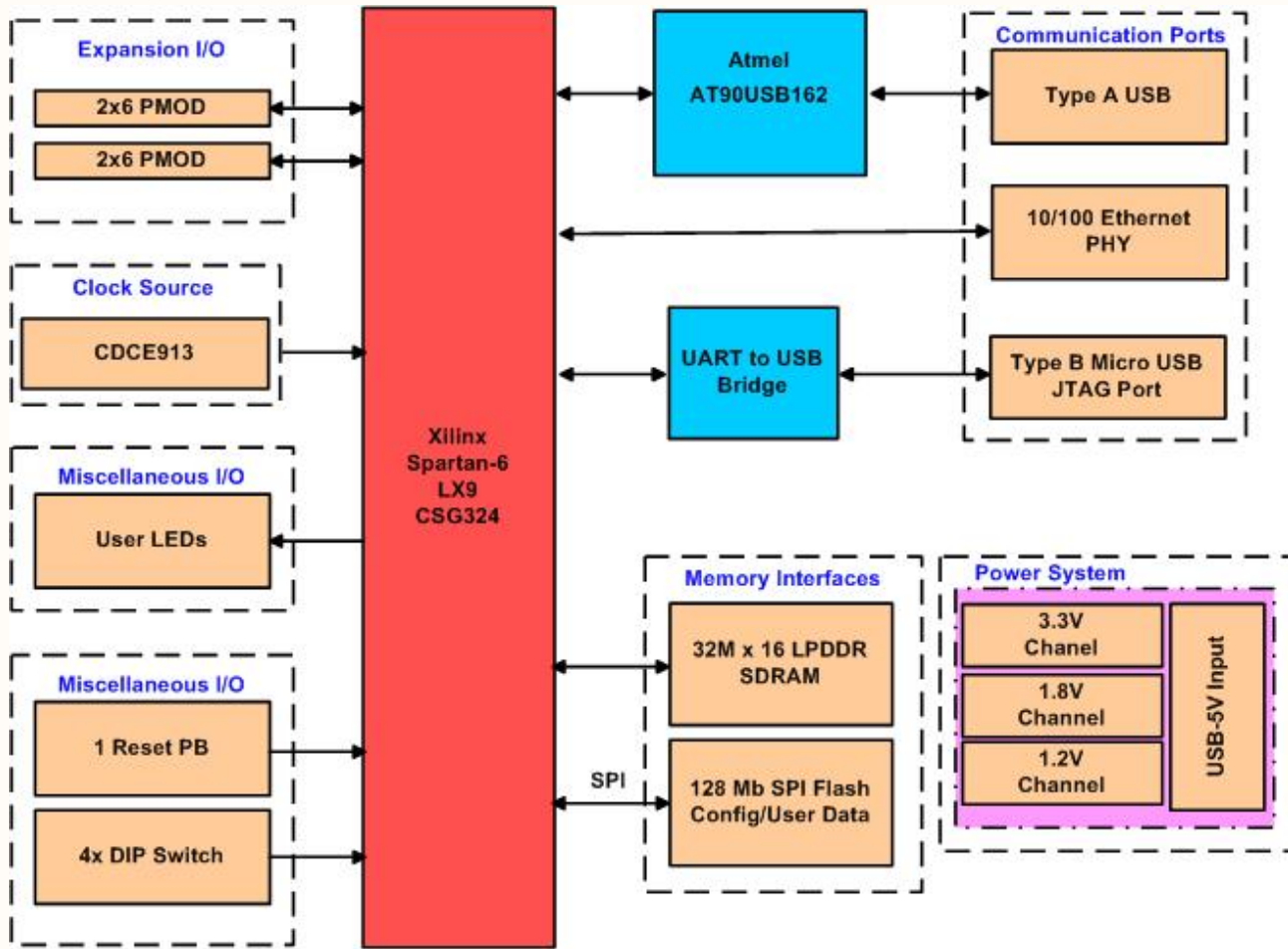
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Modified Rev A Boards are Functionally Equivalent to Rev B Boards.

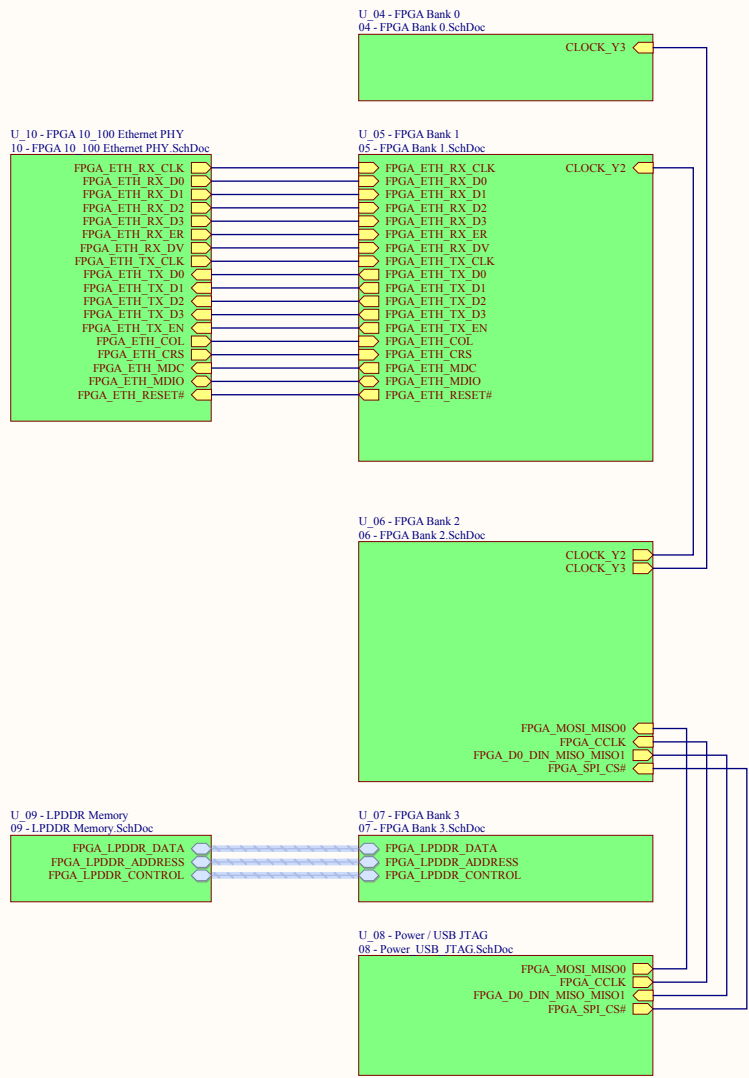
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Title: Sheet 1 - Lead Sheet		
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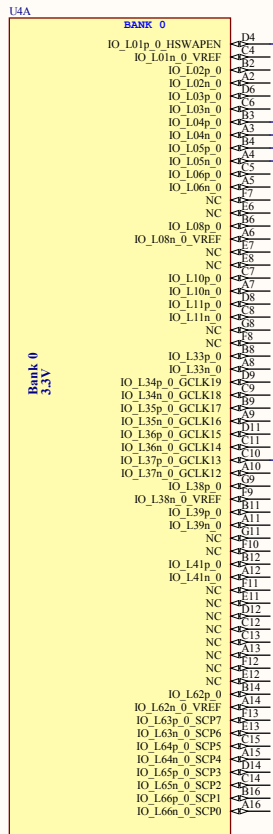
 Avnet Engineering Services	
Title: Sheet 2 - Block Diagram	
Size: B	Document Number: S6-LX9-SCH-B
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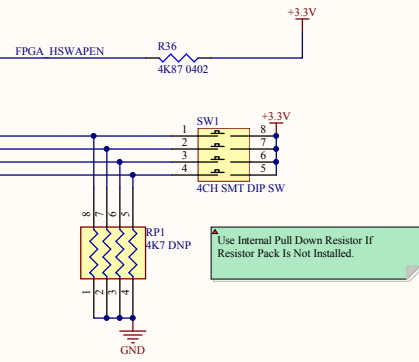
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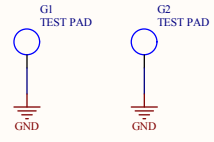
Avnet Engineering Services			
Title: Sheet 3 - Architecture			
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XC6SLX9-2CSG324



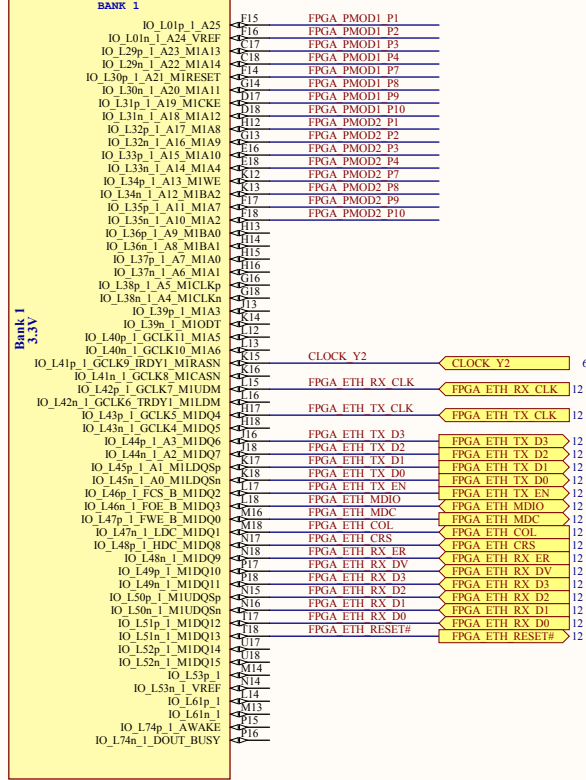
CLOCK_Y3 6



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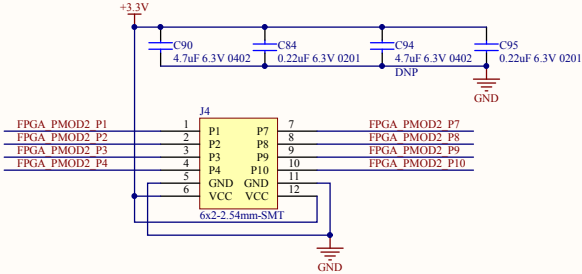
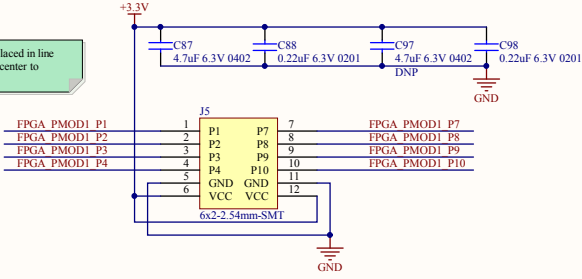
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Title: Sheet 4 - FPGA Bank 0	
Size: B	Document Number: SG-LX9-SCH-B
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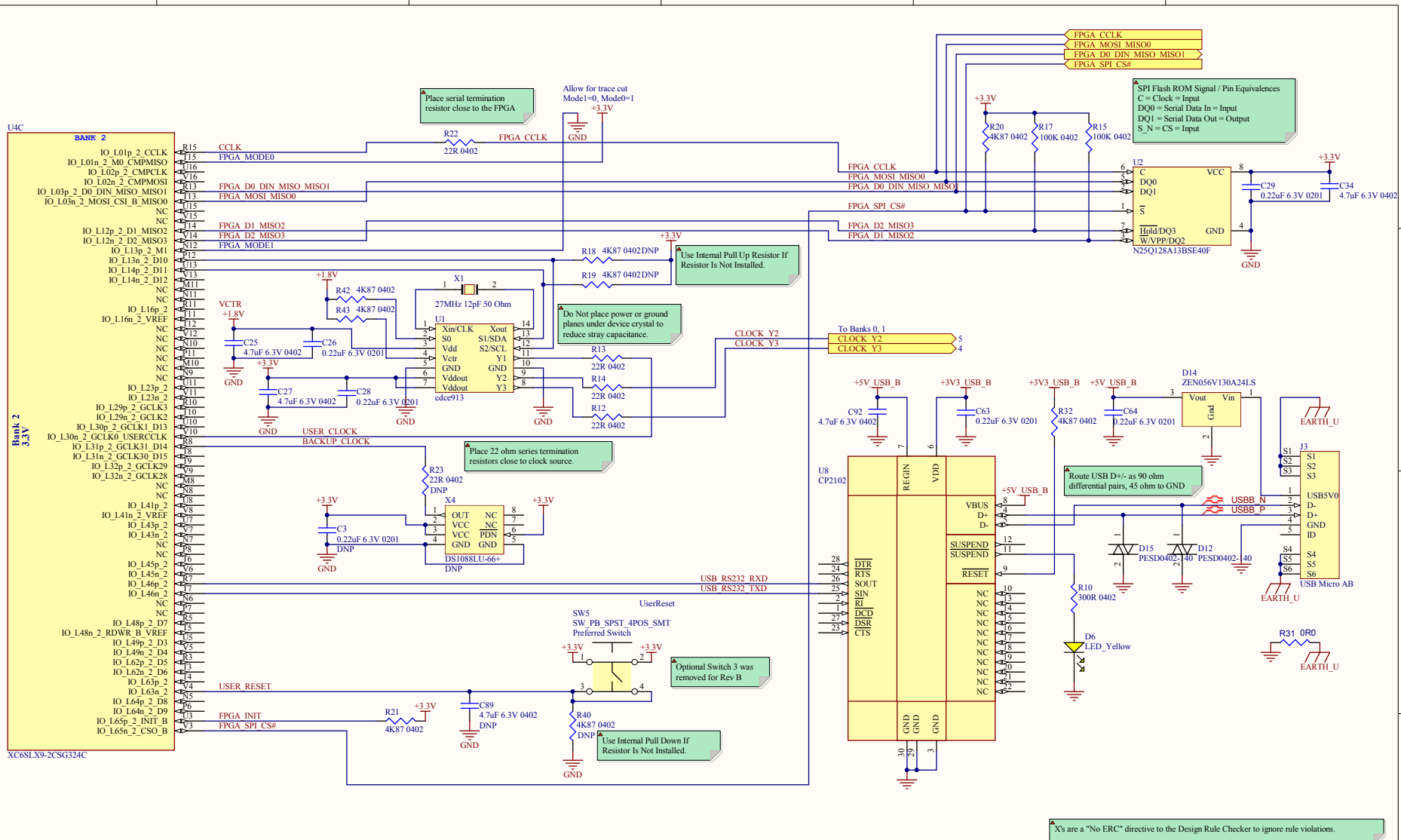


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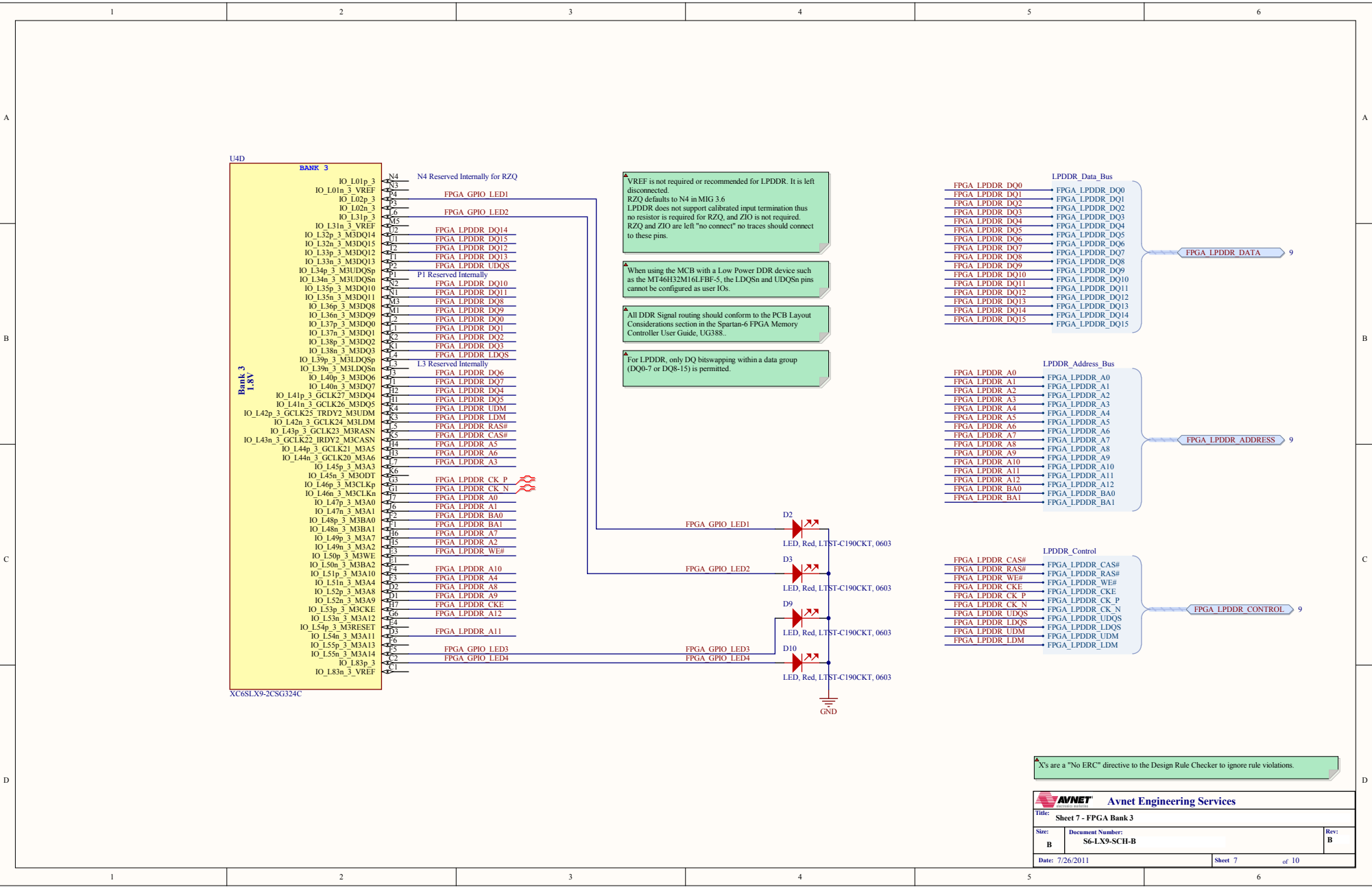
PMOD Headers must be placed in line with 400mil spacing pin 6 center to following pin 1 center.



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VREF is not required or recommended for LPDDR. It is left disconnected.
 RZQ defaults to N4 in MIG 3.6
 LPDDR does not support calibrated input termination thus no resistor is required for RZQ, and ZIO is not required.
 RZQ and ZIO are left "no connect" no traces should connect to these pins.

When using the MCB with a Low Power DDR device such as the MT46H32M16LFBF-5, the LDQSn and UDQSn pins cannot be configured as user I/Os.

All DDR Signal routing should conform to the PCB Layout Considerations section in the Spartan-6 FPGA Memory Controller User Guide, UG388.

For LPDDR, only DQ bitwapping within a data group (DQ0-7 or DQ8-15) is permitted.

- LPDDR Data Bus**
- FPGA LPDDR DQ0 → FPGA LPDDR_DQ0
 - FPGA LPDDR DQ1 → FPGA LPDDR_DQ1
 - FPGA LPDDR DQ2 → FPGA LPDDR_DQ2
 - FPGA LPDDR DQ3 → FPGA LPDDR_DQ3
 - FPGA LPDDR DQ4 → FPGA LPDDR_DQ4
 - FPGA LPDDR DQ5 → FPGA LPDDR_DQ5
 - FPGA LPDDR DQ6 → FPGA LPDDR_DQ6
 - FPGA LPDDR DQ7 → FPGA LPDDR_DQ7
 - FPGA LPDDR DQ8 → FPGA LPDDR_DQ8
 - FPGA LPDDR DQ9 → FPGA LPDDR_DQ9
 - FPGA LPDDR DQ10 → FPGA LPDDR_DQ10
 - FPGA LPDDR DQ11 → FPGA LPDDR_DQ11
 - FPGA LPDDR DQ12 → FPGA LPDDR_DQ12
 - FPGA LPDDR DQ13 → FPGA LPDDR_DQ13
 - FPGA LPDDR DQ14 → FPGA LPDDR_DQ14
 - FPGA LPDDR DQ15 → FPGA LPDDR_DQ15
- FPGA LPDDR DATA** 9

- LPDDR Address Bus**
- FPGA LPDDR A0 → FPGA LPDDR_A0
 - FPGA LPDDR A1 → FPGA LPDDR_A1
 - FPGA LPDDR A2 → FPGA LPDDR_A2
 - FPGA LPDDR A3 → FPGA LPDDR_A3
 - FPGA LPDDR A4 → FPGA LPDDR_A4
 - FPGA LPDDR A5 → FPGA LPDDR_A5
 - FPGA LPDDR A6 → FPGA LPDDR_A6
 - FPGA LPDDR A7 → FPGA LPDDR_A7
 - FPGA LPDDR A8 → FPGA LPDDR_A8
 - FPGA LPDDR A9 → FPGA LPDDR_A9
 - FPGA LPDDR A10 → FPGA LPDDR_A10
 - FPGA LPDDR A11 → FPGA LPDDR_A11
 - FPGA LPDDR BA0 → FPGA LPDDR_A12
 - FPGA LPDDR BA1 → FPGA LPDDR_BA0
- FPGA LPDDR ADDRESS** 9

- LPDDR Control**
- FPGA LPDDR CAS# → FPGA LPDDR_CAS#
 - FPGA LPDDR RAS# → FPGA LPDDR_RAS#
 - FPGA LPDDR WE# → FPGA LPDDR_WE#
 - FPGA LPDDR CK_E → FPGA LPDDR_CKE
 - FPGA LPDDR CK_P → FPGA LPDDR_CK_P
 - FPGA LPDDR CK_N → FPGA LPDDR_CK_N
 - FPGA LPDDR UDM → FPGA LPDDR_UDQS
 - FPGA LPDDR LDQS → FPGA LPDDR_UDQS
 - FPGA LPDDR LDM → FPGA LPDDR_LDM
- FPGA LPDDR CONTROL** 9

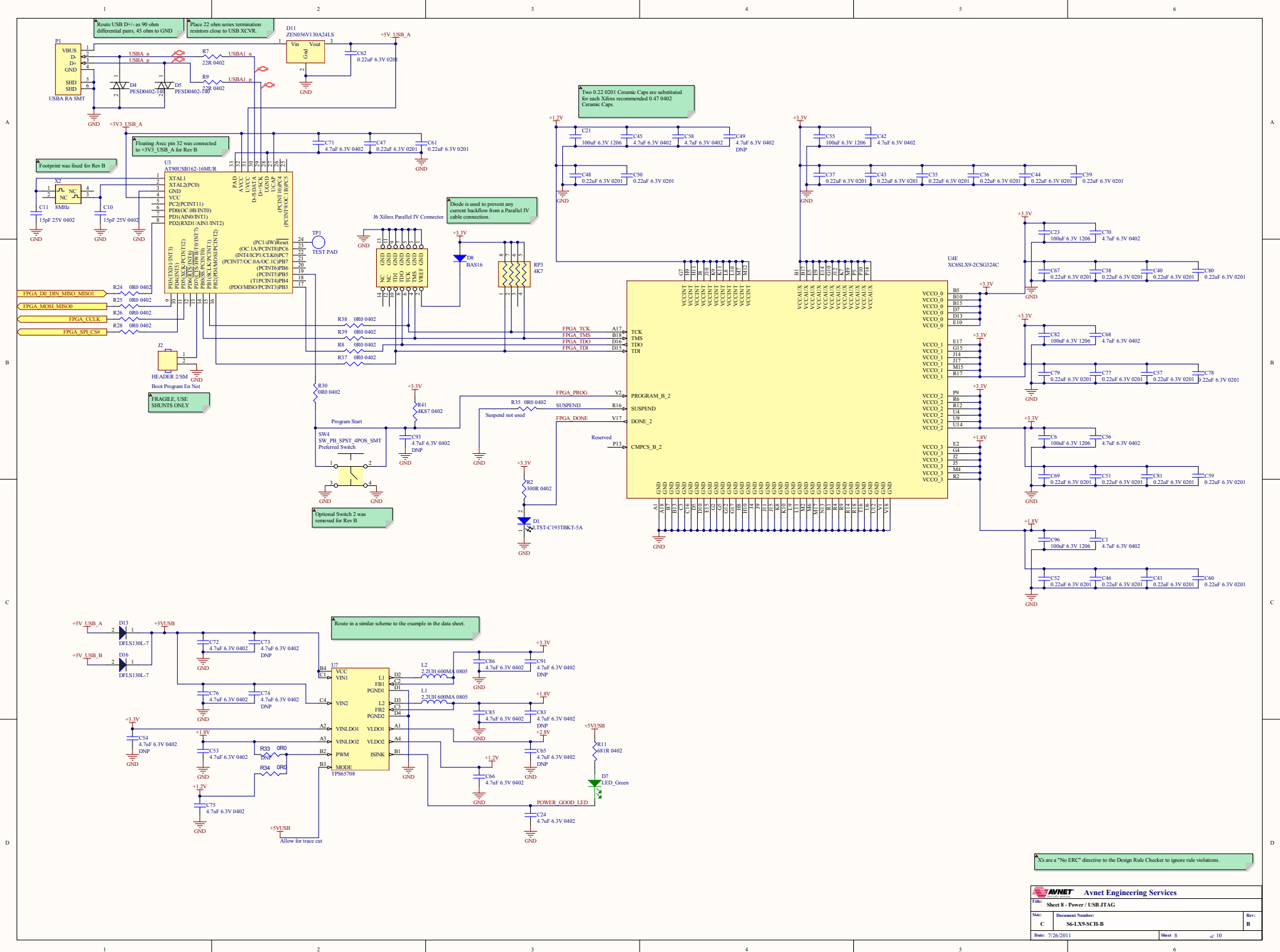
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Title: Sheet 7 - FPGA Bank 3

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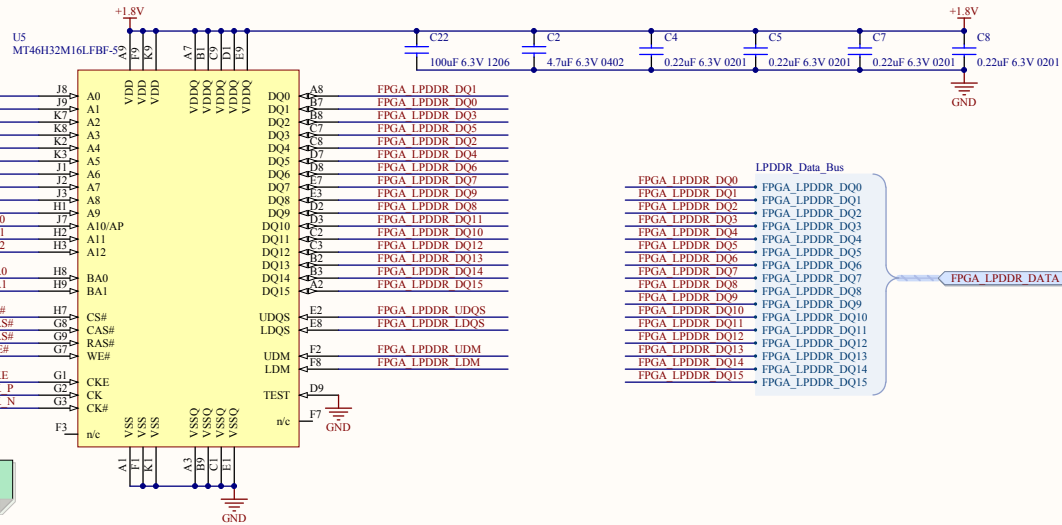
LPDDR Address Bus	
FPGA_LPDDR_A0	FPGA_LPDDR_A0
FPGA_LPDDR_A1	FPGA_LPDDR_A1
FPGA_LPDDR_A2	FPGA_LPDDR_A2
FPGA_LPDDR_A3	FPGA_LPDDR_A3
FPGA_LPDDR_A4	FPGA_LPDDR_A4
FPGA_LPDDR_A5	FPGA_LPDDR_A5
FPGA_LPDDR_A6	FPGA_LPDDR_A6
FPGA_LPDDR_A7	FPGA_LPDDR_A7
FPGA_LPDDR_A8	FPGA_LPDDR_A8
FPGA_LPDDR_A9	FPGA_LPDDR_A9
FPGA_LPDDR_A10	FPGA_LPDDR_A10
FPGA_LPDDR_A11	FPGA_LPDDR_A11
FPGA_LPDDR_A12	FPGA_LPDDR_A12
FPGA_LPDDR_BA0	FPGA_LPDDR_BA0
FPGA_LPDDR_BA1	FPGA_LPDDR_BA1

7 FPGA_LPDDR_ADDRESS

LPDDR Control	
FPGA_LPDDR_CAS#	FPGA_LPDDR_CAS#
FPGA_LPDDR_RAS#	FPGA_LPDDR_RAS#
FPGA_LPDDR_WE#	FPGA_LPDDR_WE#
FPGA_LPDDR_CKE	FPGA_LPDDR_CKE
FPGA_LPDDR_CK_P	FPGA_LPDDR_CK_P
FPGA_LPDDR_CK_N	FPGA_LPDDR_CK_N
FPGA_LPDDR_UDQS	FPGA_LPDDR_UDQS
FPGA_LPDDR_LDQS	FPGA_LPDDR_LDQS
FPGA_LPDDR_UDM	FPGA_LPDDR_UDM
FPGA_LPDDR_LDM	FPGA_LPDDR_LDM

7 FPGA_LPDDR_CONTROL

All DDR Signal routing should conform to the PCB Layout Considerations section in the Spartan-6 FPGA Memory Controller User Guide, UG388.



Place clock termination resistor as close as possible to MT46H32M16LFBF-5 LPDDR device.

LPDDR Data Bus	
FPGA_LPDDR_DQ0	FPGA_LPDDR_DQ0
FPGA_LPDDR_DQ1	FPGA_LPDDR_DQ1
FPGA_LPDDR_DQ2	FPGA_LPDDR_DQ2
FPGA_LPDDR_DQ3	FPGA_LPDDR_DQ3
FPGA_LPDDR_DQ4	FPGA_LPDDR_DQ4
FPGA_LPDDR_DQ5	FPGA_LPDDR_DQ5
FPGA_LPDDR_DQ6	FPGA_LPDDR_DQ6
FPGA_LPDDR_DQ7	FPGA_LPDDR_DQ7
FPGA_LPDDR_DQ8	FPGA_LPDDR_DQ8
FPGA_LPDDR_DQ9	FPGA_LPDDR_DQ9
FPGA_LPDDR_DQ10	FPGA_LPDDR_DQ10
FPGA_LPDDR_DQ11	FPGA_LPDDR_DQ11
FPGA_LPDDR_DQ12	FPGA_LPDDR_DQ12
FPGA_LPDDR_DQ13	FPGA_LPDDR_DQ13
FPGA_LPDDR_DQ14	FPGA_LPDDR_DQ14
FPGA_LPDDR_DQ15	FPGA_LPDDR_DQ15

FPGA_LPDDR_DATA 7

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