Tutorial for Digilent NEXYS 2 and Xilinx 12.3 with Linux/Debian

This tutorial was tested under Ubuntu 10.10.

1 Getting the software

What you need is:

- Xilinx ISE Design Suit 12 or later (WebPack License)
- UrJTAG (Universal JTAG library, server and tools) in version 0.10 or later (opensource)
- Digilent Adept Runtime in version 2.5.1 or later for Linux 32Bit/64Bit (free)
- Digilent Adept Utilities in version 2.1.1 or later for Linux 32Bit/64Bit (free)
- Digilent Plugin for Xilinx ISE 12 or later

1.1 Preparation of the operating system

```
Make sure you have following packages installed on your system:
sudo apt-get install libstdc++5 libmotif3 libxp6 libcurl3
```

```
For compiling software on your own you should have also done: sudo apt-get install build-essentials
```

1.2 Xilinx ISE

Starting Point for getting Xilinx is <u>http://www.xilinx.com/webpack/</u>. Select the free WebPack License Version and as a single download file.

A quick and fairly painless registration with Xilinx is required.

This is a huge download, a arround 2 GB if I remember correctly! Make sure you've got some time...

There is also a "Web Install Client", but that was much slower for me, and if you use it, the following procedure will be different.

Before you run the installation routine you must get needed runtime software. These packages should also be available for other distros, such as SuSE. sudo apt-get install fxload libftdil

Afterwards you can untar the downloaded single archive

```
tar xf FILENAME.tar
cd NEWDIRECTORY
```

```
and run
chmod +x ./xsetup
sudo ./xsetup
in the current installation directory to the final destination /opt/Xilinx/12.X/.
```

1.3 UrJTAG

This package conflicts with the UrJTAG tools that we will install in the next step, and development has been discontinued in favor of UrJTAG anyway. sudo apt-get remove openwince-jtag

You can download from http://urjtag.sourceforge.net/ the newest version and compile it your self.

```
tar xzf urjtag-VERSION.tar.gz
cd urjtag-VERSION
./configure
make
sudo make install
```

Currently we have created a binary package for debian based systems in version 0.10 of UrJTAG for 32Bit, so for the lazy one: sudo dpkg -i urjtag_0.10-1_i386.deb

1.4 Digilent Adept

The three Packages listed above you can get from <u>www.digilentinc.com</u> under the section products/software. Then you must uncompresse the Runtime firstly, then the Utilities and execute in each directory case

```
sudo bash install.sh
```

with only hitting enter to set default configuration and paths.

Then you get the Xilinx Plugin right by copying the whole directory, for example:

```
cp
(from)
./libCseDigilent_[*version*]-i686/ISE[*correspond-version*]/plugin
(to)
/opt/Xilinx/12.1/ISE_DS/ISE/lib/lin/plugins/Digilent/libCseDigilent
```

2 Programming with JTAG over USB with Xilinx

After you have successfully compiled and generated your bit file in your Project in Xilinx ISE, you can start the Impact Tool in the menue..



Xilinx Impact is used to download FPGA bitstreams to FPGA boards. (Ignore the starting error message for the programmer chain initialisation.)

Select a new project, set up like in the screenshot below and make okey:

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Second impact Flows Second (III)		
SystemACE		
E Create PROM File (PROM File Form		
	Welcome to iMPACT S S	
	Please select an action from the list below	
	Configure devices using Boundary-Scan (JTAG)	
	Enter a Boundary-Scan chain manually	
	O Prepare a PROM File	
	O Prepare a System ACE File	
	O Prepare a Boundary-Scan File	
	SVF	
impact Processes		
	OK	
	Console	
Welcome to iMPACT		
iMPACT Version: 12.1		
Console 🛛 Errors 🦄 Warnings		

The following steps show how to use Impact with the Plug-in. Select "Output Cable Setup..." menu item.



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Available Operations are:	Communication Mode Parallel Cable III Parallel Cable III Parallel Cable IV Advanced USB Cable Setup TCK Speed/Baud Rate: Port Default Speed Cable Location Cable Location Host Name: Cable Plug-in K [Open Cable Plug-in. Select or enter a Plug-in from the list belof digilent_plugin OK Cancel Help	
	Boundary Scan	
Cable connection failed. PROGRESS_END - End Operation. Elapsed time = 4 sec.		
Console 🙆 Errors 🔔 Warnings	No Cable Connection No File	Open

Select or enter manually the **digilent_plugin** in the input box

then you must initialisate the JTAG boundary scan chain:

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Boundary Scan SystemACE Create PROM File (PROM File Form		
	Add Xilinx Device Ctrl+D	
	Add <u>N</u> on-Xilinx Device Ctrl+K	
	Initialize Chain Ctrl+I	
	<u>C</u> able Auto Connect	
	Cable Setup	
	Output File Type	
	Right click to Add Device or Initialize JTAG chain	
iMPACT Processes		
Available Operations are:		
	😵 Boundary Scan 🗵	
	Console	
INFO: iMPACT - Digilent Plugin	Firmware Version: 0303	<u> </u>
(INFO: iMPACT - Digilent Plugin	JTAG Port Number: 0 JTAG Clock Frequency: 1600000 Hz	
Charles in Ref - Digitene Flagin	Siko cieck Frequency. 100000 Hz	
Console 💟 Errors 🥼 Warnings		
		Configuration Onboard USB 1600000

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IMPACT Frocesses Available Operations are: Get Device Signature/Usercode Read Device Status	Image: Second secon	
	😵 Boundary Scan	
	Console	
PROGRESS_END - End Operation. Elapsed time = 8 sec.		
// *** BATCH CMD : identifyMPH	м	
		Ē
Console Errors A Warnings		

You will be asked for a bit file that you have compiled for the board, so click okey and select one:

Maybe you have also a not necessary PROM file to transfare it via SPI, we say no and continue to the end changing nothing.

Now you can download your Code to the Digilent Nexys 2 Board out of Xilinx by double clicking on Programm. I hope this tutorial served you well.

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