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Eliminating I/O Coupling Effects when Interfacing Large-Swing Single-Ended Signals to User I/O Pins on Spartan-3 Families

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Summary

The Spartan®-3 families, consisting of Spartan-3, Spartan-3E, and Extended Spartan-3A devices, support an exceptionally robust and flexible I/O feature set, such that the signaling requirements of most applications can easily be met. It is possible to program User I/O pins of these families to handle many different single-ended signal standards. The standard single-ended signaling voltage levels are 1.2V, 1.5V, 1.8V, 2.5V, and 3.3V.

There are a number of applications for which it is desirable to receive signals with a greater voltage swing than User I/O pins ordinarily permit. The most common use case is receiving 5.0V signals on User I/O pins that are powered for use with one of the standard single-ended signaling levels listed above. In this application note, such signals are referred to as large-swing signals. Large-swing signals might be received by design or might be applied to the User I/O unintentionally from severe positive and/or negative overshoot. The cases of severe positive and/or negative overshoot can occur regardless of the programmed “direction” of a User I/O pin.

This application note describes solutions to receive large-swing signals by design. In one solution (and in the general case of severe positive and/or negative overshoot), parasitic leakage current between User I/O in differential pin pairs might occur, even though the User I/O pins are configured with single-ended I/O standards. This application note addresses the parasitic leakage current behavior that occurs outside the recommended operating conditions. This parasitic leakage can also occur within the recommended operating conditions in cases of undershoot below –0.2V. For more details on parasitic leakage within the recommended operating conditions, refer to the “Parasitic Leakage” section in UG331, *Spartan-3 Generation FPGA User Guide*.

For the specific case of interfacing to the PCI™ bus, see XAPP457, *Powering and Configuring Spartan-3 Generation FPGAs in Compliant PCI Applications*. PCI Bus applications use bidirectional signaling and have unique requirements, which are addressed in XAPP457 and its supporting references.

Overview of I/O Pin Types

User I/O pins are assigned to signals of the design programmed into the FPGA. These pins are only active when the FPGA operates in user mode. Before then, during configuration, they are either in a high impedance state or weakly pulled up. User I/O pins are organized in banks around the perimeter of the die. Each Spartan-3 device has eight banks, while Spartan-3E and Extended Spartan-3A (Spartan-3A, Spartan-3AN, and Spartan-3A DSP) devices have four banks. An independent V_{CCO} rail per bank (for example, VCCO_0, VCCO_1, etc.) powers the output buffers associated with the User I/O pins in each bank. User I/O input buffers are powered by V_{CCO}, V_{CCINT}, or V_{CCAUX}, depending on the device family and the signal standard in use.

Dual-purpose pins function as specific configuration-related signals before entry into user mode; afterwards, they become User I/O pins. The power sources for these pins are the same as for User I/O pins, and for the purposes of this application note, they can be considered as User I/O pins.

Dedicated pins perform unique functions that are always active during configuration. Such functions include configuration-related signals (for example, PROG_B, DONE, etc.) and JTAG pins (for example, TDI, TMS, TCK, and TDO). Some of these pins retain their functions in user mode. These pins require special analysis for interfacing to large-swing signals. Dedicated pins

are not addressed in this application note, but are discussed in UG332, *Spartan-3 Generation Configuration User Guide* and XAPP453, *The 3.3V Configuration of Spartan-3 FPGAs*.

Structures and Specifications of User I/O

This section briefly describes the Input-Output Block (IOB) of the Spartan-3 families.

Structures

Figure 1 shows a simplified portion of the IOB that is effectively the same for both the Spartan-3 and Spartan-3E families. The bidirectional User I/O pin connects to input buffers and output buffers. A ground diode lies between the I/O pin and GND. A power diode lies between the I/O pin and V_{CCO}. This pair of diodes provides ESD protection for the User I/O pin. These diodes are present on all User I/O pins all of the time. These diodes simplify interfaces with large-swing signals, but they complicate hot-swap interfaces. For recommendations on hot-swap capability, refer to the section on hot-swap in the "Powering Spartan-3 Generation FPGAs" chapter in UG331, *Spartan-3 Generation FPGA User Guide*.

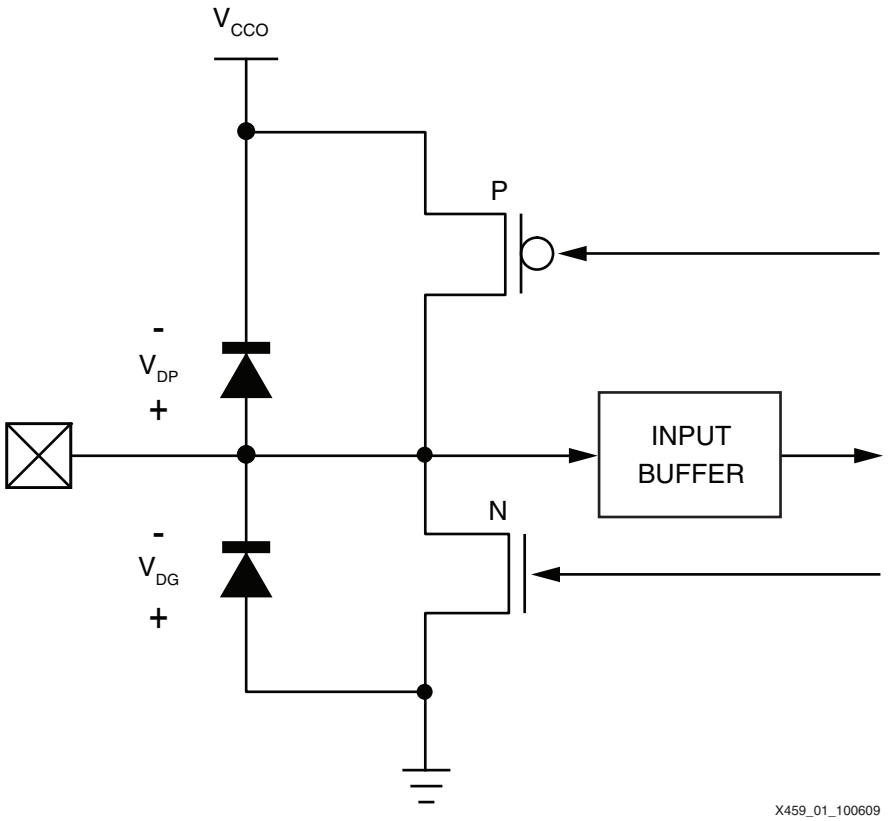

Figure 1: **Simplified IOB Diagram for Spartan-3 and Spartan-3E FPGAs**

Figure 2 shows a simplified portion of the IOB that is effectively the same for the Extended Spartan-3A families. These devices employ a floating N-well in the design of each User I/O pin. The bidirectional User I/O pin connects to input buffers and output buffers. A ground diode lies between the I/O pin and GND. There is no dedicated power diode connected to V_{CCO}. A proprietary circuit and the ground diode provide ESD protection. A programmable clamp diode exists specifically for PCI Bus applications, but it is normally disabled. The absence of a power diode simplifies hot-swap interfaces, but complicates interfaces with large-swing signals.

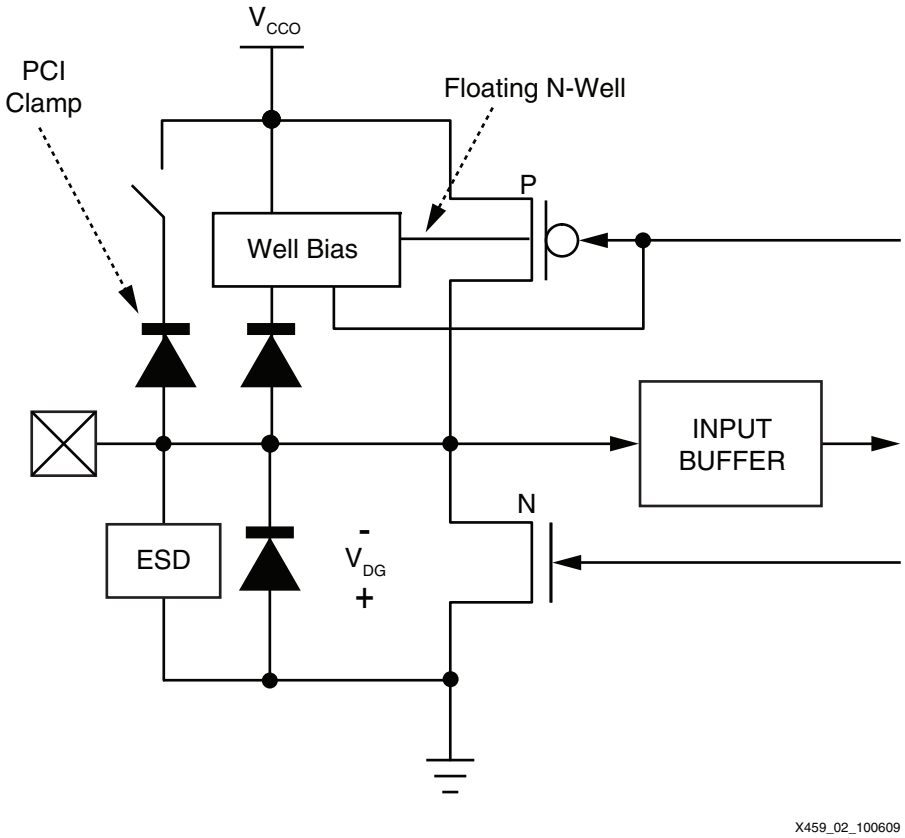

Figure 2: **Simplified IOB Diagram for Extended Spartan-3A FPGAs**

Specifications

To design for success, it is critical to understand the electrical specifications of User I/O pins. When applying large-swing signals to User I/O pin inputs, logic level requirements are easily met. Nevertheless, several important device specifications must be taken into account.

Table 1 shows a relevant portion of the general recommended operating conditions for Spartan-3 FPGAs (see DS099, *Spartan-3 FPGA Family Data Sheet*). The recommended voltage range for V_{CCO} spans from 1.140V to 3.465V. Further, the recommended voltage range for signals applied to User I/O pins, V_{IN}, spans from –0.3V to (V_{CCO} + 0.3V), with a cap at 3.75V. Observing these general recommended operating conditions conservatively ensures that the power diode and ground diode are off. While not required, it is recommended that the power diode and ground diode remain off during normal device operation.

Table 1: **General Recommended Operating Conditions for Spartan-3 FPGAs**

Symbol	Description		Min	Nom	Max	Units
V_{CCO} (1)	Output driver supply voltage		1.140	-	3.465	V
V_{IN} (2)	Voltage applied to all User I/O pins and Dual-Purpose pins relative to GND (3)	V_{CCO} = 3.3V	–0.3	-	3.75	V
		$V_{CCO} \leq$ 2.5V	–0.3	-	V_{CCO} + 0.3 (3)	V
	Voltage applied to all Dedicated pins relative to GND		–0.3	-	V_{CCAUX} + 0.3	V

Notes:

1. The V_{CCO} range given here spans the lowest and highest operating voltages of all supported I/O standards.
2. Input voltages outside the recommended range is permissible provided that the I_{IK} input diode clamp diode rating is met.
3. Each of the User I/O and Dual-Purpose pins is associated with one of the V_{CCO} rails. Meeting the V_{IN} limit ensures that the internal diode junctions that exist between these pins and their associated V_{CCO} and GND rails do not turn on. The absolute maximum rating is provided in Table 2.

Footnote 3 of Table 1 describes the conditions under which it is permitted to forward bias the power and ground diodes, and cites parameters from Table 2. Table 2 shows a relevant portion of the absolute maximum ratings for Spartan-3 FPGAs. This table shows the absolute maximum voltages that can be applied to User I/O pins: $-0.95V \leq V_{IN} \leq 4.4V$ for commercial grade devices, and $-0.85V \leq V_{IN} \leq 4.3V$ for industrial grade devices. Table 2 also sets a limit on the maximum current allowed through the power and ground diodes when they are forward biased, I_{IK}, which is 100 mA.

Footnote 2 of Table 2 specifies the range of V_{IN} for which the diodes will not conduct significant forward current. That range is $-0.5V < V_{IN} < (V_{CCO} + 0.5V)$. The footnote also specifies a limit on the number of User I/O pins that are allowed to simultaneously exceed the general recommended operating conditions for V_{IN}.

Table 2: **Absolute Maximum Ratings(1) for Spartan-3 FPGAs**

Symbol	Description	Conditions		Min	Max	Units
V_{IN}	Voltage applied to all User I/O pins and Dual-Purpose pins relative to GND(2)	Driver in a high-impedance state	Commercial	–0.95	4.4	V
			Industrial	–0.85	4.3	V
	Voltage applied to all Dedicated pins relative to GND		All temp. ranges	–0.5	V_{CCAUX} + 0.5	V
I_{IK}	Input clamp current per I/O pin	$-0.5\ V < V_{IN} < (V_{CCO} + 0.5\ V)$		-	±100	mA

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time adversely affects device reliability.
2. All User I/O and Dual-Purpose pins (DIN/D0, D1–D7, CS_B, RDWR_B, BUSY/DOUT, and INIT_B) draw power from the V_{CCO} power rail of the associated bank. Keeping V_{IN} within 500 mV of the associated V_{CCO} rails or ground rail ensures that the internal diode junctions that exist between each of these pins and the V_{CCO} and GND rails do not turn on. Table 1 specifies the V_{CCO} range used to determine the maximum limit. Input voltages outside the –0.5V to V_{CCO}+0.5V voltage range are permissible provided that the I_{IK} input clamp diode rating is met and no more than 100 pins exceed the range simultaneously. The V_{IN} limits apply to both the DC and AC components of signals. Simple application solutions are available that show how to handle overshoot/undershoot as well as achieve PCI compliance. Refer to these application notes: **XAPP457**, *Powering and Configuring Spartan-3 Generation FPGAs in Compliant PCI Applications* and **XAPP659**, *Using 3.3V I/O Guidelines in a Virtex®-II Pro Design*.

Table 3 shows a relevant portion of the general recommended operating conditions for Spartan-3E FPGAs (see DS312, *Spartan-3E FPGA Family: Data Sheet*). The recommended voltage range for V_{CCO} spans from 1.100V to 3.450V. Further, the recommended voltage range for signals applied to User I/O pins, V_{IN}, spans from –0.5V to (V_{CCO} + 0.5V). Observing these general recommended operating conditions conservatively ensures that the power diode and ground diode are off. While not required, it is recommended that the power diode and ground diode remain off during normal device operation.

Table 3: **General Recommended Operating Conditions for Spartan-3E FPGAs**

Symbol	Description		Min	Nominal	Max	Units
V_{CCO}(1)	Output driver supply voltage		1.100	-	3.450	V
V_{IN}(2,3)	Input voltage extremes to avoid turning on I/O protection diodes.	I/O, Input-only, and Dual-Purpose pins(2)	–0.5	–	V_{CCO} + 0.5	V
		Dedicated pins	–0.5	–	V_{CCAUX} + 0.5	V

Notes:

1. This V_{CCO} range spans the lowest and highest operating voltages for all supported I/O standards.
2. Each of the User I/O and Dual-Purpose pins is associated with one of the four banks' V_{CCO} rails. Meeting the V_{IN} limit ensures that the internal diode junctions that exist between these pins and their associated V_{CCO} and GND rails do not turn on. The absolute maximum rating is provided in Table 2.
3. Input voltages outside the recommended range is permissible provided that the I_{IK} input diode clamp diode rating is met.

Footnote 3 of Table 3 describes the conditions under which it is permitted to forward bias the power and ground diodes, and cites parameters from Table 4. Table 4 shows a relevant portion of the absolute maximum ratings for Spartan-3E FPGAs. This table shows the absolute maximum voltages that can be applied to User I/O pins; $-0.95V \leq V_{IN} \leq 4.4V$ for commercial grade devices, and $-0.85V \leq V_{IN} \leq 4.3V$ for industrial grade devices. Table 4 also sets a limit on the maximum current allowed through the power and ground diodes when they are forward biased, I_{IK}, which is 100 mA.

Table 4: **Absolute Maximum Ratings for Spartan-3E FPGAs**

Symbol	Description	Conditions		Min	Max	Units
V_{IN}(1,2)	Voltage applied to all User I/O pins and Dual-Purpose pins	Driver in a high-impedance state	Commercial	–0.95	4.4	V
			Industrial	–0.85	4.3	V
	Voltage applied to all Dedicated pins		All temp. ranges	–0.5	V_{CCAUX} + 0.5	V
I_{IK}	Input clamp current per I/O pin	$-0.5\ V < V_{IN} < (V_{CCO} + 0.5\ V)$		-	±100	mA

Notes:

1. Each of the User I/O and Dual-Purpose pins is associated with one of the four banks' V_{CCO} rails. Keeping V_{IN} within 500 mV of the associated V_{CCO} rails or ground rail ensures that the internal diode junctions do not turn on. Table 3 specifies the V_{CCO} range used to evaluate the maximum V_{IN} voltage.
2. Input voltages outside the –0.5V to V_{CCO} + 0.5V voltage range are permissible provided that the I_{IK} input diode clamp diode rating is met and no more than 100 pins exceed the range simultaneously.

Footnote 1 of Table 4 specifies the range of V_{IN} for which the diodes will not conduct significant forward current. That range is $-0.5\ V < V_{IN} < (V_{CCO} + 0.5\ V)$. Footnote 2 of Table 4 specifies a limit on the number of User I/O pins that are allowed to simultaneously exceed the general recommended operating conditions for V_{IN}.

Table 5 shows a relevant portion of the general recommended operating conditions for Extended Spartan-3A FPGAs (see DS529, *Spartan-3A FPGA Family: Data Sheet*, DS557, *Spartan-3AN FPGA Family Data Sheet*, and DS610, *Spartan-3A DSP FPGA Family: Data Sheet*). The recommended voltage range for V_{CCO} spans from 1.100V to 3.600V.

Table 5: **General Recommended Operating Conditions for Extended Spartan-3A FPGAs**

Symbol	Description		Min	Nominal	Max	Units
V_{CCO}(1)	Output driver supply voltage		1.100	-	3.600	V
V_{IN}(2)	Input voltage extremes	I/O, Input-only, and Dual-Purpose pins(2)	–0.5	-	4.1	V
		Dedicated pins	–0.5	-	V_{CCAUX} + 0.5	V

Notes:

1. This V_{CCO} range spans the lowest and highest operating voltages for all supported I/O standards.
2. Each of the User I/O and Dual-Purpose pins is associated with one of the four banks' V_{CCO} rails. The absolute maximum rating is provided in Table 6.

Table 6 shows a relevant portion of the absolute maximum ratings for Extended Spartan-3A FPGAs, and shows the absolute maximum voltages that can be applied to User I/O pins: $-0.95V \leq V_{IN} \leq 4.6V$.

Table 6: **Absolute Maximum Ratings for Extended Spartan-3A FPGAs**

Symbol	Description	Conditions	Min	Max	Units
V_{IN}	Voltage applied to all User I/O pins and Dual-Purpose pins	Driver in a high-impedance state	–0.95	4.6	V
	Voltage applied to all Dedicated pins		–0.5	4.6	V

Solution 1: Voltage Level Translators

Xilinx recommends the use of voltage level translators as the preferred solution when interfacing with large-swing signals. A voltage level translator is a circuit that converts a signal from one signaling voltage to another. Voltage level translators can be unidirectional or bidirectional and they offer direct solutions to interfacing with large-swing signals. Voltage level translators work with all Xilinx® FPGAs.

A voltage level translator can be as simple as a two-resistor voltage divider, a unidirectional solution that is both simple and inexpensive. At the other end of the spectrum, a voltage level translator can be as complex as a transparent PCI-to-PCI bridge, a bidirectional solution often used to connect PCI Bus devices that employ different signaling voltages when strict adherence to the PCI Local Bus Specification is required.

Due to the increase in the number of mixed-voltage system designs, the available selection of voltage level translators has grown dramatically. Table 7 shows a survey of low-cost solutions originally published in SCYB018A, *Translation Guide* by Texas Instruments Inc. Texas Instruments Inc. offers a full spectrum of products to implement voltage level translation. Other vendors also offer voltage level translation products.

Table 7: **Voltage Level Translation Solutions (Courtesy Texas Instruments Inc.)**

Solution	Up-Translate	Down-Translate	Provides Output Drive	Power Consumption
Dual-supply level translators	Yes	Yes	Yes	Good
FET switches	Yes	Yes	No	Good(1)
Overvoltage-tolerant devices	No	Yes	Yes	Good
Devices with open-drain outputs	Yes	Yes	Yes	Not optimal
Devices with TTL inputs and CMOS outputs	Yes(2)	No	Yes	Not optimal

Notes:

1. Varies depending on type of FET switch and application.
2. LVCMOS33/LVTTL to 5.0V CMOS only.

Each of the approaches listed in Table 7 has different merits. To make the best selection, the attributes shown in Table 7 should be evaluated along with switching performance, voltage range, component cost, and PCB area requirements.

The required switching performance and voltage range is dictated by the application. While evaluating interfacing solutions, the designer must understand the signaling standards in use, along with any applicable timing budgets that apply to the interface. Voltage-level translators must be selected that solve the problem and fit in the timing budget. Component cost and added PCB area are two frequently cited disadvantages of voltage translators. This might be true if an alternative exists that does not require external components, but the reality of interfacing with large-swing signals is that external components are generally required.

The least expensive voltage translation solution is a passive voltage divider consisting of two resistors. This implementation might only cost a couple of cents in high volume; the only PCB area required is for two resistor footprints. Higher performance active solutions, such as the Texas Instruments SN74LVC2G34 Dual Buffer Gate, are slightly more expensive, but still only about five cents per signal (based on current DigiKey pricing). If PCB area is at a premium, the SN74LVC2G34 Dual Buffer Gate is offered in a tiny die-size ball grid array at a nominally higher price.

An excellent guide to voltage level translation is available in SCEA035A, *Selecting the Right Level-Translation Solution*, by Texas Instruments Inc.

Solution 2: Open-Drain Interfacing

Open-drain interfacing is shown in Table 7 as one of several voltage level translation solutions, but this technique merits additional discussion. In many cases, open-drain interfacing might be possible without requiring additional components at all. While this technique does not directly enable the application of a large-swing signal to a User I/O pin, it is a viable design alternative for moderate to low performance signaling requirements and is applicable to all Spartan-3 families.

Various integrated circuits (for example, embedded processors) offer options to configure data pins as either totem-pole outputs or open-drain outputs. An open-drain output buffer is configured to only sink current for a low voltage level. Therefore, to provide a high voltage level, the output needs a pull-up resistor. This pull-up resistor can be an external resistor or the programmable pull-up resistor that is present in all User I/O pins. This interfacing technique can be used to a convert what might otherwise have been a large-swing signal into one with a smaller swing.

Figure 3 shows an example of a device with an open-drain output connected to a Spartan-3 FPGA. The supply voltage used by the device with the open-drain output is of no concern, because the output driver only drives Low. The pull-up resistor is connected from the open-drain output driver to the V_{CCO} supply powering the User I/O pin in the FPGA. As a result, the signal on this line can only rise as high as V_{CCO} for a high voltage level. A power diode is shown for the FPGA device in Figure 3. It is shaded gray to indicate that it might not be present, but if it is present, it is off. Both C_{IN} and C_{OUT} are lumped models of the pin capacitance for each device.

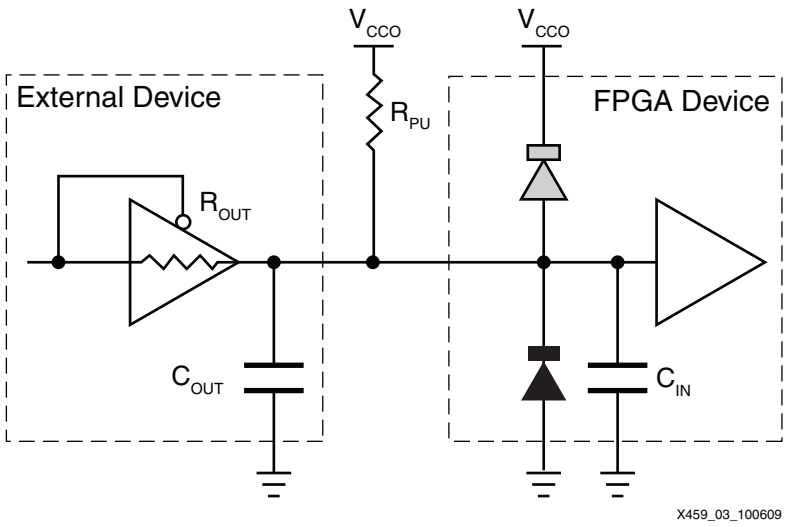

Figure 3: **Open-Drain Interfacing**

The transition from a low voltage level to a high voltage level is gentle due to the time constant of the RC network formed by C_{OUT} and C_{IN} connected to the relatively high impedance of the pull-up resistor R_{PU}. The value of R_{PU} influences the rise time and is commonly between 2.5KΩ and 10KΩ — selected to be a substantially higher resistance than R_{OUT} (typically by one to two orders of magnitude). For this reason, open-drain interfaces are best for moderate to low performance signaling requirements.

The transition from a high voltage level to a low voltage level will be considerably sharper because an active driver is used. The output driver is enabled, creating an additional low impedance path to ground through R_{OUT}. Where possible, it is desirable to reduce unwanted negative overshoot during the transition by selection of R_{PU} and R_{OUT}. Static power is consumed during the low voltage steady state from current V_{CCO} to ground through (R_{PU} + R_{OUT}).

The following example illustrates the calculation of several key points for an application of an open-drain interface to a Spartan-3E FPGA using a V_{CCO} of 3.3V with the User I/O configured

for LVCMOS33 operation. In this mode, V_{IL}, max = 0.8V, V_{IH}, min = 2.0V, and C_{IN} = 10 pF. For the external device, assume C_{OUT} = 5 pF and R_{OUT} = 50Ω, with the external R_{PU} = 2.5 KΩ.

Static power: $P = V_{CCO}^2 / (R_{OUT} + R_{PU}) = 4.27$ mW

Approximate Rise Time: $t = -R_{PU} * (C_{OUT} + C_{IN}) * \ln(1 - (V_{IH} / V_{CCO})) \approx$ 35 ns

Approximate Fall Time: $t = -R_{TH} * (C_{OUT} + C_{IN}) * \ln((V_{IL} - V_{TH}) / (V_{CCO} - V_{TH})) \approx$ 1.1 ns

The PCB trace characteristics have been ignored. For the fall time approximation, the Thevenin equivalent of the output driver and the external pull-up resistor is used, but for many practical cases, the effect of the external pull-up on the fall time is negligible if R_{PU} is significantly larger than R_{OUT}.

Solution 3: Voltage Clamps Using Internal Diodes

For Spartan-3 and Spartan-3E devices with both power and ground diodes, another solution is possible. This solution leverages the power and ground diodes to work as voltage clamps. To use the diodes in this manner, external resistors and some careful analysis are required. It is a viable technique for low performance signaling requirements.

Caution! Do not use this technique with Extended Spartan-3A FPGAs. Permanent damage might occur as a result of exceeding the absolute maximum ratings because these devices have a different I/O structure that will not work as a voltage clamp.

Note: Xilinx recommends designers clearly describe any application of this technique, including its limitations, on relevant design documentation, such as a PCB schematic. This reduces the potential for error if the design is later retargeted to an Extended Spartan-3A FPGA.

The following example illustrates the application of this technique by showing how to apply a 5.0V large-swing signal to a Spartan-3E FPGA User I/O pin, which is by far the most common use case. The same approach used to achieve 5.0V tolerance can also be used to seek solutions for still higher voltages. The circuit solution is essentially the same although the external resistor values are different.

For Spartan-3E FPGAs, the recommended V_{IN} limit is V_{CCO} + 0.5V. For this reason, it makes sense to select an I/O configuration that results in the highest possible voltage for V_{CCO}. An appropriate choice is LVCMOS33 or LVTTL, both of which require a typical V_{CCO} of 3.3V. This minimizes the voltage developed across the power diode, keeping the diode current smaller than it would be for other I/O configurations that use lower voltages for V_{CCO}. For the purposes of this example, it is assumed the large-swing signal is ground referenced (which is typically the case for single-ended signals) so that the ground diode will never be forward biased. Setting V_{CCO} = 3.3V, it follows that:

$V_{IN} < V_{CCO} + 0.5V$

$V_{IN} < 3.3V + 0.5V$

$V_{IN} < 3.8V$

With an external device driving 5.0V applied to a User I/O pin, both the recommended and absolute maximum values for V_{IN} are violated. The voltage across the power diode is $V_{IN} - V_{CCO} = 5.0V - 3.3V = 1.7V$. Per Footnote 1 of Table 4, the power diode will be strongly forward biased and an unacceptable amount of current will result, violating I_{IK}. Of secondary concern, the power diode acts as a charge pump, injecting current into the V_{CCO} rail which can often cause many voltage regulation solutions to fail.

To permit the Spartan-3E FPGA to operate within specifications, it is important to protect the input from exposure to unacceptably high voltage as well as control the diode current. Any reverse current into the V_{CCO} supply must also be managed. It is possible to achieve these goals simply by adding a few resistors to the design.

Seeking a Solution

Any solution that permits an external device to drive a large-swing signal on a User I/O pin, such that the power diode turns on, must meet three conditions:

1. V_{IN} must not exceed the absolute maximum rating of the device.
2. The diode current must not exceed 10 mA. Although the absolute maximum rating for I_{IK} is 100 mA, prolonged exposure to such current might compromise device reliability. A sustained current of 10 mA will not compromise device reliability.
3. The diode current, a reverse current into V_{CCO}, must not adversely affect V_{CCO} regulation.

The next section shows how to use load-line analysis to iteratively find a solution that simultaneously satisfies conditions 1 and 2. This solution takes the form of a series resistor, R_{SER}, that is connected between the signal source and the User I/O pin. See "Managing the Reverse Current", page 14, for information on how to meet condition 3, essentially by connecting a parallel resistor (R_{PAR}) from the V_{CCO} regulator output to ground.

Controlling the Diode Current and Protecting the Input

Putting a resistor (R_{SER}) in series with the User I/O pins helps limit the power diode current to 10 mA or less (condition 2) as well as keep V_{IN} under the absolute maximum rating (condition 1). Figure 4 shows R_{SER} connected to the User I/O pins. Looking in "through the User I/O pins," both the driver and input buffer are in a high impedance state and can be ignored in the analysis that follows. C_{IN} is a lumped model of the User I/O pin capacitance.

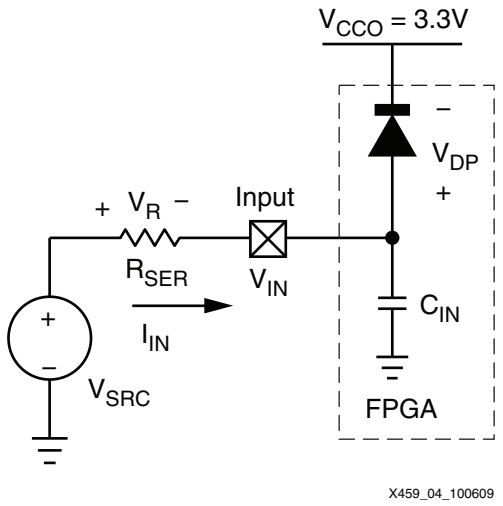

Figure 4: **External Device Driving Large-Swing Signal on User I/O**

A high logic level from the external device's output is modeled as a voltage source V_{SRC} with a value of 5.0V ±10% for the purposes of this example. As previously mentioned, using the highest reasonable V_{CCO} level reduces the potential voltage V_{DP} across the power diode, which also serves to reduce the diode current. For this example, the User I/O pin is configured for LVCMOS33 and V_{CCO} is nominally 3.3V.

Determining R_{SER} involves solving a system of two current-voltage relationships. One is the V-I characteristic of the power diode. The other is a voltage loop equation that includes R_{SER}, the unknown variable.

The IBIS file for the Spartan-3E FPGA is a useful source of information about the diode characteristics. The IBIS file can be opened and read as a text file. The "POWER_clamp" section is a table of current and voltage numbers that describe the power diode. For each V_{DP} value in the left-hand column, there are minimum, typical, and maximum currents given in the columns to the right.

The graphical analysis shown in Figure 5 through Figure 8 uses a POWER_clamp table extracted from the Spartan-3E FPGA IBIS file. The data is taken from the LVCMOS33_S_12 model and reprinted in Table 8.

Table 8: **Spartan-3E FPGA Power Diode Data for LVCMOS33_S_12 (IBIS File XC3SE.IBS)**

Voltage	I (typ)	I (min)	I (max)
–3.3	3.14A	2.52A	3.53A
–3.2	3.01A	2.42A	3.38A
–3.1	2.88A	2.32A	3.24A
–3	2.75A	2.22A	3.09A
–2.9	2.62A	2.12A	2.94A
–2.8	2.49A	2.02A	2.80A
–2.7	2.36A	1.92A	2.65A
–2.6	2.23A	1.82A	2.50A
–2.5	2.10A	1.72A	2.35A
–2.4	1.97A	1.62A	2.21A
–2.3	1.85A	1.52A	2.06A
–2.2	1.72A	1.42A	1.91A
–2.1	1.59A	1.32A	1.77A
–2	1.46A	1.22A	1.62A
–1.9	1.33A	1.12A	1.47A
–1.8	1.20A	1.02A	1.32A
–1.7	1.07A	0.92A	1.18A
–1.6	0.94A	0.82A	1.03A
–1.5	0.81A	0.72A	0.88A
–1.4	0.69A	0.62A	0.74A
–1.3	0.56A	0.52A	0.59A
–1.2	0.43A	0.42A	0.44A
–1.1	0.30A	0.32A	0.30A
–1	0.17A	0.22A	0.15A
–0.9	45.39mA	0.12A	22.39mA
–0.8	7.78mA	23.01mA	8.63mA
–0.7	4.56mA	4.41mA	5.65mA
–0.6	2.55mA	2.06mA	3.26mA
–0.5	1.02mA	0.84mA	1.38mA
–0.4	0.20mA	0.20mA	0.30mA
–0.3	17.34µA	24.91µA	22.95µA
–0.2	0.93µA	2.28µA	0.99µA
–0.1	50.03nA	0.22µA	49.69nA
0	17.84nA	86.83nA	23.01nA

The data, when plotted, resembles a typical diode V-I curve. From the data in Table 8, three useful plots are possible. The minimum V-I curve is based on the minimum recommended V_{CCO} for the LVCMOS33 standard—in this case, 3.0V. The typical V-I curve is based on a

typical recommended V_{CCO} of 3.3V. The maximum V-I curve is based on a maximum recommended V_{CCO} of 3.45V. This range is documented in the device data sheet.

> ***Caution!*** The Spartan-3 FPGA power diode data is different from the Spartan-3E FPGA power diode data. Spartan-3 and Spartan-3E FPGA designs demand separate analysis. Any resulting solution for interfacing to large-swing signals will be different for each family.

The next steps involve formulating what to plot on a graph of I_{IN} versus V_{IN} to graphically find a solution. The first elements to plot on the graph of I_{IN} versus V_{IN} are the Spartan-3E FPGA I_{IN} and V_{IN} limits posed in the original solution requirements (conditions 1 and 2). The I_{IN} limit of 10 mA is a horizontal line and the V_{IN} limit of 4.4V is a vertical line.

This is shown in Figure 5.

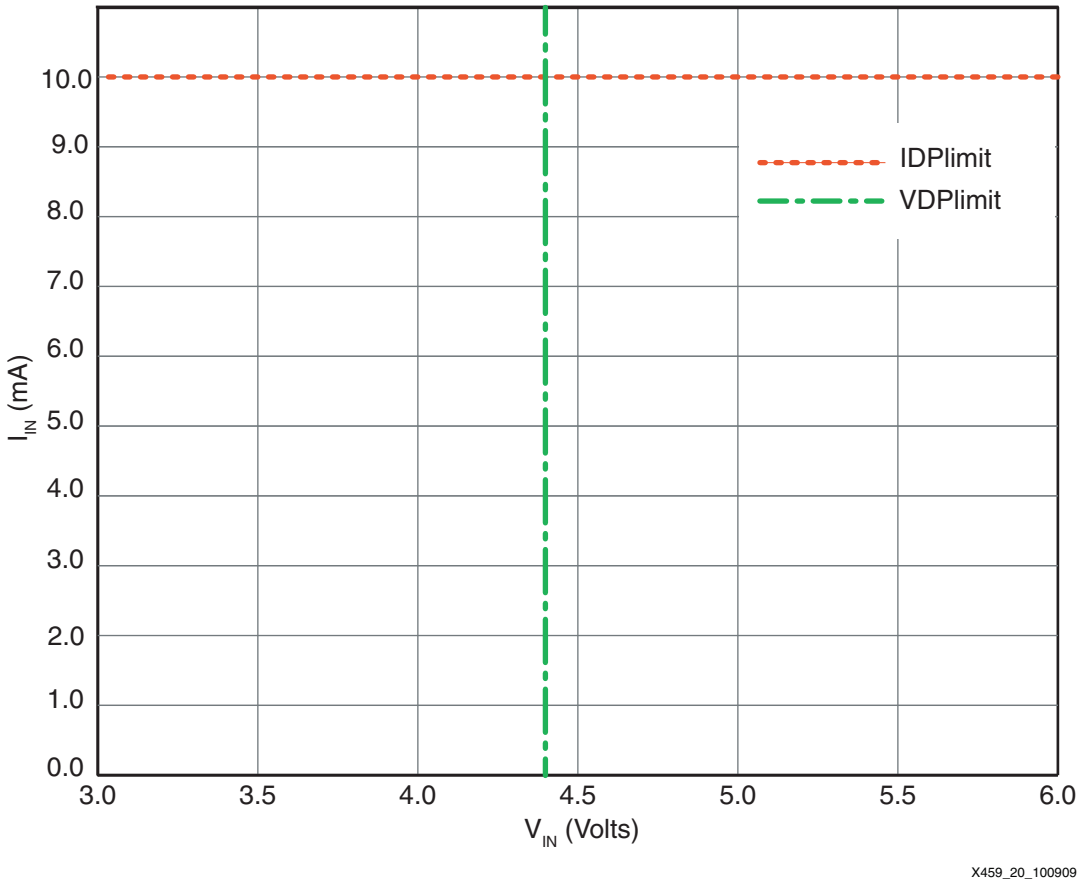

Figure 5: **Plot of I_{IN} and V_{IN} Limits on I_{IN} vs. V_{IN} Graph**

The second element to plot on the graph of I_{IN} versus V_{IN} is the Spartan-3E FPGA power diode behavior. This data is obtained from the IBIS file, and all three sets of data (min, typ, max) are plotted although only the minimum and maximum data are required for the analysis. The diode behavior exists as diode current versus diode voltage. The diode current is I_{IN}, but the diode voltage is not V_{IN}. To plot the data, the following relationship is used: $V_{IN} = V_{CCO} + V_{DP}$. For each data set, the appropriate V_{CCO} value is used:

- $V_{IN} = 3.0V + V_{DP}$ (minimum data set)
- $V_{IN} = 3.3V + V_{DP}$ (typical data set)
- $V_{IN} = 3.45V + V_{DP}$ (maximum data set)

The power diode behavior, superimposed on Figure 5, yields the graph shown in Figure 6.

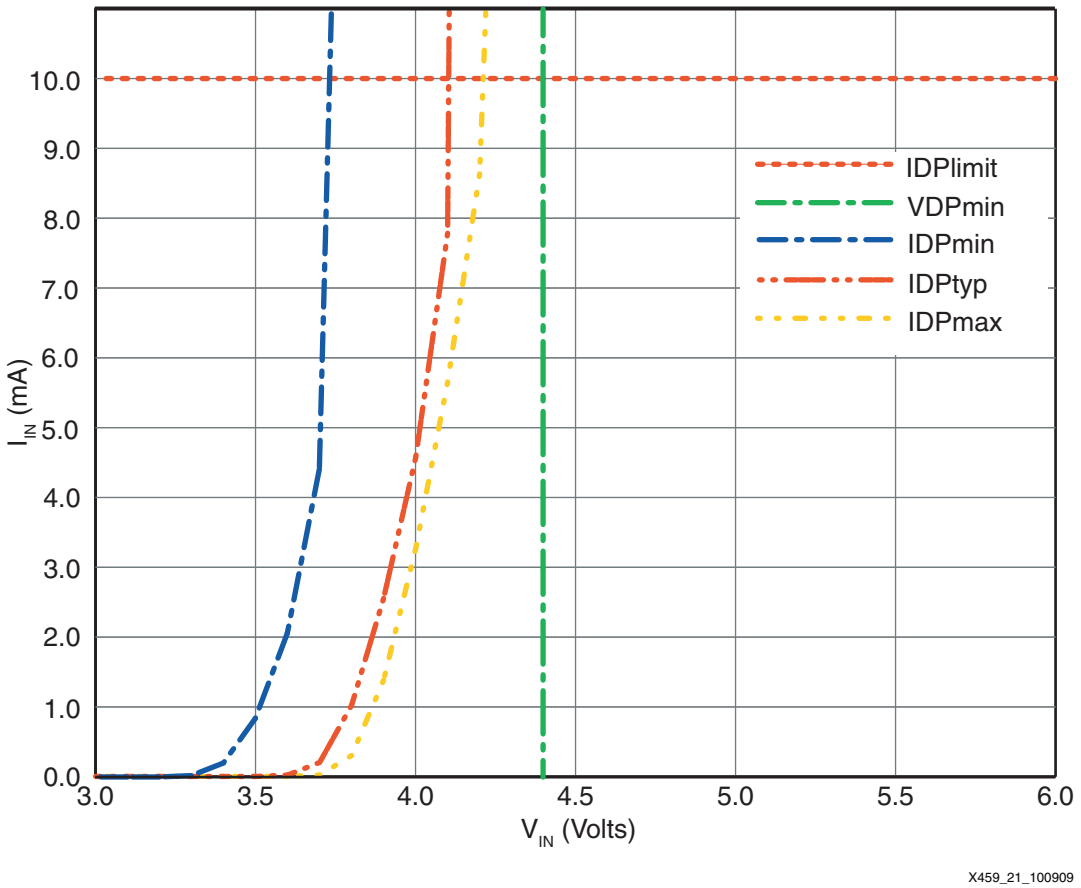

Figure 6: **Power Diode Behavior Added to I_{IN} vs. V_{IN} Graph**

The third element to plot on the graph of I_{IN} versus V_{IN} is a representation of a load-line equation containing the variable R_{SER}. Applying Ohm's Law to R_{SER} in Figure 4 results in the following:

$$R_{SER} = (V_{SRC} - V_{IN}) / I_{IN}$$

Rearranging the terms into the slope-intercept form of a line (y = mx + b) gives:

$$I_{IN} = ((-1/R_{SER}) * V_{IN}) + V_{SRC}/R_{SER}$$

With this form of the equation, it is clear that the slope of the load line is $(-1/R_{SER})$ and the intercept is (V_{SRC}/R_{SER}). At this point in the analysis, R_{SER} is unknown but the intercept of the load line can be calculated. When $I_{IN} = 0$, $V_{IN} = V_{SRC}$, which was previously defined as 5.0V ±10% for this example. The maximum value of V_{SRC} is 5.5V, the typical value is 5.0V, and the minimum value is 4.5V. As a result, three load lines are plotted although only the minimum and maximum data is required for analysis. As R_{SER} changes during the iterative solution search, the slope of the load lines change—effectively, the load lines pivot around their respective intercepts.

The load line behavior, superimposed on Figure 6, yields the graph shown in Figure 7. Remember that R_{SER} is unknown. In order to plot actual lines, an initial guess of 500Ω is used for R_{SER} to generate Figure 7. This initial guess is not necessarily a valid solution, but a starting point for iteration.

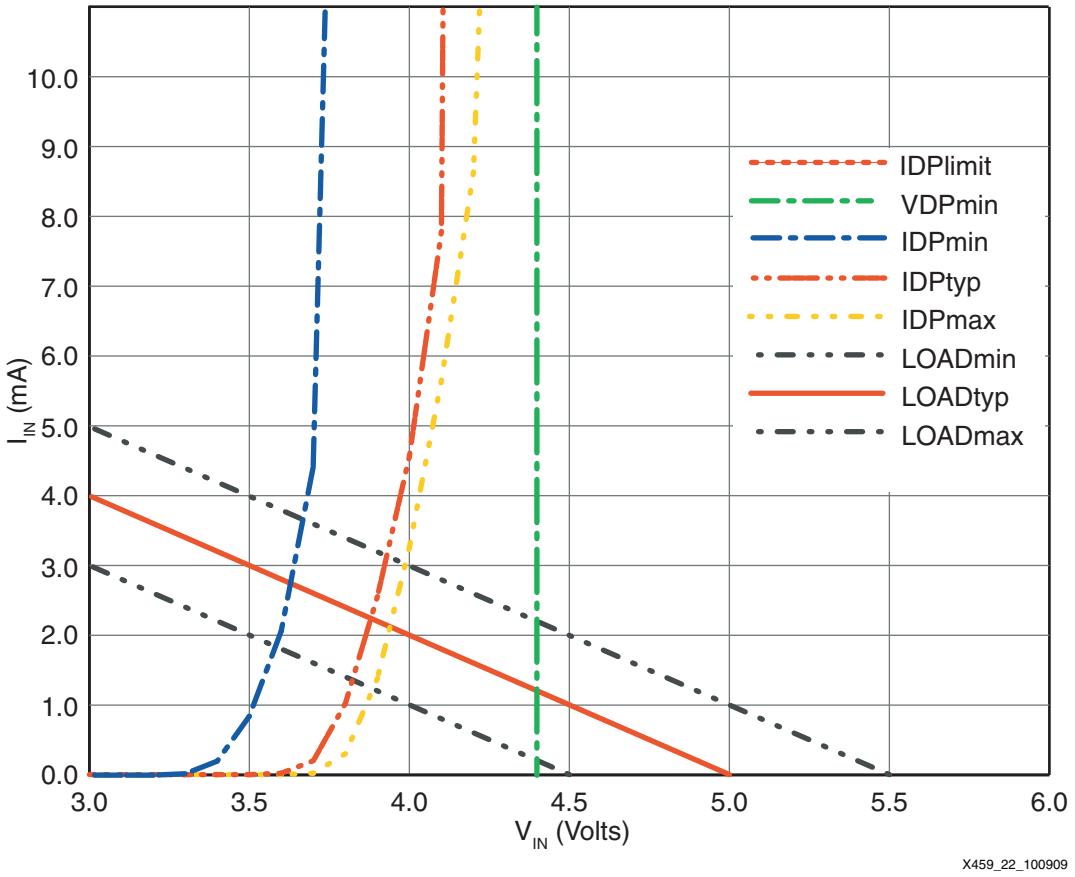

Figure 7: **Load Lines Added to I_{IN} vs. V_{IN} Graph with R_{SER} Guess**

The operating region for the circuit is the intersection of the diode curves and the load lines. Depending on conditions such as temperature, process variation, and supply voltage, the operating point of the circuit will fall somewhere inside this intersection.

Any given operating region, ultimately determined by the value of R_{SER}, is subject to the limits posed in the original solution requirements (conditions 1 and 2). Specifically, the operating region must wholly reside below the I_{IN} limit and to the left of the V_{IN} limit. In Figure 7, the I_{IN} limit is shown with a white line, while the V_{IN} limit is shown with a black line. There is typically a range of R_{SER} values that solves the system of diode curves and load lines. It turns out the initial guess of 500Ω is a valid solution. However, it is not the only solution.

To seek the bounds of the full solution set, iteratively change the R_{SER} value until the operating region is completely valid and just barely touching one (or possibly both) of the V_{IN} and I_{IN} limits. Figure 8 shows this condition for the design example; R_{SER} has a value of approximately 176Ω. While adjusting R_{SER}, the operating region first hits the I_{IN} limit, although this might be different in other design cases. Depending on the design parameters, the operating region might first hit the V_{IN} limit.

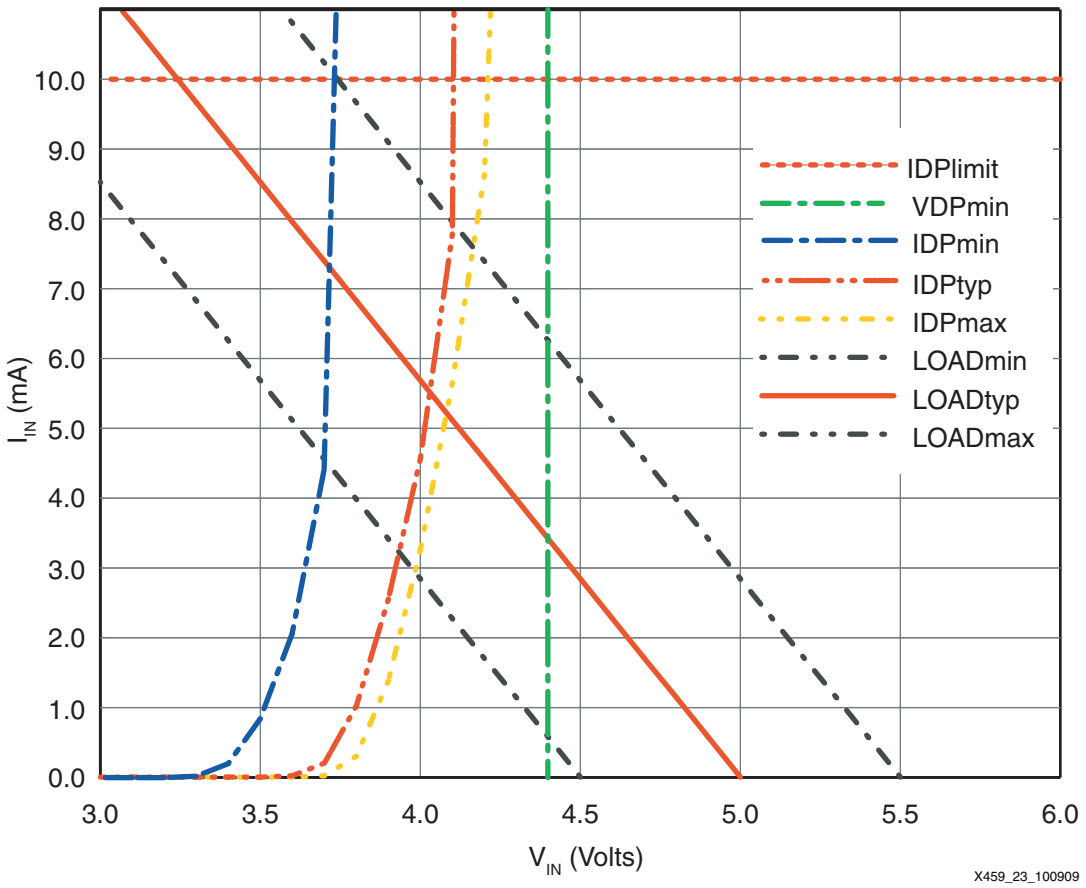

Figure 8: **Final I_{IN} vs. V_{IN} Graph with R_{SER} = 176Ω**

For higher values of R_{SER} (like the initial guess of 500 Ω), the slope of the load lines decreases, moving the operating region further away from the I_{IN} and V_{IN} limits. The main advantages of using higher values are providing additional design margin and reducing the current into the V_{CCO} supply rail. This current is undesirable because it can affect the V_{CCO} supply regulation scheme and increase power consumption.

The main disadvantage of using higher values is the increase in the signal transition time as observed by the User I/O. For estimates of signal rise and fall times, use a circuit simulator with a model of the external device output driver.

Managing the Reverse Current

Continuing with the example shown in Figure 4, this section addresses condition 3 of the limits posed in the original solution requirement. With the power diode on, charge is injected into the V_{CCO} rail associated with the User I/O. This current must not be allowed to adversely affect V_{CCO} regulation. If not properly handled, the reverse current can force the supply voltage out of regulation, causing V_{CCO} to rise above its specified range. There are two ways to manage the reverse current.

One solution requires the use of a supply regulator that has the specified ability to sink the maximum expected current that will be injected into the V_{CCO} rail. Such regulators are available from many power solution manufacturers. However, most common (inexpensive) linear and switching regulators do not offer this capability.

Another solution is to connect a parallel resistor, R_{PAR}, from the regulator output to ground. This is often called a bleed resistor. This resistor shunts current to ground, artificially increasing the current output of the regulator. The idea is to artificially increase the regulator current output to offset any potential reverse current, so that the regulator output current will never become

negative. An obvious side-effect of this approach is that some amount of current is wasted, which consumes extra power and, in some cases, forces the use of a regulator with higher current capacity than otherwise required.

The expected maximum diode current per User I/O, I_{IN}, is measured at the highest point of the operating region of the interface solution. Based on the requirements of the interfacing solution, this will never exceed 10 mA per pin. The current can be less if the location of the operating region indicates the actual current will be less than 10 mA. Figure 9 shows how several User I/Os can result in a significant amount of current injected into the V_{CCO} rail.

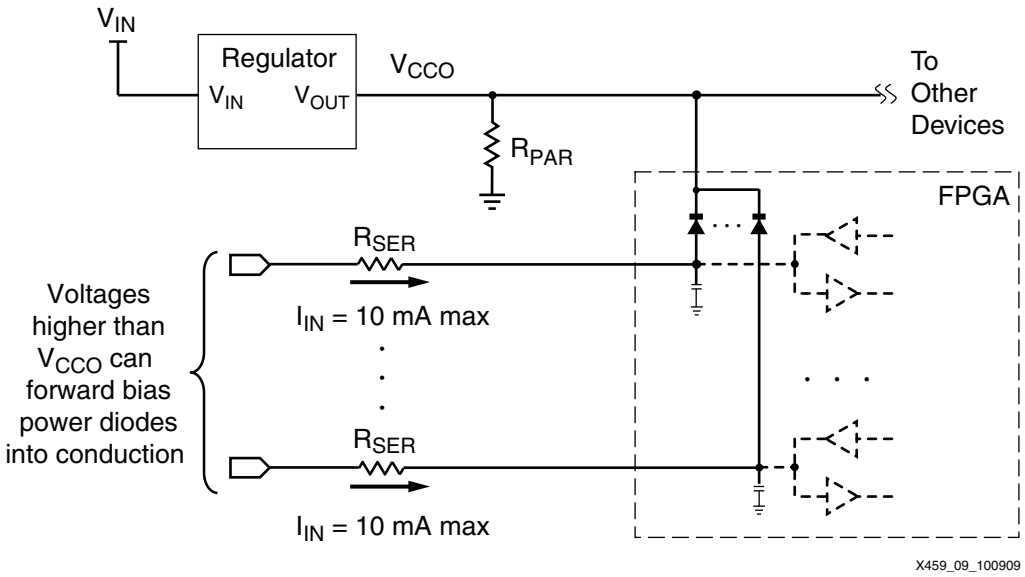

Figure 9: **Reverse Current Solution for Regulator**

The total maximum current injected into the V_{CCO} power rail, I_{REV}, is the sum of all the contributions from all User I/O with forward-biased power diodes. The simple solution to manage the reverse current is to increase the quiescent regulator output current by I_{REV}. This is done by adding R_{PAR}. The value of R_{PAR} is calculated by:

$$R_{PAR} = V_{CCO}, \text{ min} / I_{REV}, \text{ max}$$

With R_{PAR}, the regulator output current never becomes negative even if the maximum I_{REV} is injected into the V_{CCO} supply rail through the power diodes.

In some cases, other devices share the V_{CCO} supply rail. For example, lower voltage FPGA supplies such as V_{CCAUX} and V_{CCINT} can be regulated from the V_{CCO} supply rail. Other peripheral devices can also draw current from V_{CCO}. In these cases, if it is possible to determine a minimum guaranteed quiescent current drawn from V_{CCO}, that current can be used to offset the I_{REV}, max current in the R_{PAR} calculation. This increases the value of R_{PAR}—reducing the power consumption.

If, during design analysis, the power consumption of R_{PAR} is deemed undesirably large, the designer can consider increasing the value of R_{SER} used in the interfacing solution to reduce the current contribution of each User I/O. There is a trade-off between the power that R_{PAR} consumes and the degree to which R_{SER} slows down the signal transition time seen by the User I/O. Ultimately, the particular needs of the application determine the optimal balance between the R_{SER} and R_{PAR} values.

Parasitic Pin Leakage Current Issue

The flexible User I/O pins present on the Spartan-3 FPGA families generally exist as differential pin pairs. A differential pin pair consists of two User I/O pins that can be used as two single-ended I/O or as a single differential I/O. Based on the user's design, the User I/O pins are configured as required. Since the User I/O is configurable, the physical silicon design of each differential pin pair inherently includes both single-ended and differential capabilities, with certain functions disabled based on the user's design.

Between the two pins of every differential pin pair, there is a programmable circuit that behaves like a differential termination resistor. This circuit can be enabled in differential signaling applications using the DIFF_TERM attribute but is otherwise disabled. However, a parasitic path through this circuit is always physically present, even when the circuit is disabled. At any differential pin pair, if the pin voltage of one of the User I/O pins is below –0.2V or exceeds the general recommended operating conditions, then it is possible to observe an increased leakage current on the other User I/O pin in the differential pin pair:

- Spartan-3 devices are susceptible to increased leakage when $V_{IN} < –0.2V$ or when $V_{IN} > V_{CCO} + 0.3V$.
- Spartan-3E devices are susceptible to increased leakage when $V_{IN} < –0.2V$ or when $V_{IN} > V_{CCO} + 0.5V$.
- Extended Spartan-3A devices are susceptible to increased leakage only when $V_{IN} < –0.2V$.

The increased leakage current can cause unexpected design behavior, but does not damage the device. To avoid costly debug efforts and hardware redesign, understanding how to manage or avoid this behavior is crucial. First, it is important to recognize scenarios that can cause this behavior.

- Severe positive and/or negative overshoot can result in transient pin voltages that exceed the conditions in the three bulleted items above. Severe positive and/or negative overshoot must be avoided by ensuring all board level connectivity exhibits good signal integrity. Edge rates must be lowered (where possible), and appropriate termination schemes should be applied. Any interface with the possibility of signal integrity issues should be simulated.
- Implementations of "Solution 3: Voltage Clamps Using Internal Diodes" might result in pin voltages exceeding the conditions in the three bulleted items above. One avoidance approach is to use voltage-level translators. Another avoidance approach, when using the internal diodes, is to leave the other pin of the differential pin pair unused so that the leakage current has no effect.

Use of the technique presented in "Solution 3: Voltage Clamps Using Internal Diodes" requires that the designer manage the potential effects of the increased leakage current.

This parasitic leakage can occur within the recommended operating conditions in cases of undershoot below –0.2V and above the operating condition specification (–0.3V for Spartan-3 FPGAs, –0.5V for Spartan-3E and Extended Spartan-3A FPGAs). For more details on parasitic leakage within the recommended operating conditions, refer to the "Parasitic Leakage" section in UG331, *Spartan-3 Generation FPGA User Guide*.

Based on the general conditions of the solution, the behavior of the device clamp diodes, the large-swing signal amplitude, and the value selected for R_{SER}, the User I/O pin voltage might actually rise to the absolute maximum rating of the device. This is clearly in excess of the general recommended operating conditions, beyond which appreciable parasitic pin leakage occurs. This is an acceptable large-swing signal interface design, but it can have unintended side effects on the other pin of the differential pin pair. Figure 10 and Figure 11 illustrate observed worst case behavior.

Figure 10 plots the aggressor pin current versus the victim pin current for cases where the pin voltage is lower than GND. This graph applies to all Spartan-3 families.

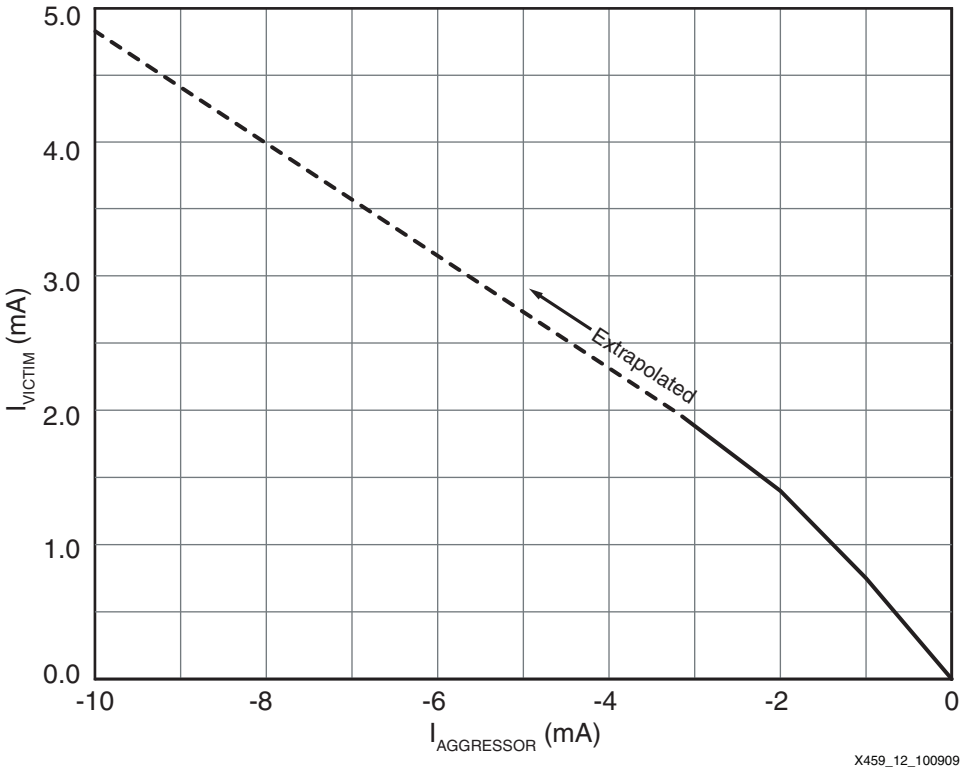

Figure 10: **Worst Case Parasitic Pin Leakage (Negative Overshoot)**

Figure 11 plots the aggressor pin current versus the victim pin current for cases where the pin voltage is higher than V_{CCO}. This graph applies to Spartan-3 and Spartan-3E FPGAs only. Extended Spartan-3A FPGAs do not exhibit the behavior shown in Figure 11.

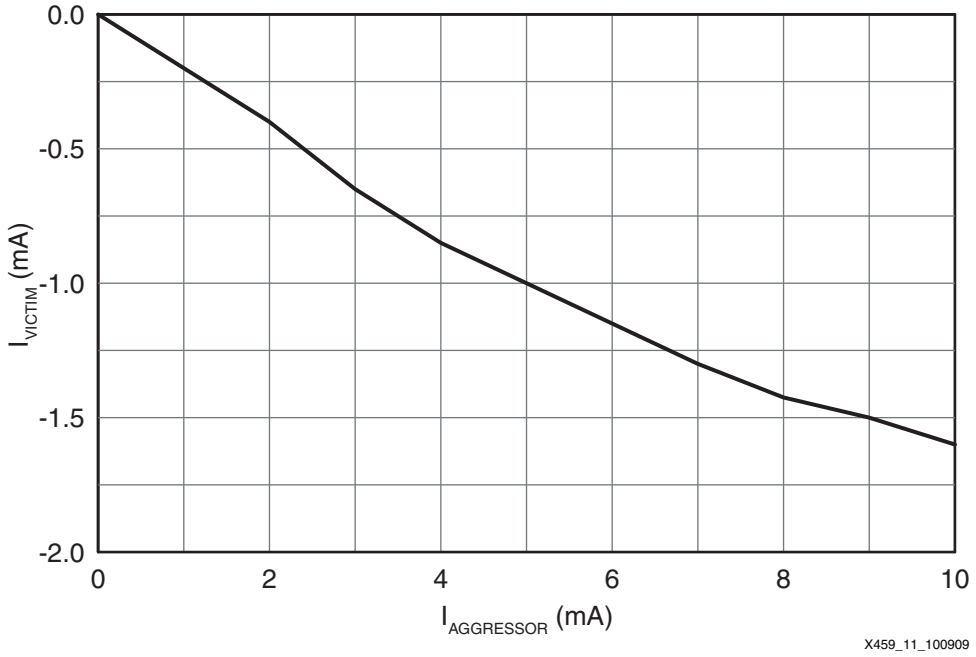

Figure 11: **Worst Case Parasitic Pin Leakage (Positive Overshoot)**

A potential design failure scenario is presented in Figure 12; it is based on the application of "Solution 3: Voltage Clamps Using Internal Diodes" for Spartan-3E FPGAs where the other pin in the differential pin pair is receiving a signal that is weakly driven. This weakly driven signal could represent a bussed control that is occasionally not driven and relies on a pull down to hold a valid logic level. It could also represent an arbitrary analog circuit with a high output impedance.

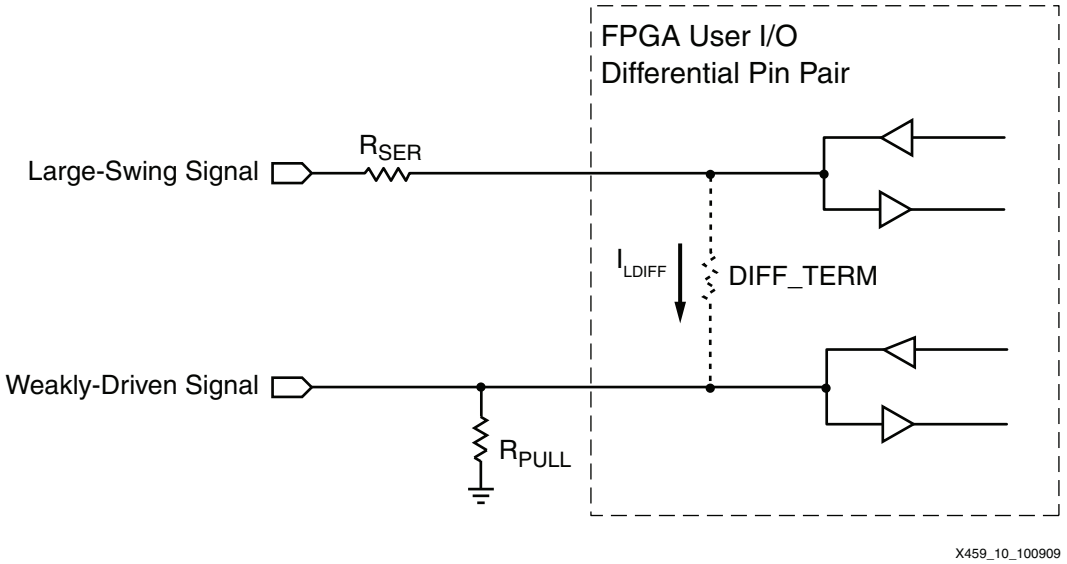

Figure 12: **Potential Design Failure Scenario**

Based on the result of Figure 8 and the data in Figure 11, the pin current of the aggressor User I/O pin can rise as high as 10 mA, resulting in I_{LDIFF} leakage current in excess of 1.5 mA in the victim User I/O pin. Unfortunately, with an R_{PULL} of 2 kΩ, the magnitude of this leakage current is sufficient to change the logic level observed by the input buffer of the victim User I/O.

This is clearly undesirable. If the weakly driven signal is a data signal, data corruption might result from activity on the large swing signal. If the weakly driven signal is a clock, reset, or other control signal, the application might exhibit spurious failures.

Conclusion

This application note presents solutions that permit the Spartan-3 FPGA families to receive signals with a larger swing than is ordinarily permitted. Approaches include external voltage level translators for high performance interfacing, open-drain techniques for moderate performance interfacing, and a unique solution (applicable only to Spartan-3 and Spartan-3E FPGAs) leveraging internal diodes associated with User I/O pins of the FPGA.

Additionally, the issue of parasitic pin leakage is discussed to clarify a behavior that might be observed when leveraging internal diodes for the purpose of receiving large-swing signals. This behavior can also occur when large-swing signals are applied to the User I/O pins in the form of severe positive and/or negative overshoot.

References

These references provide additional information useful to this application note:

1. DS099, *Spartan-3 FPGA Family: Complete Data Sheet*
2. DS312, *Spartan-3E FPGA Family: Complete Data Sheet*
3. DS529, *Spartan-3A FPGA Family: Data Sheet*
4. DS557, *Spartan-3AN FPGA Family: Data Sheet*
5. DS610, *Spartan-3A DSP FPGA Family: Data Sheet*

6. UG331, *Spartan-3 Generation FPGA User Guide*
7. UG332, *Spartan-3 Generation Configuration User Guide*
8. XAPP453, *The 3.3V Configuration of Spartan-3 FPGAs*
9. XAPP646, *Connecting Devices in the Virtex and Spartan-3 Families to a 3.3V or 5V PCI Bus*
10. *Translation Guide*, SCYB018A, Texas Instruments Inc.
11. *Selecting the Right Level-Translation Solution*, SCEA035A, Texas Instruments Inc.
12. *SN74LVC2G34 Dual Buffer Gate*, SCES359H, Texas Instruments Inc.
13. Xilinx IBIS Files, www.xilinx.com/download

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
04/18/08	1.0	Initial Xilinx release.
12/4/09	1.1	Updated Spartan-3 family names. In Table 5, changed the V_{IN} maximum value for the I/O, Input-only, and Dual-Purpose pins to 4.1V to match the data sheets.
09/24/10	1.2	Added sentences about parasitic leakage to third paragraph of the "Summary" section. In the "Parasitic Pin Leakage Current Issue" section, added "below –0.2V" as an option for the pin voltage of one of the User I/O pins to the second paragraph; changed the first V_{IN} expression to $V_{IN} < –0.2V$ for all devices in the first three bullets; clarified the conditions that are referred to in the fourth and fifth bullets; and added a paragraph about when parasitic leakage can occur within the recommended operating conditions. Added UG331 to the "References" section.

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