



OpenCores.Org

# Random Number Generator Library User Guide

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## Revision History

<b>Rev.</b>	<b>Date</b>	<b>Author</b>	<b>Description</b>
1.0	02/09/04	Geir Drange	First version

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# 1

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# Introduction

When writing test benches, it is often useful to include a degree of randomness in the simulation. Typical examples are:

- Random data generation
- Adding noise to signals
- Generate random delays
- Clock jitter generation
- Etc

VHDL does not have any built-in functions for random numbers (yet). The Random Number Generator Library can easily be included in a test bench to supply random number functions.

Note that this library will NOT synthesize. It is intended for test bench use only.

# 2

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## Using the library

To use the library, add the following line to the test bench:

```
use work.rng_lib.all;
```

A random variable is defined by a record, and must be initialized before use. There is a separate initialization function for each type of distribution. Example:

```
r_uni := init_uniform(0, 0, 0, 0.0, 200.0);
```

will initialize a uniform distributed variable with values between 0 and 200. The random variable (real) is accessed by the .rnd member of the record:

```
r := r_uni.rnd; -- r is a real  
i := integer(r_uni.rnd); -- i is an integer
```

Generate a new number with the rand() function:

```
r_uni := rand(r_uni);
```

### 2.1 Seeds

The first 3 parameters (a, b, c) for the initialization functions are seeds for the Tausworthe generators. If a seed is set to zero, a predefined seed will be used. Predefined seeds will also be used if  $a < 3$ ,  $b < 9$  or  $c < 17$ .









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## Know issues

The library will not work with Symphony EDA Sonata simulator. Due to bad floating point support?