GFX_TextController

Description

This is a text mode video display controller that supports color intended for use with a 64-bit bus. The controller uses several internal dual ported memories to store text, text attributes and character font bitmaps. The display memory is memory mapped into the processor address space and is sixty-four bits wide. Up to 4096 different simultaneous characters may be displayed along with 21-bit background and foreground colors (RGB777 format). The use of internal dual ported memories means that the text controller does not consume any memory bandwidth from the processor.

The core is selected via a circuit select input. It acts as a memory mapped I/O (MMIO) device and requires a 128kB address range.

Address	Description
$0000 to $0FFFF	text screen and attribute memory area, currently the controller only supports a 64kB memory
$18000 to $1FFFF	character bitmap memory, currently the controller only supports a 32kB memory, which allows 4096 8x8 character bitmaps. The bitmap memory is write-only.
$17F00 to $17FFF	text controller register area

Text and Attribute Memory Layout

63 58	57 37	36 16	11 0
z-order	Fg Color	Bk Color	char code

Clocks

The text video display controller uses two clocks, a bus timing clock (clk_i) and a video timing clock (dot_clk_i), which can be completely independent.

The core synchronizes the display relative to externally supplied horizontal and vertical synchronization signals.

Register Description

Reg. No.	Bits	0	R/W	Description
00h	0 to 7	ccccccccc	RW	c…c = number of columns ddd = character output delay (default 3).
	8 to 15	rrrrrrrr	RW	number of displayed rows
	16 to 23	dddddddd	RW	character output delay
	24 to 31		RW	reserved
	32 to 43	nnnnnnnnnnnn	W	Text window position- pixels before the display starts, referenced to the hsync signal
	44 to 48		RW	reserved
	48 to 59	nnnnnnnnnnnn	W	Text window position - scan lines down from the top of the screen referenced to the vsync signal
	60 to 63		RW	reserved
08h	0 to 5	nnnnn	W	maximum scan line used to display chars default is 18.
	6 to 7		RW	reserved
	8 to 11	wwww	W	pixel width in video clocks, default is 0 (1 video clocks per pixel)
	12 to 15	hhhh	W	pixel height in scan lines default is 0 (one video scan lines per pixel).
	16 to 21		RW	maximum horizontal pixel used to display char. default is 11.
	22 to 23		RW	reserved
	24	r	W	This bit when set to 1 places the controller in a special reset mode. Default is 1.
	25 to 31		RW	reserved
	32		RW	controller enable, 0 = disable controller (may gate off clock)
	33 to 39		RW	reserved
	40 to 47		RW	reserved
	48 to 52		RW	y-scroll
	53 to 55		RW	reserved

	56 to 60		RW	x-scroll
	61 to 63		RW	reserved
10h	0 to 21	RGB777	W	color value that corresponds to a transparent background color
	22 to 31		RW	reserved
	32 to 63	RGB888	W	border color
18h	0 to 4	eeeee	W	scan line cursor display ends on
	5 to 7	bbb	W	**BB = Cursor Blink Rate** 00 no blink 01 no display 10 1/16 frame rate (4 times per second) 11 1/32 frame rate (2 times per second)
	12 to 8	sssss	W	scan line cursor display starts on
	14 to 15	TT	W	**TT = Cursor Type** 00 Box 01 Line 10 Underscore 11 Asterisk
	16 to 31		RW	reserved
	32 to 47		RW	location of the cursor in the display memory
	48 to 63		RW	reserved
20h	0 to 15	aaaaaaaa aaaaaaaa	W	starting address of the text screen in the display memory, defaults to zero
	16 to 63		RW	reserved
28h	0 to 14	aaaaaaa aaaaaaaa	W	font address in bitmap memory
	15 to 63		RW	reserved
30h	0 to 63		RW	reserved
38h	0 to 15	aaaaaaaa aaaaaaaa	R	address of the light pen
	16 to 63		RW	reserved

Graphics

The core may be used as a low-resolution graphics controller via the programmable character set. The characters can be programmed for block graphics. For instance, each character could be a

two by two grid of pixels. Sixteen different characters would be required to represent all the different combinations. It is also possible to program characters to a three by three grid of pixels using 512 programmable characters to represent every possible combination of on/off pixels. The default resolution is 64x33 or (768x594 pixels).

Graphics and text may be intermixed by allocating part of the programmable character set for a graphic array. For instance, using 256 programmable characters a 128x128 bitmapped display can be created.

Special Reset Mode

In special reset mode the core display memory is continuously updated according to the address on the address bus. This mode allows an echo of the system startup data to the display. This mode is disabled by writing a zero bit to register 08h bit 24.

Core Parameters

Name	Default Value	Description
COLS	64	default number of columns of text
ROWS	33	default number of rows of text

Module Interface Description

rtfTextController

```
module rtfTextController(rst_i, clk_i, cs_i, cyc_i, stb_i, ack_o, we_i, adr_i, dat_i, dat_o,
vclk, hsync, vsync, blank, border, rgbIn, rgbOut);
```

System	Description
rst_i	This signal is normally connected to the system reset signal. It resets the text controller interface forcing it to the reset state.
clk_i	This is usually connected to the system clock and is used as a base timing clock for I/O operations.
Slave Port	
cs_i	circuit select input - selects the core for a read or write operation.
cyc_i	indicates that a valid bus cycle is taking place. The core will not respond to the bus unless this signal is active.
stb_i	This strobe signal also indicates that a valid bus cycle is taking place
ack_o	This signal indicates that the core has processed the bus transaction (it is the logical and of cyc_i and stb_i).

we_i	This signal is used to signify a write operation to the text controller.
adr_i	This sixteen bit address bus is used to address one of text controllers's registers or internal memory. (Registers are described below). Registers respond to the address range $DFxx
dat_i	This is the 32 bit data input bus to the text controller.
dat_o	This is the 32 bit data output bus from the text controller.
Video Ports	
vclk	This input is the video clock input. Pixel timing is derived from it.
hsync	Horizontal sync. This input signal signals the start/end of a video scanline (end-of-line)
vsync	Vertical sync. This input signal indicates the end of the video frame.
blank	This input signal indicates that the display should be blanked. It is active during the video blanking period.
border	This input signal indicates that a border area is active.
rgbIn	This 32 bit input bus can be connected to an external RGB input. (The text controller may display on top of the external input).
rgbOut	This output signal bus contains the 32 bit RGB display data.
Parameters	
ROWS	Use this parameter to specify the default number of text rows.
COLS	Use this parameter to specify the default number of text columns.

WISHBONE Compatibility Datasheet

The text controller core may be directly interfaced to a WISHBONE compatible bus.

WISHBONE Datasheet WISHBONE SoC Architecture Specification, Revision B.3	
Description:	Specifications:
General Description:	GFX_TextController - Text mode video display controller
Supported Cycles:	SLAVE, READ / WRITE

	SLAVE, BLOCK READ / WRITE SLAVE, RMW	
Data port, size: Data port, granularity: Data port, maximum operand size: Data transfer ordering: Data transfer sequencing	64 bit 64 bit 64 bit Little Endian any (undefined)	
Clock frequency constraints:		
Supported signal list and cross reference to equivalent WISHBONE signals	Signal Name: ack_o adr_i(16:0) clk_i dat_i(63:0) dat_o(63:0) cyc_i stb_i we_i	WISHBONE Equiv. ACK_O ADR_I() CLK_I DAT_I() DAT_O() CYC_I STB_I WE_I
Special Requirements:	external sync generator	