



# SGMII Core

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*SGMII*

This document describes interfaces and design of SGMII Core

*11/10/2012*

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## 1. OVERVIEW

This core implements Physical Coding Sublayer of 1000BaseX transmission (IEEE 802.3 Clause36 and 37). This core can also be used for SGMII interface as this interface leverages 1000BaseX PCS. The differences between the 2 protocols are Link-timer and the control information exchanged during Auto-negotiation process.

Modes of operation:

- 1000BaseX mode. This is the default mode of the core. In this mode, local capability register needs be set so that the core can advertise the capability of local link.
- Mac-SGMII mode: in this mode, the core works in SGMII mode at MAC side. The core only transmits acknowledgement bit during negotiation process, the other bits are set to “0” as specified by Cisco. The operating speed/duplex is set by:
  - o Received partner speed/duplex (default)
  - o Or Bit 6,13, and 8 in control register. To force the core into this speed, Use\_Local bit in Mode register must be set.
- Phy-SGMII mode: in this mode, the core works in SGMII mode at Phy-Side. That means the core would actively advertise control information which can be set by external ports (i\_PhyDuplex, i2\_PhySpeed, i\_PhyLink) or via **Local Capability registers**. The actual operating speed and duplex are controlled by the external ports or **Control Registers**.

## 2. INTERFACE

Tranceiver Interface	
input i_SerRx, output o_SerTx, input i_CalClk, input i_RefClk125M, input i_ARstHardware_L,	This interface requires 125MHz reference clock and 50MHz Calibration Clock to feed to Transceiver. o_SerTx and i_SerRx are Transmit and Receive line of the transceiver. i_ARstHardware_L is to be connected to hardware reset line.
Local BUS interface Wishbonebus, single transaction mode (non-pipeline slave)	
input i_Cyc, input i_Stb, input i_WEn, input [31:00] i32_WrData, input [07:00] iv_Addr, output [31:00] o32_RdData, output o_Ack,	This wishbone interface is to configures registers such as mode, link-timer or speed ...
input i_Mdc, inout io_Mdio,	Mdio clause 22 interface, not supported yet
Link Status	
output o_Linkup, output o_ANDone, output [1:0] o2_SGMII Speed, output o_SGMIIDuplex,	Link-up is asserted after the synchronization is acquired. AN_Done is asserted after auto-negotiation process is done. SGMII Speed encodes speed of SGMII mode: 10b: 1000Mbps 01b: 100Mbps 00b: 10Mbps (not supported) SGMIIDuplex, this core only support full duplex mode.
SGMII Phy-Side Signals	
input i_PhyLink, input i_PhyDuplex, input [1:0] i2_PhySpeed,	Phy-Side SGMII advertised information PhyLink bit is tied to Bit.15 of Advertised Configurations to indicate copper-link is up or down. PhyDuplex and PhySpeed are tied to bit 12,11:10 of advertised 16-bit information
GMII Interface	
input [07:00] i8_TxD, input i_TxEN, input i_TxER, output [07:00] o8_RxD, output o_RxDV, output o_RxER, output o_GMIIClk, output o_MIIClk, output o_Col, output o_Crs	Standard GMII interface GMII Clk output 125MHz clock output by the transceiver. MIIClk output 25MHz clock used in 100Mbps mode.

## 2.1. REGISTERS

The registers in the cores are accessed through 32-bit bus. Therefore registers are mapped into Double-word address although each register is only 16-bit. The 16 most significant bits are always zeros.

Bit	Name	Offset	Default	Description															
	Control Register	0x00																	
5:0	Reserved	R/W	5'b0	Not used															
6	MSB Speed Selection	R/W	0	From Table 22-7 (IEEE 802.3-2008-Section2) <table style="margin-left: 20px;"> <tr> <td>0.6</td> <td>0.13</td> <td></td> </tr> <tr> <td>1</td> <td>1</td> <td>= Reserved</td> </tr> <tr> <td>1</td> <td>0</td> <td>= 1000 Mb/s</td> </tr> <tr> <td>0</td> <td>1</td> <td>= 100 Mb/s</td> </tr> <tr> <td>0</td> <td>0</td> <td>= 10 Mb/s</td> </tr> </table> <p>This bit is used only inSGMII mode. The speed of SGMII mode can be configured to use these 2 bits or use link partner advertised speed and duplex.</p>	0.6	0.13		1	1	= Reserved	1	0	= 1000 Mb/s	0	1	= 100 Mb/s	0	0	= 10 Mb/s
0.6	0.13																		
1	1	= Reserved																	
1	0	= 1000 Mb/s																	
0	1	= 100 Mb/s																	
0	0	= 10 Mb/s																	
7	Collision Test	R/W	1'b0	Not support															
8	Duplex Mode	R/W		Only full duplex mode is supported, this bit has no effect															
9	Auto-nego Restart	R/W SC	1'b0	Restart autonegotiation process. This bit is self cleared.															
10	Isolate	R/W	1'b0	Not supported															
11	PowerDown	R/W	1'b0	To power down the transceiver, this bit goes directly to powerdown pin of transceiver. Use with care. This feature has not been tested yet.															
12	ANEnable	R/W	1'b0	Enable auto negotiation															
13	LSB Speed Selection	R/W	1'b0	LSB of speed control															
14	Loopback	R/W	1'b0	Enable/Disable Loopback mode (not tested)															
15	Reset	R/W/SC	1'b0	Write '1' to Soft-Reset the whole module															
31:16	Reserved	RO		Zeros															

Bit	Name	Offset	Default	Description
	Status Register	0x04		
1:0		RO	2'b00	
2	Sync Status	RO	1'b0	Status of Synchronization process 1: Synchronization has been done. 0: Rx can't sync to the incoming bit stream
4:3		RO	2'b00	2'b01
5	AN complete	RO	1'b0	Autonegotiation is done
31:6		RO	26'h0	Zeros

Bit	Name	Offset	Default	Description															
	Local Advertised Ability	0x10		This register sets the advertised capability of local link. Some bits are used in 1000BaseX, some are used in SGMII Mode, some are used in both.															
				1000BaseX mode															
4:0																			
6:5				Only supports Full Duplex mode															
7				Pause															
8				Asymmetric dir Table 37-2—Pause encoding <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>PAUSE (D7)</th> <th>ASM_DIR(D8)</th> <th>Capability</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>No PAUSE</td> </tr> <tr> <td>0</td> <td>1</td> <td>Asymmetric PAUSE toward link partner</td> </tr> <tr> <td>1</td> <td>0</td> <td>Symmetric PAUSE</td> </tr> <tr> <td>1</td> <td>1</td> <td>Both Symmetric PAUSE and Asymmetric PAUSE toward local device</td> </tr> </tbody> </table>	PAUSE (D7)	ASM_DIR(D8)	Capability	0	0	No PAUSE	0	1	Asymmetric PAUSE toward link partner	1	0	Symmetric PAUSE	1	1	Both Symmetric PAUSE and Asymmetric PAUSE toward local device
PAUSE (D7)	ASM_DIR(D8)	Capability																	
0	0	No PAUSE																	
0	1	Asymmetric PAUSE toward link partner																	
1	0	Symmetric PAUSE																	
1	1	Both Symmetric PAUSE and Asymmetric PAUSE toward local device																	
11:10	SGMII Speed			Advetised Speed in SGMII mode Encoding: 10: 1000Mbps 01: 100Mbps 00: 10Mbps Notice that these bit are used only in Phy-Side SGMII mode. In Phy SGMII mode, the advertised speed is: $i2\_PhySpeed   LocalAdvertisedCapability[11:10]$ In Mac-side SGMII mode, the bits are always zeros as SGMII specifications.															
12	SGMII Duplex/ Remote Fault 1			1000BaseX mode: Remote fault bit 1 SGMII Phy-Mode: Duplex mode, the advertised Duplex mode is: $i\_PhyDuplex   LocalAdvertisedCapability[12]$															
13	Remote Fault 2			Table 37-3—Remote Fault encoding <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>RF1</th> <th>RF2</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>No error, link OK (default)</td> </tr> <tr> <td>0</td> <td>1</td> <td>Offline</td> </tr> <tr> <td>1</td> <td>0</td> <td>Link_Failure</td> </tr> <tr> <td>1</td> <td>1</td> <td>Auto-Negotiation_Error</td> </tr> </tbody> </table> Table 37-3 and 37-2 from IEEE 802.3-2008 Section 3.	RF1	RF2	Description	0	0	No error, link OK (default)	0	1	Offline	1	0	Link_Failure	1	1	Auto-Negotiation_Error
RF1	RF2	Description																	
0	0	No error, link OK (default)																	
0	1	Offline																	
1	0	Link_Failure																	
1	1	Auto-Negotiation_Error																	
14	Ack bit																		
15	1'b0																		

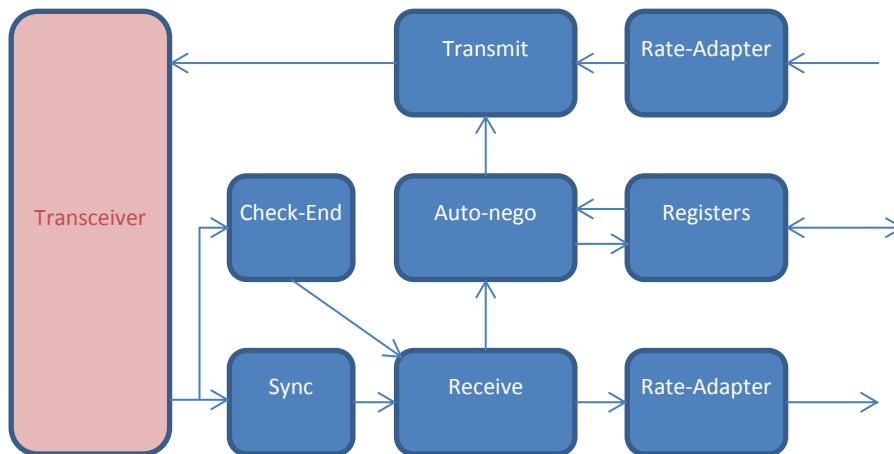
Bit	Name	Offset	Default	Description
	Link Partner capability	0x14		Capability advertised by Link Partner. The values change with mode of operations
				1000BaseX mode
				SGMII mode
0	reserved			1'b0
1	reserved			1'b0
2	reserved			1'b0
3	reserved			1'b0
4	reserved			1'b0
5	FD			Full Duplex
6	HD			Half Duplex
7	PS1			Pause
8	PS2			ASM_DIR
9				1'b0
10	Speed0			Speed Bit 0
11	Speed1			Speed Bit 1. Encoding: 10: 1000Mbps 01: 100Mbps 00: 10Mbps
12	RF1			Remote fault 1
				1: Full Duplex 0: Half Duplex
13	RF2			Remote fault 2
14	Ack Bit			Sent between partners to acknowledge autonego process
				SGMII Mode, sent from MAC to Phy to acknowledge the autonegotiation process
15	Link State			Sent from PHY to Mac
				1: Link Up 0: Link Down
31:16	Reserved			

Bit	Name	Offset	Default	Description
15:0	Link Timer 1	0x20		Least Significant 16-bit of Link Timer
	Link Timer 2	0x24		
4:0				Most Significant 5 bit of Link Timer Together these 2 registers form 21 bit timer which is run by 8-ns clock. Change the value of this register to smaller value during simulation to speed up simulation process.
15:0	Scratch	0x28		Scratch register to test

Bit	Name	Offset	Default	Description
	Mode	0x7C		
0	SGMII			1: SGMII mode 0: 1000BaseX mode The 2 modes differ in autonegotiation process and capability resolution
1	Phy			1: Use as in SGMII Phy Side, i.e. transmit the control information. 0: Use as in SGMII Mac Side, i.e receive the control information and send ack bit
2	Use Local Config			For SGMII Mode Mac Side, the speed and duplex at which the core is operated are set by Link-partner's "advertised" information by default. If this " <b>Use Local Config</b> " is set to "1", the Speed and Duplex are set by control bits 6,13 and 8. Phy Side, the speed and duplex at which the core is operated have to be set by either input port: i_PhyDuplex, i2_PhySpeed or by control bits 8 and 6,13 Note: Do not get confused by advertised speed and the operating speed. Mac-Side SGMII: the Advertised 16-bits are all "0" except ack bit and bit 0. Phy-Side SGMII: The advertised speed/duplex are set by either i_Phy* ports or by Local Capability bits 12..10. The operating speed and duplex are set by either i_Phy* port of by Control register bits 8, 6, 13.



## 2.2. ARCHITECTURES



Sync block: synchronises to the received characters and gives odd/even flag and type of the received order-set. The first code-group of any ordered set must be “even”.

Check-end block: the end of a packet may occur in many “fashion”. The check-end block buffers 3 consecutive code-group and decodes what kind of “end of transmission” is about to happen. The information is fed into Receive block so that the receive block could generate appropriate receive signals.

Receive block: the Receive block receives code groups and generate RxDV, RxER signals. If the received code-group belongs to Configuration Ordered Set (C1/C2), it copies the configuration data and presents to Auto-negotiation block, else it feeds to the rate adapter.

Auto-negotiation block: this block is in charge of sending configuration code groups, checking of the received configuration codes and send “ack” bit if all auto-nego information is valid. It also gives out the current state of the synchronization process which is used by both Transmit and Receive.

Transmit block: In auto-negotiation state, the transmit block receives “config data” from auto-negotiation block and then transmit this 16-bit register in Configuration Ordered set. In data transmit state, it transmits data from rate-adapter block.

Registers block: this block contains registers that control the operation of the core. The registers are accessible via Wishbone-compatible bus. MDIO will be implemented if necessary.

Rate adapter block: in 1000Mb speed rate, the rate adapter is bypassed. In 10/100Mb speed rate, this block elongated each data byte 100/10 times so that it can be transmitted in 1000Mb line rate.

Transceiver block: this block is technology dependent and you have to modify it to fit your system. The transceiver can be implemented using dedicated transceiver or using LVDS differential IO. Using lvds differential IOs requires 8b10b encoder/decoder. The current implementation of bit-slip signal requires the 8b10b encoder/decoder generates Decoding Error signal. Some 8b10b endec doesn't have this signal. In that case, bit-slip should be generated by searching for a fixed pattern (e.g 0xBC) in the received bytes.

### 3. SIMULATION GUIDE

Testbench and simulation scripts are placed in sim folder. The latest simulation script that should be run is: *Sim\_SGMII1000Mblvds.do*. The paths need to be changed to fit user's Quartus Installation. This simulation script compile and run the core in SGMII mode with LVDS serdes. The link partner is an Altera's SGMII-core instantiated in *sim/BFMs* folder. Other scripts that would be useful are:

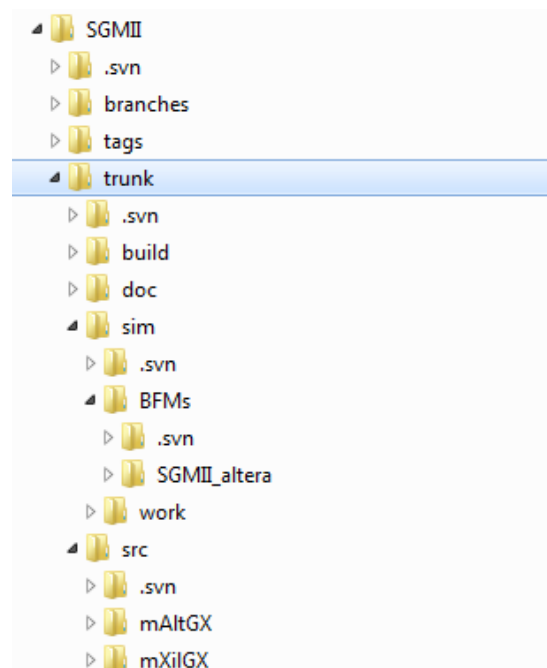
*Sim\_1000BaseX.do*: Simulates the core in 1000BaseX mode using dedicated transceiver.

*Sim\_SGMII1000Mb.do*: simulates the core in SGMII 1000Mbps using dedicated transceiver

*Sim\_SGMII100Mb.do*: simulates the core in SGMII 100Mb using dedicated transceiver.

For these 3 simulations, users have to modify the SGMII.v top file to instantiate GXB-based Serdes.

If everything goes right, simulator should print out something like this:



```
Note : CYCLONEIVGX PLL locked to incoming clock
# Time: 36000000 Instance: mSGMIITestbench.u1SGMII.n1010.cycloneiv_pll.pll4
# Waiting for Auto Negotiation Done
# Link Dropped
# Link Acquired
# ---Core Version : 1000
# Altera SGMII Core Version 0c00
# Link Timer 0 01e2
# Link Timer 1 0000
# Mode Register 1 0013
# Restart PHY auto-nego
# Link Acquired
# (      14573)MAC      : Start Rx Task
# Link Acquired
# Auto-nego completes
# Link Speed      1000 Mbps
# Link Duplex Full
# (      14749)MAC      : Start Rx Task
# E@(      14772): expect 1400, actual 4001 (Link Partner Advertised Ability,Testbench_AltGXB_SGMII1000Mbps.sv, 296)
# E@(      14860): expect 1800, actual d801 (Link Partner Advertised Ability,Testbench_AltGXB_SGMII1000Mbps.sv, 298)
# Start Generating Scenarios
# Transmit Type Normal
# u0: Sending Packet      0 Size      1098
# u1: Sending Packet      0 Size      1098
# MAC: Start Receiving
# MAC: Start Receiving
# u0: Sending Packet      1 Size       501
# u1: Sending Packet      1 Size       501
# MAC: Packet Received with      1098 bytes
# u0: Checked Pkt        1
# (      33788)MAC      : Start Rx Task
# MAC: Packet Received with      1098 bytes
# u1: Checked Pkt        1
# (      33852)MAC      : Start Rx Task
# MAC: Start Receiving
# MAC: Start Receiving
# u0: Sending Packet      2 Size       834
# u1: Sending Packet      2 Size       834
# MAC: Packet Received with      501 bytes
```

#### 4. REVISION HISTORY

<b>Date (dd/mm/yy)</b>	<b>Author</b>	<b>Doc's Rev</b>	<b>Core's Rev</b>	<b>Description</b>
	Jeff	1.0		Core is in verification state
		1.1		Correct some typos Core has been verified in SGMII mode with 88E1111 Marvell Phy
10/11/12	Jeff	1.2	19	Correct some typos Added simulation guide

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