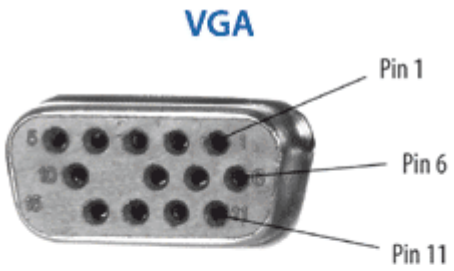
# FPGA to VGA monitor

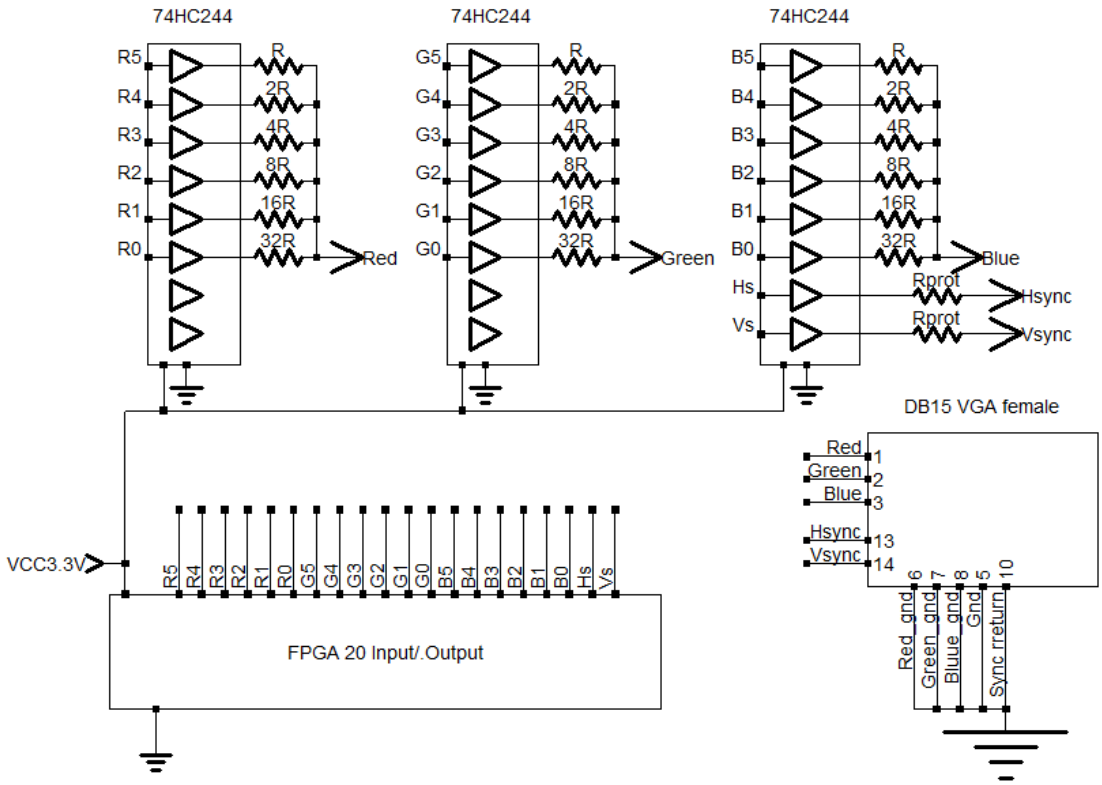
## A-Hardware setup

Pinout  of the VGA graphic card connector:




| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | Red | 9 | *NO CONNECTION* |
| 2 | Green | 10 | Sync Return |
| 3 | Blue | 11 | ID Bit 0 |
| 4 | ID Bit 2 | 12 | ID Bit 1 |
| 5 | Ground | 13 | Horizontal Sync |
| 6 | Red Shield | 14 | Vertical Sync |
| 7 | Green Shield | 15 | *NO CONNECTION* |
| 8 | Blue Shield | | |

Schematic of the adapter card:




Components for the adapter card:

We use small SN74HCT244PWR (TSSOP pitch 0.65). Resistors will be 0603.

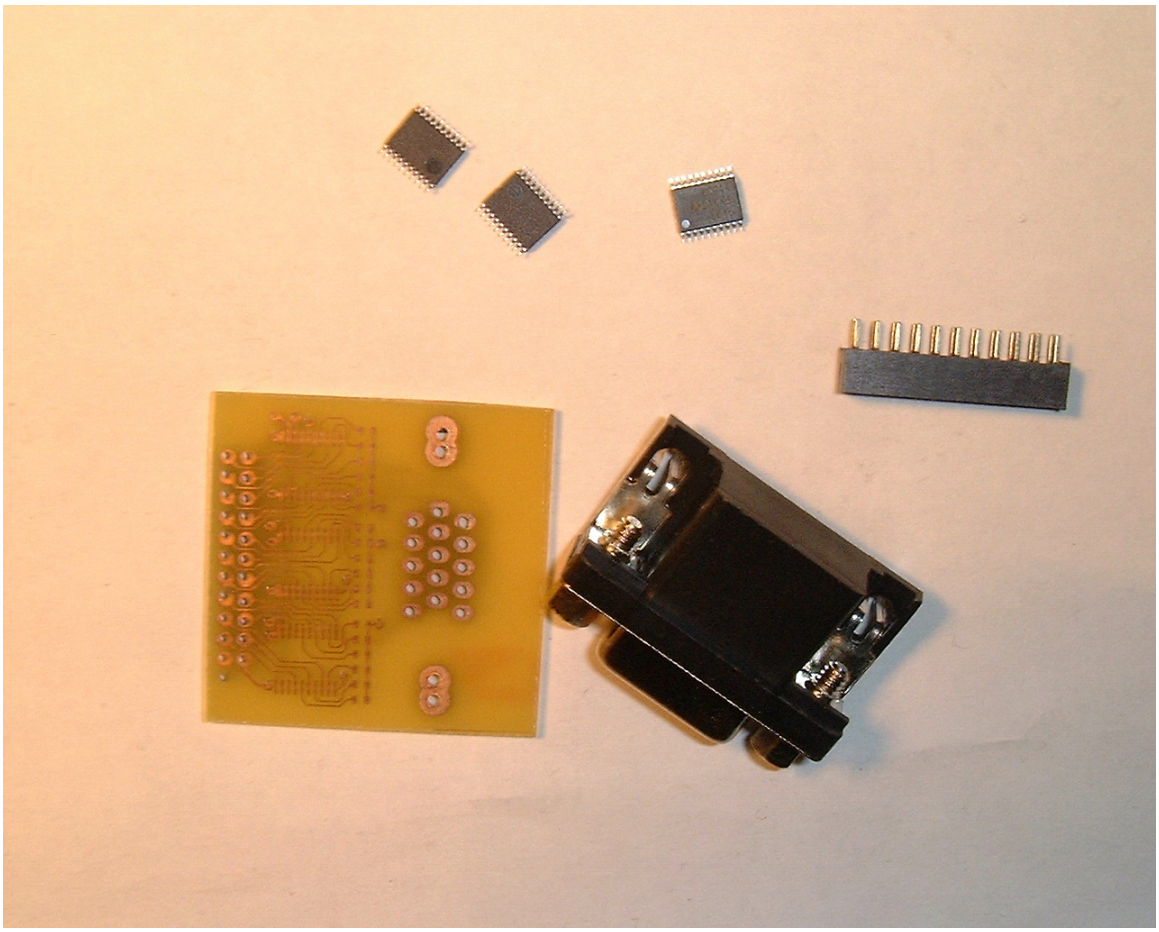
Rprot resistors on HSync,VSync can protect against unexpected currents , i take 100ohm.

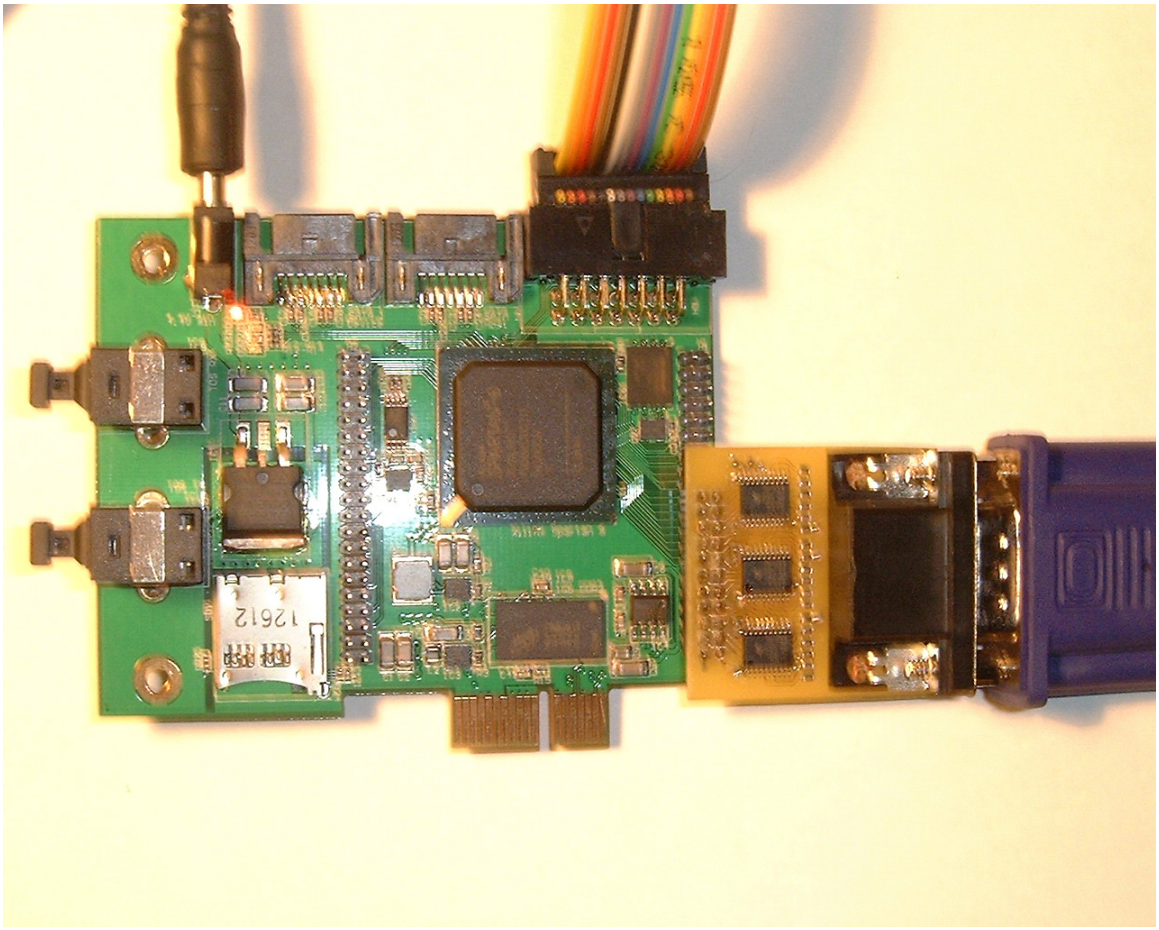
DAC (Digital to analog converter) resistors for 5-5-5 RGB:

(Taken from "OLIMEX LOW COST LCD-TO-VGA ADAPTER"
http://olimex.wordpress.com/2012/06/12/low-cost-lcd-to-vga-adapter/)

| theorical value | Approx. value available |
|---|---|
| R=549 ohm | 560 |
| 2R=1050 ohm | 1K1 |
| 4R=2180 ohm | 2K2 |
| 8R=4370 ohm | 4K3 |
| 16R=8660 ohm | 9K1 |
| 32R=17800 ohm | 18K |

Photos:



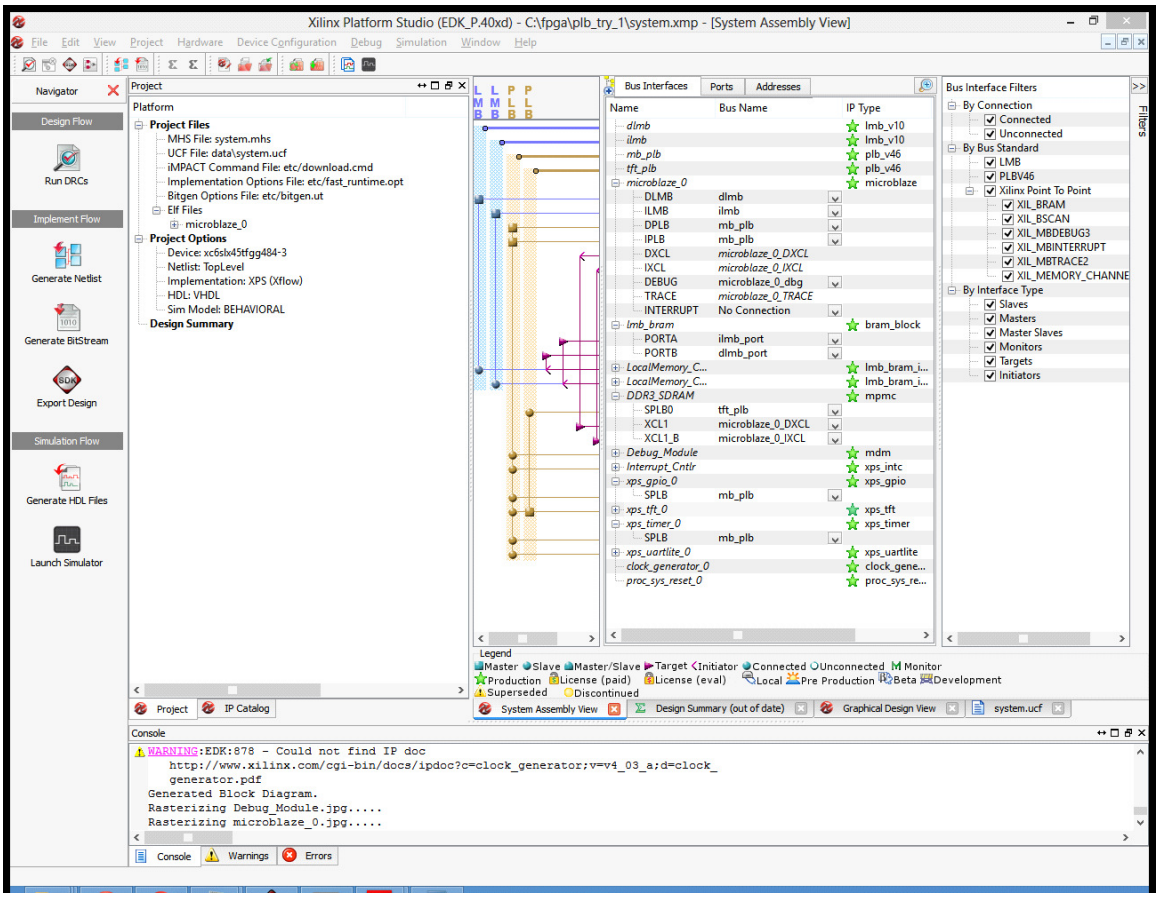


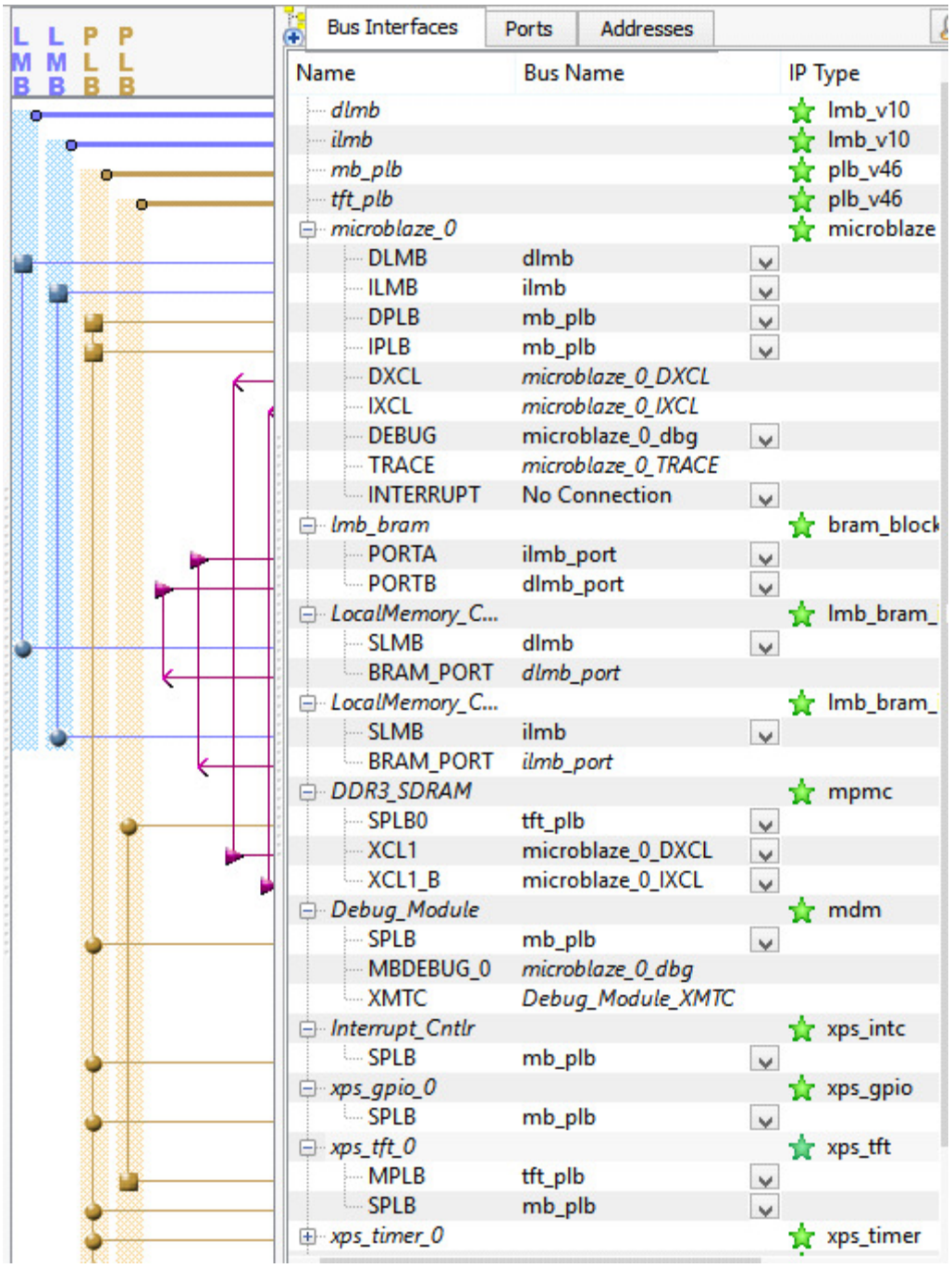
# B-Building the Microblaze processor with xps  tft core in Xilinx Platform studio

A graphic controller core for LCD and VGA is available with Xilinx Platform Studio.

Unfortunately this core is avaliable only  in old  PLB bus on Spartan 6 (It is avaialble as AXI bus peripheral for other FPGA family).

So , i have entirely redesigned a new Microblaze project using the PLBv4.3 bus.


Xilinx Platform Studio (EDK_P.40xd) - C:\fpga\plb_try_1\system.xmp - [System Assembly View]
File Edit View Project Hardware Device Configuration Debug Simulation Window Help
Navigator
Design Flow
Run DRCs
Implement Flow
Generate Netlist
Generate BitStream
Export Design
Simulation Flow
Generate HDL Files
Launch Simulator
Project
Platform
Project Files
MHS File: system.mhs
UCF File: data\system.ucf
iMPACT Command File: etc/download.cmd
Implementation Options File: etc/fast_runtime.opt
Bitgen Options File: etc/bitgen.ut
Elf Files
microblaze_0
Project Options
Device: xc6slx45tfgg484-3
Netlist: TopLevel
Implementation: XPS (Xflow)
HDL: VHDL
Sim Model: BEHAVIORAL
Design Summary
Bus Interfaces
Ports
Addresses
Name
Bus Name
IP Type
dlmb
ilmb
mb_plb
tft_plb
microblaze_0
DLMB
ILMB
DPLB
IPLB
DXCL
IXCL
DEBUG
TRACE
INTERRUPT
lmb_bram
PORTA
PORTB
LocalMemory_C...
DDR3_SDRAM
SPLB0
XCL1
XCL1_B
Debug_Module
Interrupt_Cntlr
xps_gpio_0
SPLB
xps_tft_0
xps_timer_0
xps_uartlite_0
clock_generator_0
proc_sys_reset_0
Bus Interface Filters
By Connection
Connected
Unconnected
By Bus Standard
LMB
PLBV46
Xilinx Point To Point
XIL_BRAM
XIL_BSCAN
XIL_MBDEBUG3
XIL_MBINTERRUPT
XIL_MBTRACE2
XIL_MEMORY_CHANNE
By Interface Type
Slaves
Masters
Master Slaves
Monitors
Targets
Initiators
Filters
Legend
Master Slave Master/Slave Target Initiator Connected Unconnected Monitor
Production License (paid) License (eval) Local Pre Production Beta Development
Superseded Discontinued
Project
IP Catalog
System Assembly View
Design Summary (out of date)
Graphical Design View
system.ucf
Console
WARNING:EDK:878 - Could not find IP doc
http://www.xilinx.com/cgi-bin/docs/ipdoc?c=clock_generator;v=v4_03_a;d=clock_
generator.pdf
Generated Block Diagram.
Rasterizing Debug_Module.jpg.....
Rasterizing microblaze_0.jpg.....
Console
Warnings
Errors




The DDR3 memory has 2 ports

-Processor port

-video frame buffer port

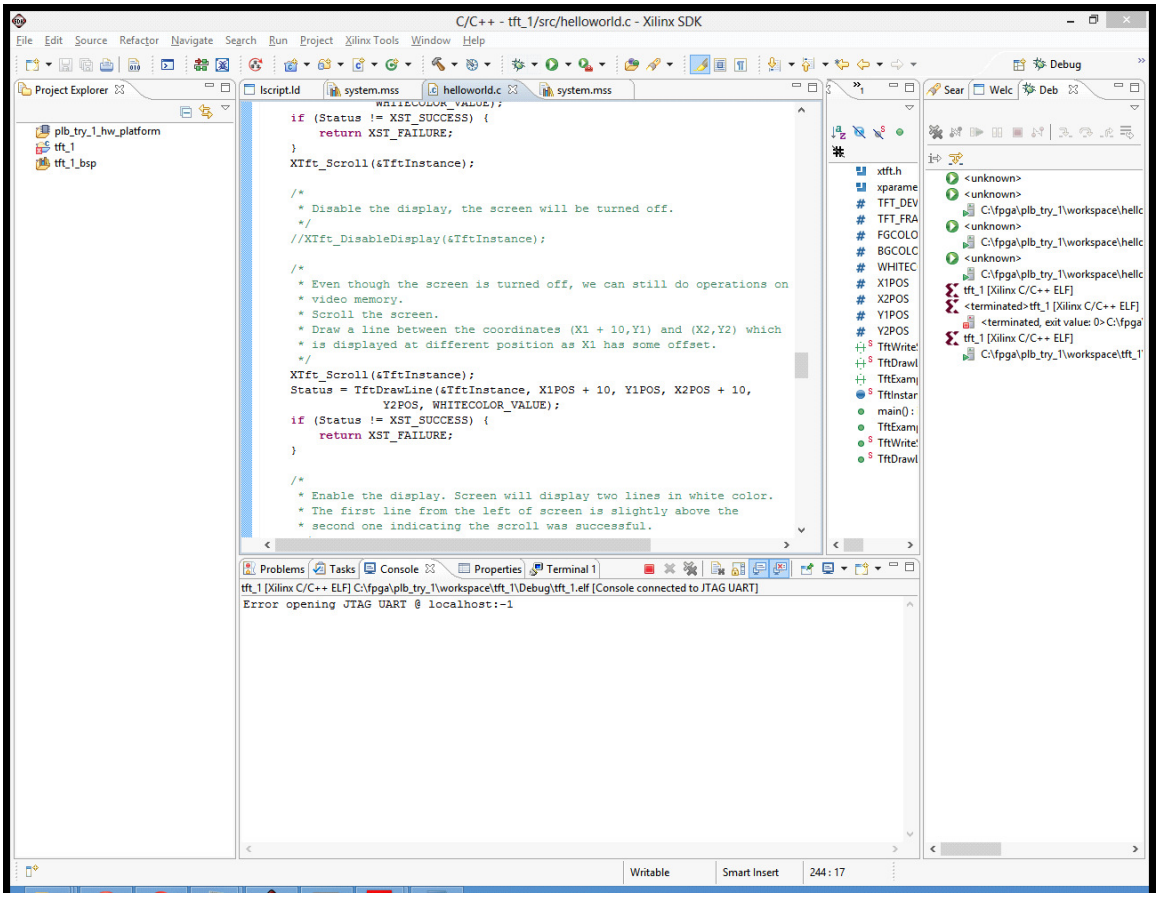
The xps_tft core access the video frame buffer directly with the DDR3 video port.

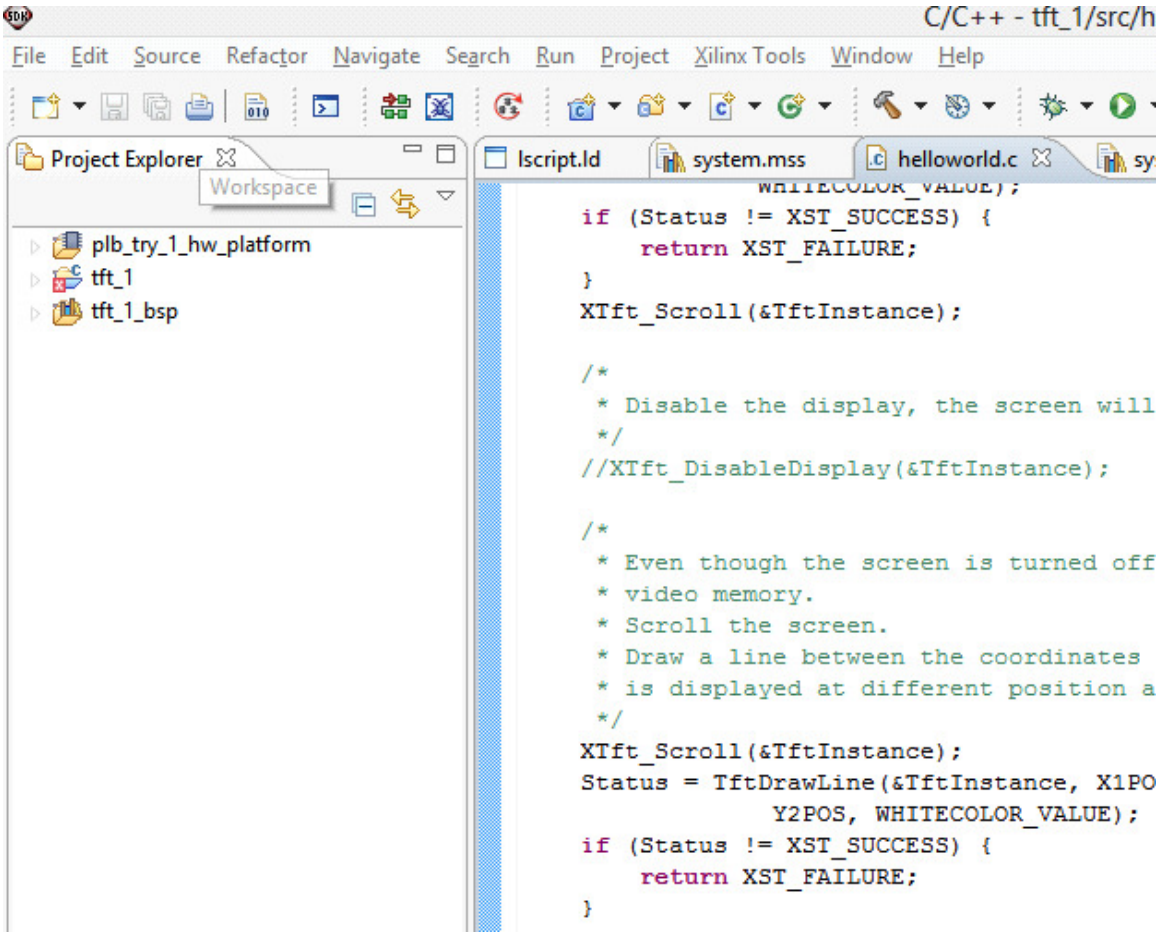
The xps_tft has 2 bus

-Slave PLB for internal registers

-Master PLB 64bit for frame buffer access

# C-Building the sample application in  Xilinx SDK






The application is generated by simply pasting the tft example (xtft_example.c) inside the default "hello world" application.

## D-Running the sample app

A sample application demonstrating the Xilinx tft support library and xps_tft core is found with EDK iunstallation (C:\Xilinx\14.3\ISE_DS\EDK\sw\XilinxProcessorIPLib\drivers\tft_v3_01_a \examples\xtft_example.c)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