uart6551x12

Overview

A UART component (Universal Asynchronous Transmitter / Receiver) is used for the asynchronous transmission and reception of data. Asynchronous referring to the lack of a clock signal during transmission or reception.

uart6551x12 is a WDC6551 register compatible uart. The uart is a 12-bit peripheral device. It may be used as an eight-bit peripheral by connecting the high order 4-bit data input lines to ground.

Baud rate is controlled by clock divider which assumes a 40MHz baud reference clock input. If a different clock frequency is used, then the divider table will need to be updated. The baud rate may also be controlled via a clock divider register. This register is 24 bits so gives a minimum frequency of 11.92 Hz assuming a 200MHz clock. (200MHz / 2^24).

Special Features

- WDC6551 register compatibility

Register Description

There are fifteen registers in the design. The function of the low order eight bits of the registers matches the 6551 function.

Reg	Moniker	Description
0	UART_TRB	Transmit and receive buffer. Data written is transmitted, on a read data available is read.
1	UART_STAT	Status Register. Returns status bits on a read, a write of any value will cause a reset of some of the command register bits
2	UART_CMD	Command register
3	UART_CTRL	Control register
4	UART_IRQS	IRQ status register
5	UART_MS	modem status
6	UART_LS	line status
7	UART_CMD1	command register
8	UART_CMD2	command register
9	UART_CMD3	command register
A	UART_CTRL1	Control register
B	UART_CTRL2	Control register
C	UART_CTRL3	Control register
D	UART_CLK1	clock divider value high order 12-bits
E	UART_CLK2	clock divider value low order 12-bits
F		reserved

UART_TRB (0)

This register is 12-bits wide. All bits may be used to transmit or receive data by the uart. Data written to the register is transmitted. A register read returns data received by the uart. When the fifo's are enabled writing to this register writes to the transmit fifo. Reading this register reads the receive fifo.

UART_STAT (1)

Uart status register. Writing any value to the status register resets some of the uart's command bits.

Bit	Status	
0	Parity Error	1 = parity error occurred, 0 = no error
1	Framing Error	1 = framing error
2	Overrun	1 = overrun
3	Rx Full	1 = receiver data available
4	Tx Empty	1 = open slot in transmit fifo
5	DCD	0 = data carrier present
6	DSR	0 = data set ready
7	IRQ	1 = irq occurred
8 to 11		reserved

UART_CMD (2)

Bit		
0	DTR	output 1 = low, 0 = high
1	RxIe	receiver interrupt enable 0 = enabled, 1 = disabled
2,3	RTS Control	
	00	output RTS high
	01	output RTS low, enable transmit interrupt
	10	output RTS low,
	11	output RTS low, send a break signal
4	LLB	1 = local loopback (receiver echo)
5 to 7	Parity Control	
	000	no parity
	001	odd parity
	011	even parity
	101	transmit mark parity (parity error disabled)
	111	transmit space parity (parity error disabled)

UART_CTRL (3)

Bit			
0 to 3	Baud Rate		
	0000	Use 16x external clock	This table is expanded using an extra control bit #27.
	0001	50	
	0010	75	
	0011	109.92	
	0100	134.58	
	0101	150	
	0110	300	
	0111	600	
	1000	1200	
	1001	1800	
	1010	2400	
	1011	3600	

	1100 4800 1101 7200 1110 9600 1111 19200	
4	Rx clock source	1 = external, 0 = baud rate generator
5,6	Word length 00 8 01 7 10 6 11 5	code for word length in bits
7	Stop Bit 0 1 1 1 if 8 bits and parity 1 1.5 if 5 bits and no parity 1 2 otherwise	

Selecting the clock divider register as the baud source allows any programmable baud rate.

UART_IRQS (4)

Uart irq status register.

Bit	Status	
	IRQ Status	
0,1	zero	these two bits are zero
2 to 4	IRQENC	encoded irq value (0 to 7)
5 to 7, 9 to 10	reserved	
8,11	irq	IRQ is set

UART_MS (5)

Uart modem status register.

Bit	Status	
	Modem Status Byte	
0	CTS	1 = CTS line changed state
1	DSR	1 = DSR line changed state
2	RI	1 = RI line changed state
3	DCD	1 = DCD line changed state
4	CTS	CTS state
5	reserved	
6	RI	RI state
7	reserved	
8 to 11	reserved	

UART_LS (6)

Uart line status register.

Bit	Status	
	Line Status Byte	

0	reserved	
1	reserved	
2	reserved	
3	reserved	
4	Break received	1 if a break signal is received
5	Tx Full	1 = transmit fifo full
6	reserved	
7	G Rcv Err	1 = global receiver error (set if any error status is set)
8 to 11	reserved	

UART_CMD1 (7)

Bit		
0	LSIe	line status change interrupt enable 1 = enabled
1	MSIe	modem status change interrupt enable 1 = enabled
2	RxToIe	receiver timeout interrupt enable 1 = enabled
3 to 11	reserved	

UART_CMD2 (8)

Not used, reserved

UART_CMD3 (9)

Not used, reserved

UART_CTRL1 (10)

Not used, reserved

UART_CTRL2 (11) (Fifo Control)

0	Fifo enable	1 = fifo's enabled
1	Rx Fifo Clear	1 = clear receiver fifo
2	Tx Fifo Clear	1 = clear transmit fifo
3	reserved	
4,5	Transmit Threshold 0 1 byte 1 ¼ full 2 ½ full 3 ¾ full	Threshold for DMA signal activation If the transit fifo count is less than the threshold then a DMA transfer is triggered.
6,7	Receive Threshold 0 1 byte 1 ¼ full 2 ½ full 3 ¾ full	Threshold for DMA signal activation. If the receive fifo count is greater than the threshold then a DMA transfer is triggered.

UART_CTRL3 (12)

0	hwfc	1 = automatic hardware flow control
1	reserved	

<table>
<tr><td>2</td><td>dmaEnable</td><td>1 = dma enabled</td></tr>
<tr><td>3</td><td>Baud Rate bit 4<table><tr><td>10000</td><td>38400</td></tr><tr><td>10001</td><td>57600</td></tr><tr><td>10010</td><td>115200</td></tr><tr><td>10011</td><td>230600</td></tr><tr><td>10100</td><td>460800</td></tr><tr><td>10101</td><td>921600</td></tr><tr><td>10110</td><td>reserved</td></tr><tr><td>10111</td><td>reserved</td></tr><tr><td>11xxx</td><td>reserved</td></tr></table></td><td>Extended baud rate selection bit, used in combination with bits 0 to 3.</td></tr>
<tr><td>4,5</td><td>reserved</td><td></td></tr>
<tr><td>6</td><td>selDV</td><td>1 = use clock divider register, 0 = use baud table</td></tr>
<tr><td>7</td><td>reserved</td><td></td></tr>
</table>

UART_CLK1 (13)

Bit		
0 to 11	CLKHI	clock divider bits 12 to 23

UART_CLK2 (13)

Bit		
0 to 11	CLKLO	clock divider bits 0 to 12

Ports

Signal	I/O	Wid	Purpose
rst_i	I	1	reset
clk_i	I	1	bus clock input
cs_i	I	1	circuit/core select
irq_o	O	1	interrupt request
	WISHBONE SIGNALS		
cyc_i	I	1	bus cycle valid
stb_i	I	1	data transfer strobe
ack_o	O	1	data transfer acknowledge
we_i	I	1	write enable
adr_i	I	4	address bits 0 to 3 (selects register)
dat_i	I	12	data input bus (ground bits 8 to 31 if using as an 8-bit peripheral)
dat_o	O	12	data output bus
	Modem Controls		
cts_ni	I	1	clear to send input active low.
rts_no	O	1	request to send output active low
dsr_ni	I	1	data set ready active low
dcd_ni	I	1	data carrier detect active low
dtr_no	O	1	data terminal ready active low
ri_ni	I	1	ring indicator active low
rxd_i	I	1	serial data input (receive)
txd_o	O	1	serial data output (transmit)
data_present	O	1	data is present in the receiver
rxDRQ_o	O	1	receiver DMA request
txDRQ_o	O	1	transmitter DMA request
xclk_i	I	1	external baud rate clock
RxC_i	I	1	external receiver clock