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## The ZipCPU

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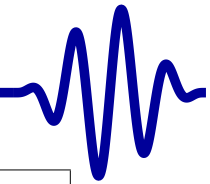
A resource efficient  
32-bit SoftCore CPU

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October, 2016





# Survey of CPUs



Feature	Nios	$\mu$ Blaze	ECO-32	RISC-V	OpenRISC	LM32	ZipCPU
Open Architecture?	<b>No</b>		<b>Yes</b>				
Number of Instructions	<b>86</b>	<b>129</b>	<b>61</b>	<b>50+</b>	<b>48+</b>	<b>62</b>	
OpCode Bits	6-17	6-11	6	10	6	6-32	
Interrupt/Exception Vectors	1	6	2	9+	14	32	
Register Indirect plus displacement (bits)	16			12	16		
Immediate direct addressing (bits)	16, using R0=0						
Relative branching (bits)	16		26 (28)	21	26	21	
Conditional branching (bits)	16		16 (18)	13	26	16	
Register Size (bits)	32			32 (Opt. 64 Exts.)		32	
Special Purpose Registers	<b>6</b>	<b>25</b>	<b>6</b>	<b>66+</b>	<b>65+</b>	<b>10</b>	
General Purpose Registers	32 (but R0=0, others are unusable, ... 24)						
8-bit data	Yes						
16-bit data	Yes						
32-bit data	Yes						
64-bit data	No			Yes, by extension		No	
32-bit floats	Optional		No	Yes, by extension		No	
64-bit floats	No			Yes, by Extension		No	
Vector instructions	No			Not yet	64-bits, Ext	No	
MMU	Yes, but optional						
Instruction Cache	Yes, configurable						
Data Cache	Yes, configurable						