Aquarius

A Pipelined RISC CPU

What is Aquarius

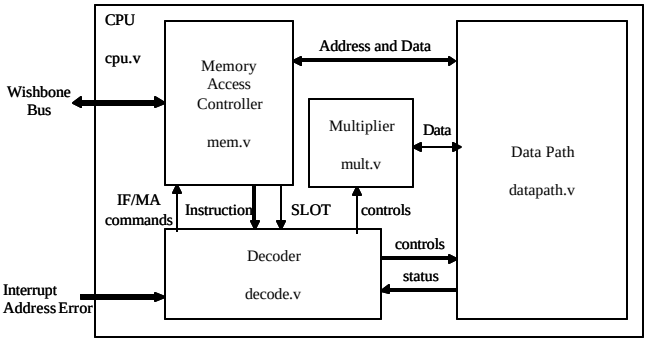
Aquarius is a Core IP of pipelined RISC CPU and can execute SuperH-2* instructions. Aquarius and related information are released to OpenCores Organization web site (www.opencores.org). You can freely download and use all resources on the site.*: SuperH is a trademark of Renesas Technology Corp.

What is SuperH

1. SuperH is a very popular CPU core. The software development environments such as C compiler have been well prepared. The GNU C compiler for SuperH is very famous and easy to get.
2. SuperH-2 is a CPU for MCU (Micro Controller Unit). Then the CPU need not handle complex exception recovering such as memory fault exception from MMU (Memory Managing Unit). This means SuperH-2 has simple structure, easiness to design, and it does not consume many logic gates and power.
3. All SuperH-2 instructions have 16bit length. It also makes the hardware very simple. And most important aspect from 16bit fixed length of instructions is that the object code size compiled from C source programs becomes very small.

Aquarius Features

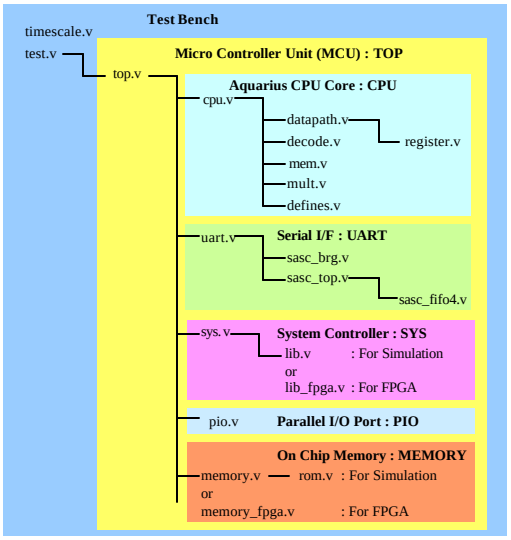
1. Instruction set is compatible with SuperH-2.
2. Bus interface is compatible with WISHBONE.
3. Aquarius is written in Verilog RTL codes.
4. Aquarius has verified on a test bench by both vector simulation and FPGA implementation with GNU Assembler and C Compiler.
5. Interrupts and Exceptions are fully supported.
6. Low Power Mode (SLEEP) is supported.
7. Some small applications are providedincluding debugging monitor for a FPGA board.
8. A complete Document with over 100 pages, describing Usage of Aquarius, FPGA Implementation and Inside Aquarius, is provided.



CPU Block Diagram

Deliverables

1. Verilog RTL codes for CPU, and Test Bench including modules comprising MCU, such as UART, System Controller, Parallel I/O Interface, and Internal Memories (ROM/RAM).
2. Verification Resources, such as Converter from S-format to Verilog format for ROM coding, and Assemble Source Programs for Vector Simulation.
3. FPGA Resources, such as Circuit Schematics of Interface Board, Converter from S-format to Xilinx BlockRAM INIT statements for RAM initialization, and a sample of User Constraints File.
4. Small Applications written in C Sources including LCD Test Program, Clock using interval interrupt, Debugging Monitor, and Calculation of Circular Constant (Pi).



Aquarius RTL Tree

Download

Documents, RTL Source codes and related Tools can be downloaded from the OpenCores CVS directory "Aquarius".

FPGA Verification System

Aquarius has verified by using FPGA Verification System. It consists of Xilinx VirtexE, LCD Display Interface, Key Matrix Interface and RS-232C Interface.

FPGA System

Performance

Aquarius CPU core and related peripheral modules have been configured in both Xilinx and Altera. Following table shows their performance.

FPGA Device	Performance
Xilinx VirtexE (XCV300E)	2753 slices @21MHz
Altera Stratix (EP1S10)	7499 cells @31MHz

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