ctl_bus_inc_oe — INPUT VCC

clrpc — INPUT VCC

NOT inst9

abus[15..0] — BIDIR VCC

AND2 inst3

TRI inst4

Address increment / decrement

inc_dec
limit6
decrement
d[15..0]
carry_in
address[15..0]
inst_inc_dec

ctl_inc_limit6 — INPUT VCC
ctl_inc_dec — INPUT VCC

ctl_inc_cy — INPUT VCC

abusz[15..0]

DFFE
PRN
D   Q
ENA
CLRN
alatch

clk — INPUT VCC
ctl_al_we — INPUT VCC

nreset — INPUT VCC

ctl_apin_mux2 — INPUT VCC
ctl_apin_mux — INPUT VCC

address_mux
in1[15..0]
out[15..0]
in0[15..0]
select
mux

address_mux
in1[15..0]
out[15..0]
in0[15..0]
select
inst7

OR8
Q[15]
Q[14]
Q[13]
Q[12]
Q[11]
Q[10]
Q[9]
Q[8]
inst6

OR8
Q[7]
Q[6]
Q[5]
Q[4]
Q[3]
Q[2]
Q[1]
Q[0]
inst5

Q[15..0]

NOT
n

NOR2
inst

OUTPUT — address_is_1

OUTPUT — address[15..0]

A kludge to work around the latch => flop translation

PROJECT	A-Z80	MODULE	address_latch
DESIGNER	Goran Devic		
DATE	May 17, 2014, 2016	REV	1.5

address_latch.bdf