Refresh generator logic, USPTO 4,332,008 by Shima et al.   FIG. 9A

nM1_int   INPUT
clk   INPUT VCC

DFFE  PRN  D  Q  ENA  CLRN  m1_ff
DFFE  PRN  D  Q  ENA  CLRN  q1_ff   q1
DFFE  PRN  D  Q  ENA  CLRN  q2_ff   q2NOT  noff  nq2
NAND2  inst_nrfsh
OUTPUT  nM1_out
OUTPUT  nRFSH_out

nreset   INPUT VCC

NOT

MREQ DURING REFRESH

DFFE  PRN  D  Q  ENA  CLRN  mreq
DFFE  PRN  D  Q  ENA  CLRN  mreq
NOT  noff2
NAND2  inst_nmreq
BNOR2  inst
OUTPUT  nMREQ_out

nreset

nMEMRQ_int

STANDARD MEM REQ

(End of patented circuit)

nreset
setM1   INPUT VCC
timings_en   INPUT VCC

DFFE  PRN  D  Q  ENA  CLRN  m1_ff
DFFE  PRN  D  Q  ENA  CLRN  m1_ff
DFFE  PRN  D  Q  ENA  CLRN  m1_ff
NOR2  inst16
NOR2  inst18
wait_m1
m1_mreq

MREQ DURING M1

nreset
in_intr   INPUT VCC
ctl_mRead   INPUT VCC

DFFE  PRN  D  Q  ENA  CLRN  mrd_ff
DFFE  PRN  D  Q  ENA  CLRN  mrd_ff
DFFE  PRN  D  Q  ENA  CLRN  mrd_ff
OR2  inst36
wait_mrd
mrd_mreq

MEMORY READ

nreset
ctl_mWrite   INPUT VCC

DFFE  PRN  D  Q  ENA  CLRN  mwr_ff
DFFE  PRN  D  Q  ENA  CLRN  mwr_ff
DFFE  PRN  D  Q  ENA  CLRN  mwr_ff
OR2  inst38
wait_mwr
mwr_mreq
mwr_wr

MEMORY WRITE

nreset
ctl_iorw   INPUT VCC

DFFE  PRN  D  Q  ENA  CLRN  iorq_ff
DFFE  PRN  D  Q  ENA  CLRN  iorq_ff
DFFE  PRN  D  Q  ENA  CLRN  iorq_ff
DFFE  PRN  D  Q  ENA  CLRN  iorq_ff
OR3  inst19
iorq

nreset

IO READ /. WRITE

fIORead   INPUT VCC
iorq
fIOWrite   INPUT VCC
AND2  inst1
AND2  inst2
ioRead
ioWrite

wait_iorq
iorq_Tw   INPUT VCC

DFFE  PRN  D  Q  ENA  CLRN  intr_ff
DFFE  PRN  D  Q  ENA  CLRN  intr_ff
OR2  inst40
intr_iorq

hold_clk_wait   INPUT VCC
NOT  inst4
nreset

IORQ DURING INTERRUPT ACK

mwr_mreq   mrd_mreq   m1_mreq
NOR3  inst33
nMEMRQ_int

ioRead   mrd_mreq   m1_mreq
NOR3  inst34
OUTPUT  nRD_out

mwr_wr
ioWrite
NOR2  inst37
OUTPUT  nWR_out

iorq
intr_iorq
NOR2  inst39
OUTPUT  nIORQ_out

wait_mrd
wait_m1   wait_iorq   wait_mwr
OR4  inst3
OUTPUT  latch_wait

PROJECT  A-Z80    MODULE  memory_ifc
DESIGNER  Goran Devic
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memory_ifc.bdf