AC97 Controller IP Core

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Revision History

Rev.	Date	Author	Description
0.1	11/5/01	Rudolf Usselmann	First Draft
1.0	19/5/01	RU	Filled in all of the missing parts: Added architecture descriptions. Added Suspend/Resume description. Fixed registers. Added source file layout. Added Core configuration.
1.1	10/8/01	RU	Removed RTY_O output. Added Clock and Reset Inputs. Changed IO names to be more clear. -Uniquifyed define names to be core specific.
1.2	19/9/02	RU	Minor data sheet fixes

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Introduction

This is a simple AC97 Controller IP core. It supports one AC97 codec, with 6 output and 3 input channels.

This AC97 Controller s fully AC97 Revision 2.2 compliant. it only supports AC97 Audio Codecs.

Some of the main features are:

1. Variable and Fixed Sample Rate Support, up 48 Khz
2. 16, 18 and 20 bit Sample Size Support
3. 6 Output Channel Surround Sound Support
4. Stereo Input channel Support
5. Mono Microphone Channel Support
6. External DMA Engine Support

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Architecture

Below figure illustrates the overall architecture of the core. This AC97 IP Core supports up to 6 output and 3 input channels.

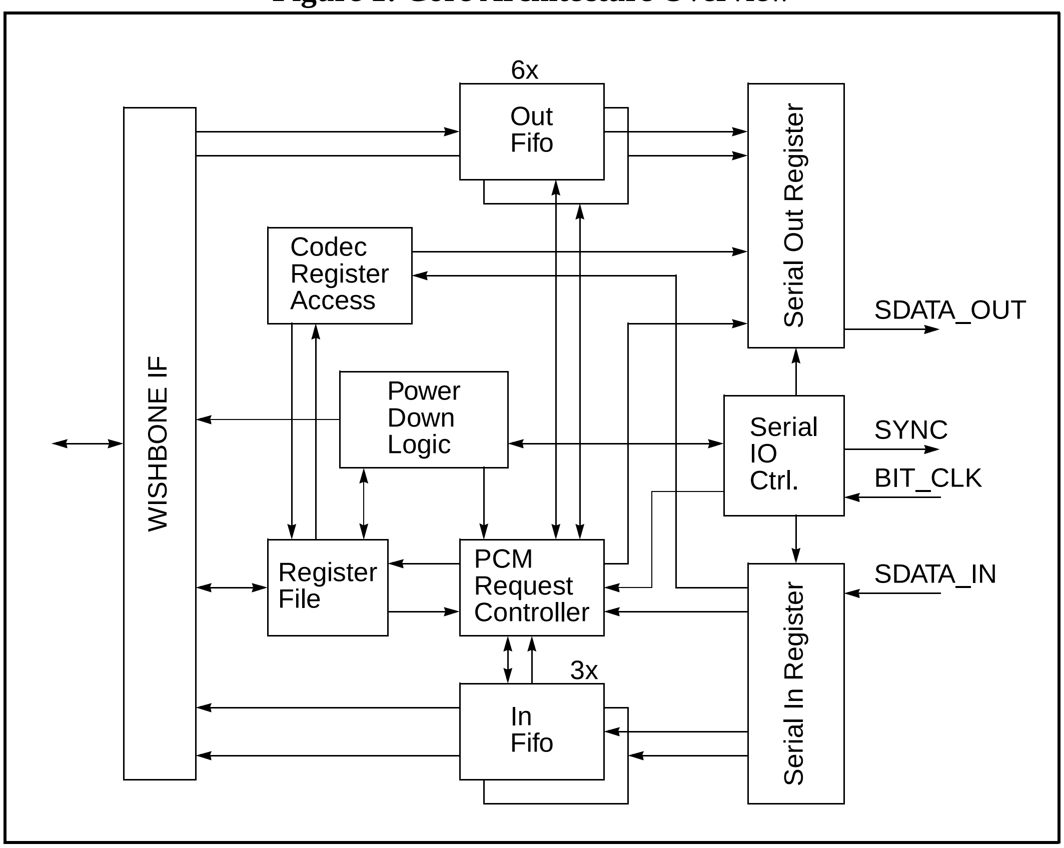
The Output Channels are:

- Left & Right Main
- Left and Right Surround
- Center and LFE

The Input Channels are:

- Stereo Input
- Mono Microphone Input

Figure 1: Core Architecture Overview



2.1. WISHBONE Interface

The AC97 Controller core includes a WISHBONE host interface.This interface is WISHBONE SoC bus specification Rev. B compliant. This implementation implements a 32 bit bus width and does not support other bus widths.

2.2. Serial IO Register

The Serial IO Registers convert the parallel input from the FIFOs and control logic to a serial bit stream and vise versa. The Serial Bit Stream is synchronized to the Sync signal from the Serial IO Controller.

2.3. Serial IO Controller

The Serial IO controller, generates a Sync signal every 20.83uS and control signals for the Serial IO Registers and PCM Request Controller.

2.4. IN/OUT FIFOs

The Input/Output FIFOs hold the data to be transmitted/has been received. The FIFOs are 4 entries deep. Each entry is 32 bits wide. Depending on the selected sample size, the FIFOs can hold 8 (16 bit sample size) or 4 (18 or 20 bit sample size) samples.

2.5. PCM Request Controller

The PCM Request Controller monitors the requests from the Codec and controls when data is being sent out or latched. The PCM Request Controller supports variable and fixed sample rate operations.

2.6. Codec Register Access

The Codec Register Access module sends requests to the Codec whenever the host wants to read or write a Codec register. It also provides feedback when a Codec register read has completed and the data is available for the host to retrieve.

2.7. Power Down Logic

In order for the AC97 sub system to be placed in to power down mode, the host has to write to the Codec register at address 26h a certain value to initiate power down. The Power Down Module monitors the Codec and reports back to the host when Power Down mode has been entered. It also includes special signaling to the Codec, when the host wants to wake up the AC97 subsystem from Power Down Mode.

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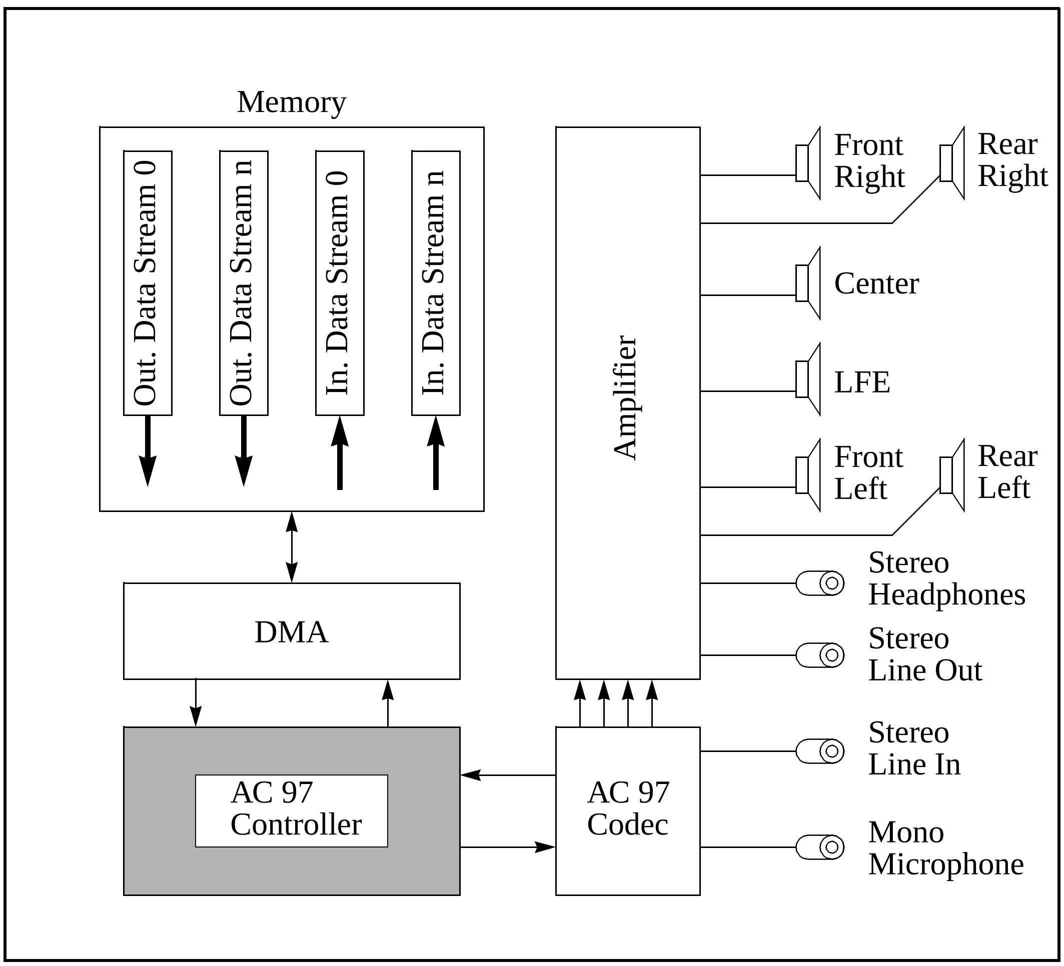
Operation

3.1. System Overview

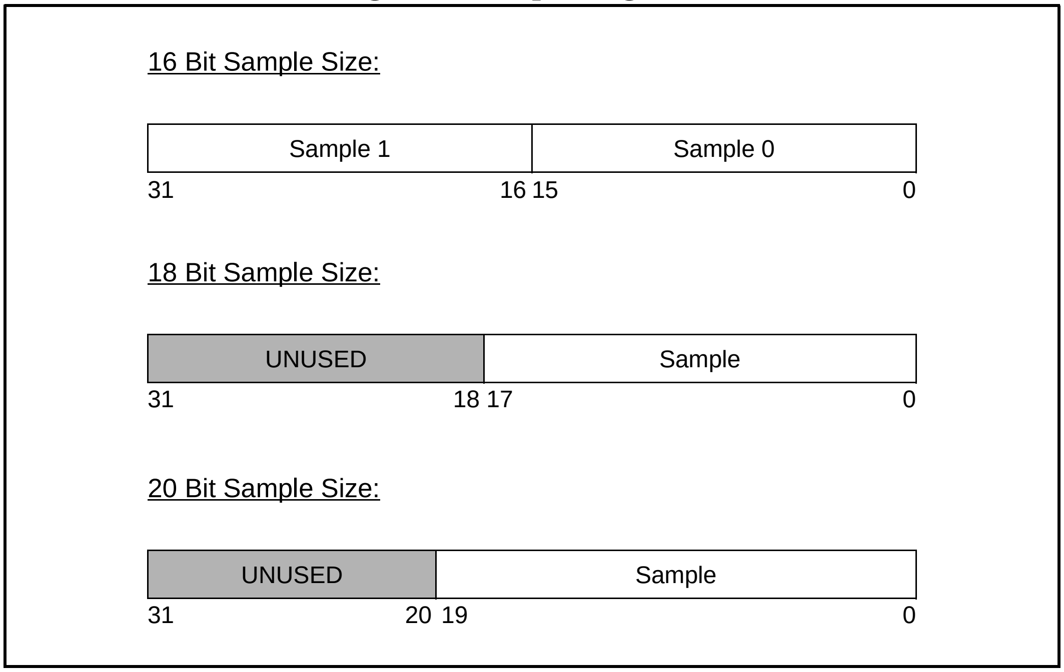
This section illustrates a simplified system level overview. In this example, a DMA engine performs automatic playback and recording functions.



3.2. Sample Alignment

Samples are always LSB aligned. Depending on the sample size, either two or one samples are contained in one word. The figure below illustrates the sample alignment.

Figure 2: Sample Alignment



3.3. Sample Rate

This AC97 Controller IP Core supports both fixed and variable rate sample rates. When SR bit is set in the Channel Configuration sub-field, variable sample rate is activated. In this mode the controller will only transmit samples when the AC97 Codec requests them, and will latch received samples when the AC97 Codec sets the valid bits for the incoming samples. In fixed rate mode (SR bit cleared) the AC97 Controller will transmit and receive samples at a fixed 48 Khz rate.

3.4. Suspend & Resume

The AC97 Controller supports power management. Entering and exiting power down mode is done by writing to various registers in the AC97 subsystem.

To place the AC97 subsystem in to power down mode the system must first disable all output channels. Then it must place the codec in to sleep mode by writing the appropriate value to the codec register at address 0x26 (see the specification of the codec for more detail). Once the codec has powered down, the AC97 Controller will assert the suspended output, and set the SUSP bit in the CSR register. After the AC97 Controller has asserted suspended output, all of its clocks may be turned off.

To resume normal operations, a one must be written to the SUSP bit, after all clocks are stable. The AC97 Controller will signal to the codec to wake up. Once the AC97 Codec has resumed operations, the SUSP bit in the AC97 Controller CSR register will be cleared and normal operations may resume.

3.5. DMA operations

When the DE bit in the Channel Configuration sub-field is set, DMA operations are enabled. The AC97 Controller Core will assert DMA request when the FIFO threshold has been reached, and de-assert DMA request when the FIFO is above/below the threshold.

3.6. Interrupts

The AC97 Controller can generate an interrupt when any of the following conditions have occurred: 1) FIFO Overrun; 2) FIFO Underrun; 3) FIFO threshold reached. Each channel can generate an interrupt for the above conditions.

The host must read the interrupt source register to clear the interrupt after it has dealt with it and "fixed" the interrupt source.

3.7. AC97 Reset

The AC97 Controller will stretch the WISHBONE reset to at least 1uS for the AC97 Codec. Software may also perform a Cold Reset to the AC97 Codec by writing a 1 to the CRST bit in the CSR register. Writing a 1 to the CSR register CRST bit will assert reset to the Codec for at least 1uS.

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Core Registers

This section describes all control and status registers inside the AC 97 Controller core. The *Address* field indicates a relative address in hexadecimal. *Width* specifies the number of bits in the register, and *Access* specifies the valid access types to that register. Where RW stands for read and write access, RO for read only access. A 'C' appended to RW or RO, indicates that some or all of the bits are cleared after a read.

All RESERVED bits should always be written with zero. Reading RESERVED bits will return undefined values. Software should follow this model to be compatible to future releases of this core.

Table 1: Control/Status Registers

Name	Addr.	Width	Access	Description
CSR	0	32	RW	Main Configuration/Status Register
OCC0	4	32	RO	Output Channel Configuration Register 0
OCC1	8	32	RW	Output Channel Configuration Register 1
ICC	c	32	RW	Input Channel Configuration Register
CRAC	10	32	RW	Codec Register Access Command
INTM	14	32	RW	Interrupt Mask
INTS	18	32	RW	Interrupt Status Register
	1c			
OCH0	20	32	RW	Output Channel 0
OCH1	24	32	RW	Output Channel 1
OCH2	28	32	RW	Output Channel 2
OCH3	2c	32	RW	Output Channel 3
OCH4	30	32	RW	Output Channel 4
OCH5	34	32	RW	Output Channel 5
ICH0	38	32	RW	Input Channel 0

Table 1: Control/Status Registers

Name	Addr.	Width	Access	Description
ICH1	3c	32	RW	Input Channel 1
ICH2	40	32	RW	Input Channel 2

4.1. Control Status Register (CSR)

This is the main control and status register.

Table 2: CSR Register

Bit #	Access	Description
31:2	RO	RESERVED
1	RW	SUSP Reading this bit will return the current state of the AC97 subsystem: 1 - The AC97 subsystem is suspended 0 - Normal Operation Writing a one to this bit, will start the resume procedure if the AC97 subsystem is suspended.
0	WO	CRST AC97 Cold Reset Writing a one to this bit will cause the codec to be hard reset.

Value after reset:

CSR: 0000h

4.2. Output Channel Configuration Registers (OCCn)

The Output Channel Configuration Registers allow for each channel to be configured independently.

Table 3: OCC Register 0

Bit #	Access	Description
31:24	RW	Output Channel 3: Surround Left Channel Configuration
23:16	RW	Output Channel 2: Center Channel Configuration
15:8	RW	Output Channel 1: Front Right Channel Configuration
7:0	RW	Output Channel 0: Front Left Channel Configuration

Value after reset:

OCC0: 0000 h

Table 4: OCC Register 1

Bit #	Access	Description
31:16	RW	RESERVED
15:8	RW	Output Channel 5: LFE Channel Configuration
7:0	RW	Output Channel 4: Surround Right Channel Configuration

Value after reset:

OCC1: 0000 h

4.3. Input Channel Configuration (ICC)

This register holds the configuration information for all output channels.

Table 5: ICC Register

Bit #	Access	Description
31:24	RW	RESERVED
23:16	RW	Input Channel 2: Microphone Channel Configuration
15:8	RW	Input Channel 1: Right Channel Configuration
7:0	RW	Input Channel 0: Left Channel Configuration

Value after reset:

ICC: 0000 h

4.4. Channel Configurations (Sub-field)

The Channel Configuration is the sub field in the OCCn and ICC registers for each channel. Each Channel configurations, is composed of the following bits.

Table 6: Channel Configuration

<table>
<tr><th>Bit #</th><th>Access</th><th>Description</th></tr>
<tr><td>7</td><td>RW</td><td>RESERVED</td></tr>
<tr><td>6</td><td>RW</td><td>DE
DMA Enable
1 - DMA Enabled
0 - DMA Disabled</td></tr>
<tr><td>5:4</td><td>RW</td><td>FS
FIFO Threshold
<table>
<tr><th>5:4</th><th>Output Channel</th><th>Input Channel</th></tr>
<tr><td>00</td><td>FIFO 1/4 Empty</td><td>FIFO 1/4 Full</td></tr>
<tr><td>01</td><td>FIFO 1/2 Empty</td><td>FIFO 1/2 Full</td></tr>
<tr><td>10</td><td>FIFO 3/4 Empty</td><td>FIFO 3/4 Full</td></tr>
<tr><td>11</td><td>FIFO Empty</td><td>FIFO Full</td></tr>
</table></td></tr>
<tr><td>3:2</td><td>RW</td><td>SS
Sample Size
00 - 16 Bit
01 - 18 Bit
10 - 20 Bit</td></tr>
<tr><td>1</td><td>RW</td><td>SR
Sample Rate
1- Variable Sample Rate (On Demand)
0 - Fixed Sample rate (48 Khz)</td></tr>
<tr><td>0</td><td>RW</td><td>EN
Channel Enable
1 - Channel Enabled
0 - Channel Disabled (or Power Down)</td></tr>
</table>

4.5. Codec Register Access Command (CRAC)

The Codec Register Access Command Register, provides a simple mechanism to access registers in the Codec. A write to this register will initiate a transfer to/from the codec registers.

Table 7: Codec Register Access Command

Bit #	Access	Description
31	RW	Read/Write Select 1 - Read 0 - Write
30:23	RO	RESERVED
22:16	RW	Codec Register Address
15:0	RW	Codec Register Data This is the data that is written to the selected codec register when the write operation is selected. Reading This field will return the last value received from the codec.

Value after reset:

CSCn: 0000h

4.6. Interrupt Mask Register (INTM)

The Interrupt Mask register defines the functionality of the *int* output. A bit set to a logical 1 enables the generation of the interrupt for that source, a zero disables the generation of an interrupt.

Table 8: Interrupt Mask Register

Bit #	Access	Description
31:29	RO	RESERVED
28	RW	Input Channel 2: FIFO Overrun
27	RW	Input Channel 2: FIFO Underrun
26	RW	Input Channel 2: FIFO at Threshold
25	RW	Input Channel 1: FIFO Overrun
24	RW	Input Channel 1: FIFO Underrun
23	RW	Input Channel 1: FIFO at Threshold
22	RW	Input Channel 0: FIFO Overrun
21	RW	Input Channel 0: FIFO Underrun

Table 8: Interrupt Mask Register

Bit #	Access	Description
20	RW	Input Channel 0: FIFO at Threshold
19	RW	Output Channel 5: FIFO Overrun
18	RW	Output Channel 5: FIFO Underrun
17	RW	Output Channel 5: FIFO at Threshold
16	RW	Output Channel 4: FIFO Overrun
15	RW	Output Channel 4: FIFO Underrun
14	RW	Output Channel 4: FIFO at Threshold
13	RW	Output Channel 3: FIFO Overrun
12	RW	Output Channel 3: FIFO Underrun
11	RW	Output Channel 3: FIFO at Threshold
10	RW	Output Channel 2: FIFO Overrun
9	RW	Output Channel 2: FIFO Underrun
8	RW	Output Channel 2: FIFO at Threshold
7	RW	Output Channel 1: FIFO Overrun
6	RW	Output Channel 1: FIFO Underrun
5	RW	Output Channel 1: FIFO at Threshold
4	RW	Output Channel 0: FIFO Overrun
3	RW	Output Channel 0: FIFO Underrun
2	RW	Output Channel 0: FIFO at Threshold
1	RW	Codec Register Write Done
0	RW	Codec Register Read Done

Value after reset:

INTM: 0000h

4.7. Interrupt Status Register (INTS)

The Interrupt Source Register identifies the source of an interrupt.

Table 9: Interrupt Mask Register

Bit #	Access	Description
31:29	RO	RESERVED

Table 9: Interrupt Mask Register

Bit #	Access	Description
28	ROC	Input Channel 2: FIFO Overrun
27	ROC	Input Channel 2: FIFO Underrun
26	ROC	Input Channel 2: FIFO at Threshold
25	ROC	Input Channel 1: FIFO Overrun
24	ROC	Input Channel 1: FIFO Underrun
23	ROC	Input Channel 1: FIFO at Threshold
22	ROC	Input Channel 0: FIFO Overrun
21	ROC	Input Channel 0: FIFO Underrun
20	ROC	Input Channel 0: FIFO at Threshold
19	ROC	Output Channel 5: FIFO Overrun
18	ROC	Output Channel 5: FIFO Underrun
17	ROC	Output Channel 5: FIFO at Threshold
16	ROC	Output Channel 4: FIFO Overrun
15	ROC	Output Channel 4: FIFO Underrun
14	ROC	Output Channel 4: FIFO at Threshold
13	ROC	Output Channel 3: FIFO Overrun
12	ROC	Output Channel 3: FIFO Underrun
11	ROC	Output Channel 3: FIFO at Threshold
10	ROC	Output Channel 2: FIFO Overrun
9	ROC	Output Channel 2: FIFO Underrun
8	ROC	Output Channel 2: FIFO at Threshold
7	ROC	Output Channel 1: FIFO Overrun
6	ROC	Output Channel 1: FIFO Underrun
5	ROC	Output Channel 1: FIFO at Threshold
4	ROC	Output Channel 0: FIFO Overrun
3	ROC	Output Channel 0: FIFO Underrun
2	ROC	Output Channel 0: FIFO at Threshold
1	ROC	Codec Register Write Done
0	ROC	Codec Register Read Done

Value after reset:

INTS: 0000h

4.8. OCHn and ICHn Registers

These are the access ports for the internal data fifos.

OCHn are the output fifos (data that will be send to the codec), ICHn are the input fifos (data received from the codec). Please see section “3.2. Sample Alignment” on page 8 for data format.

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Core IOs

5.1. Interface IOs

The SoC interface is WISHBONE Rev B compliant.

Table 10: Host Interface (WISHBONE)

Name	Width	Direction	Description
wb_clk_i	1	I	Clock Input
wb_rst_i	1	I	Reset Input (Asynchronous Reset)
wb_addr_i	32	I	Address Input
wb_data_i	32	I	Data Input
wb_data_o	32	O	Data Output
wb_sel_i	4	I	Indicates which bytes are valid on the data bus.
wb_we_i	1	I	Input for slave. Indicates a Write Cycle when asserted high.
wb_cyc_i	1	I	Input for slave. Encapsulates a valid transfer cycle.
wb_stb_i	1	I	Input for slave. Indicates a valid transfer.
wb_ack_o	1	O	Acknowledgment Output. Indicates a normal Cycle termination.
wb_err_o	1	O	Error acknowledgment output. Indicates an abnormal cycle termination.

In addition, the AC 97 Controller has a power management interface, that allow the core to be placed in to a power saving mode and turn off the clocks.

Table 11: Power Management Interface

Name	Width	Direction	Description
suspended_o	1	O	Indicates that the AC 97 Controller has entered suspended mode. When this signal is asserted, all clocks may be turned off.
int_o	1	O	Interrupt Output
dma_req_o	9	O	DMA Request Outputs
dm_ack_i	9	I	DMA Acknowledgement Inputs

5.2. AC97 Codec Interface IOs

This section describes the AC97 Codec interface signals.

Table 12: AC97 Codec Interface IOs

Name	Width	Direction	Description
bit_clk_pad_i	1	I	Serial Data Bit Clock
sync_pad_o	1	O	Frame Sync Output
sdata_pad_o	1	O	Serial Data Output
sdata_pad_i	1	I	Serial Data Input
ac97_reset_pad_o	32	O	AC97 Codec Reset Output

Appendix A

Core HW Configuration

This Appendix describes the configuration of the core.

A.1. Supported Channel Select

These section allows you to select which channels should be supported in any given implementation. You must comment out the define statement for each channel(s) that you do not wish to implement.

```
// Surround Left + Right
`define AC97_SURROUND  1

// Center Channel
`define AC97_CENTER    1

// LFE Channel
`define AC97_LFE       1

// Stereo Input
`define AC97_SIN       1

// Mono Microphone Input
`define AC97_MICIN     1
```

A.2. Register Base Address Select

This define statement specifies the base address for all registers within the core. This should be a simple combinatorial Verilog statement. The signal *wb_addr_i* id the WISHBONE address bus, which is 32 bits wide. The lower 4 address bit are used to select the individual registers and should not be used for the base address decoding.

```
`define          AC97_REG_SEL    (wb_addr_i[31:29] == 3'h0)
```

A.3. Time Reference Setup

The AC97 Controller IP Core requires a time reference for various AC97 signaling procedures. A prescaler is used to generate a 250nS time interval. This define statement specifies the number of WISHBONE clock cycles (less one) it takes for 250nS to elapse. For example, for a 200 MHz wishbone clock, this value is 49 (250nS / 5nS - 1).

```
`define    AC97_250_PS    6'd49
```

A.4. Reset Pulse Width Setup

This define statement defines the width of the AC97 reset pulse. AC97 specification defines a minimum length of 1uS. The reset pulse width counter is driven by the prescaler that has been setup in section A.3. For a 1uS reset pulse this value should be set to 4 (2*250nS = 1uS). This value should typically not be modified, as it is driven by the Time Reference prescaler.

```
`define    AC97_RST_DEL    3'd4
```

A.5. Resume Pulse Width Setup

This define statement defines the width of the AC97 resume pulse. AC97 specification defines a minimum length of 1uS. The resume pulse width counter is driven by the prescaler that has been setup in section A.3. For a 1uS resume pulse this value should be set to 4 (2*250nS = 1uS). This value should typically not be modified, as it is driven by the Time Reference prescaler.

```
`define    AC97_RES_SIG    3'd5
```

A.6. Suspend Detection Setup

This define statement specifies how many WISHBONE cycles to wait for a ac97 bit clock change before deciding that the AC97 Codec has suspended operations. Both the rising and falling edge of the bit clock will clear this counter. We should wait for at least two bit clock cycles before signaling suspend. The bit clock cycle time is about 81.4nS. For a 200 Mhz WISHBONE clock this would mean we would have to wait for (81.4nS * 2 / 5nS) about 33 cycles.

```
`define    AC97_SUSP_DET    6'd33
```

Appendix B

File Structure

This section outlines the hierarchy structure of the AC 97 Controller core Verilog Source files.

Figure 3: AC97 IP Core File Structure